Design of an RF-power amplifier and optimization of the thermal properties

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Abstract

This bachelor thesis covers the realization and thermal properties optimization of a broadband Radio Frequency (RF) power amplifier in the Reader of Radio Frequency Identification (RFID) applications in the Super High Frequency (SHF) band. Based on the preceding internship at the Fraunhofer Institute for Microelectronic Circuits and Systems (IMS), a number of different designs are developed in simulation to improve the thermal properties from some cost-effective aspects. Furthermore, some designs are selected for production and verification. Through measurement, their electrical characteristics and thermal properties are compared and evaluated respectively. This provides reference for subsequent production and application.

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List of Abbreviations

Abbreviation	Definition
RFID	Radio Frequency Identification
SHF	Super High Frequency
IC	Integrated Circuit
PCB	Printed Circuit Board
RF	Radio Frequency
EEsof	Electronic Engineering software
EDA	Electronic Design Automation
IMS	Fraunhofer Institute for Microelectronic Circuits and Systems
IR	Infrared Radiation
LAN	Local Area Network
IoT	Internet of Things
ID	Identity Document
AC	Alternating Current
DC	Direct Current
ASK	Amplitude Shift Keying
CPW	Coplanar Waveguide
CPWG	Coplanar Waveguide with lower Ground plane
S-parameters	Scattering Parameters

ADS	Advanced Design System
SMA	Subminiature version A
DUT	Device Under Test

List of Symbols

Latin characters

Symbol	Unit	Definition
$V_{CC1}/V_{CC2}/V_{CC3}$	V	Supply voltage of power amplifier
V_{REF}	V	Power amplifier enable and reference voltage
T_j	°C	Maximum junction temperature
a_1	W	Incident power wave of gate 1
a_2	W	Incident power wave of gate 2
b_1	W	Reflected power wave of gate 1
b_2	W	Reflected power wave of gate 2
w	m	Track width
t	m	Track thickness
h	m	Dielectric thickness
Z_0	Ω	Characteristic impedance
W	m	Effective width
H	m	Effective thickness
g	m	gap between the track and ground plane
S_{11}	dB	Input port power reflection coefficient
S_{22}	dB	Output port power reflection coefficient
S_{21}	dB	Forward power gain

S_{12}	dB	Reverse power gain
R_t	K/W	Thermal resistance
L	m	Length or thickness of the material
A	m^2	Cross-sectional area
ΔT	°C	Temperature difference across the material
Q	W	Heat current
f	GHz	Frequency range
P_{1dB}	dBm	Output 1dB com-pression point
I_{CC}	mA	Supply current
P_{input}	W	Input power
P_{output}	W	Output power
P_{heat}	W	Heat dissipation
A_{adapter}	dB	Attenuation of the adapter
$A_{\mathrm{attenuator}}$	dB	Attenuation of the attenuator
A_{wire}	dB	Attenuation of the wire
$A_{\mathrm{attenuator\ with\ wire}}$	dB	Attenuation of the attenuator with wire
$G_{\mathrm{in\ EM}}$	dB	Gain of PCB in the electrical measurement
$G_{\mathrm{in\ TM}}$	dB	Gain of PCB in the thermal measurement
$T_{max\,\mathrm{in\ TM}}$	°C	Maximum temperature in the thermal measurement
$T_{max\,\mathrm{in\ TS}}$	°C	Maximum temperature in the thermal simulation

Greek characters

Symbol	Unit	Definition
κ	W/(m·K)	Thermal conductivity
θ	rad	Polar angle
ε_{eff}	-	Effective dielectric constant
ε_r	-	Dielectric constant
θ_{JA}	K/W	Thermal resistance from the chip junction to the air around the top of the package
θ_{JC}	K/W	Thermal resistance from the chip junction to the case, which is the metal slug on the bottom of the package
θ_{Solder}	K/W	Thermal resistance of the solder
$\theta_{\mathrm{Cu+Di}}$	K/W	Thermal resistance of the copper plating on the PCB and di-electric
θ_{ViaCu}	K/W	Thermal resistance of the copper plating of the via
θ_{Air}	K/W	Thermal resistance of the air in the PCB

1 Introduction

In a medium-sized manufacturing industry, productivity is largely determined by the tools used. Since these tools wear out over time, there is always a downtime due to maintenance or damage to machines and workpieces. Fluctuation ranges of +/- 25% are a normal case for tools, as a consequence up to 50% of the tool costs are wasted.

Due to constant progress in technology, manufacturing processes in industry can be continuously optimized. A key element here is the digital mapping of production processes and tools in real factories. So-called “Smart Objects” are required for this, which can communicate with higher-level databases. For example, with the help of RFID technology, tools can be provided with a necessary interface. With a unique identification number, the entire life cycle of the tool can be automatically monitored. This makes it possible to use tools sustainably, reduce machine downtimes and thus increase the efficiency of a company. Failures and damage to workpieces and machines are also possibly avoided.

In the area of automated machines, existing technologies reach their limits due to multipath propagation and the resulting interference. In order to drive digital change in factories, it is necessary to overcome these challenges. New RFID technologies in the SHF band for this application are being investigated and developed at Fraunhofer IMS.

1.1 Motivation

Integrated Circuit (IC) is often involved in RFID technology, because the electronic equipment in RFID systems are continuously being developed following the miniaturization trend. Besides, with the constant development of semiconductor technology according to Moore's Law, the density of integrated circuits becomes everlasting higher. All ICs generate heat during operation, and the accumulation of heat will inevitably lead to an increase in the junction temperature of the semiconductor. As the junction temperature increases, the performance of semiconductor components will decrease and even cause chip damage. Therefore, each chip manufacturer will specify the maximum junction temperature of its semiconductor components.

In ordinary digital circuits, due to the low power consumption of low-speed circuits, under normal heat dissipation conditions, the temperature rise of the chip will not be considerably large, so there is no need to consider the heat dissipation of the chip. However, in high-speed circuits, the power consumption of the chip is relatively large, and the heat dissipation under normal conditions can no longer ensure that the junction temperature of the chip does not exceed the allowable operating temperature. Consequently, it is necessary to consider the heat dissipation of the chip to make the chip work within normal temperature range. In most of Printed Circuit Boards (PCBs) which are available in the market, Flame Retardant-4 (FR-4) has been chosen as the predominant material for its low cost. However, FR-4 possesses significantly low thermal conductivity which contributes to the overall thermal resistance of the PCB. Besides that, the significant increase of thermal resistance will simultaneously delaminate the interfacial layer material attached to the PCB. This is very disastrous for RF PCB.

Thus, many companies are committed to finding better thermal conductivity materials for high-frequency PCB. Among them, the RO4000 series hydrocarbon ceramic laminates developed by Rogers Corporation have better thermal conductivity compared with FR-4 material. Besides, the temperature coefficient of dielectric constant is among the lowest of any circuit PCB material, and the dielectric constant is stable over a broad frequency range. This makes it a more ideal substrate for broadband applications. Therefore, RO4000 material owns the excellent properties needed

by designers of RF circuits, matching networks and controlled impedance transmission lines. [1]

1.2 Goal of the Bachelor Thesis

The goal of this bachelor thesis is to develop a PCB for an RF-power amplifier for RFID applications in the SHF band by using the simulation and design tools of the Keysight EEsof EDA software. The RF-power amplifier should be adapted at least for the frequency range from 5.725 to 5.875 GHz and achieve an output power of 33 dBm. For this purpose, the suitability of possible line types for signal transmission must be examined and adapted to the system. Since the power amplifier usually causes the greatest energy consumption of the front end and a large part is converted into thermal losses, measures must be taken to reduce the thermal load on the component so that a stable operation can be ensured, even over long periods. The layout should thus be examined and optimized for thermal properties of the PCB in simulations. After the prototype has been produced, the design is to be validated using measurement technology. For this purpose, IMS has suitable measuring technology and Infrared Radiation (IR) camera to measure the electrical parameters and the temperature distribution on the PCB. Subsequently, further components of a front end, such as modulators and demodulators, can be added successively. As a starting point, the chip “SE5004L” from Skyworks Inc. will be used. Since the SE5004L is a 5 GHz power amplifier offering high linear power for wireless LAN applications [2], it can be used for the application without large adjustments.

2 Theoretical Background

Introduced in this chapter are first the RFID technology and system, then two transmission lines that are often used in PCBs, some important parameters and formulas involved in this thesis and RF-power amplifier as well as the chip used in this thesis.

2.1 RFID Technology and System

RFID is an automatic wireless data collection and communication technology with a long history. With the development of the Internet of Things (IoT), RFID technology has become a core technology, that has been used widely. RFID can identify specific targets and read/write related data through radio signals without requiring mechanical or optical contact between the identification system and specific targets. Unlike the barcode, the RF transponder does not need to be within the line of sight of the reader, and it can also be embedded in the tracked object.

Many industries have used RFID technology. For example, by attaching the transponder to a car in production, the factory can easily track the progress of the car on the production line. The RFID identification card allows employees to enter the locked part of the building. Besides, the RF transponder on the car can also be used to collect toll roads and parking lots.

An RFID system is mainly made up of two components: the transponder, which is located on the object to be identified and the interrogator or reader, which may be

a read or write/read device. A reader typically contains an RF module (transmitter and receiver), a control unit and a coupling element to the transponder. It can detect and recognize the transponder through the Identity Document (ID) provided by the chip manufacturer. It may also use a decoder in order to read the information carried by the incident wave. In addition, many readers are fitted with an additional interface that enables them to forward the data received to another system (robot control system, etc.). The transponder, which represents the actual data-carrying device of an RFID system, normally consists of a coupling element and an electronic microchip. [3]

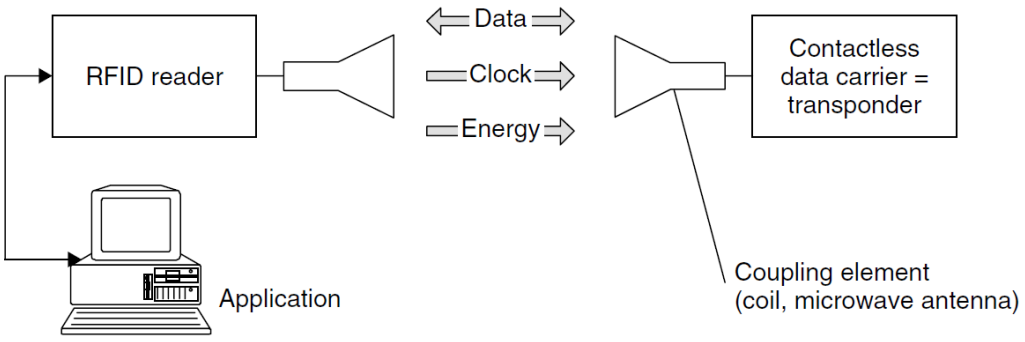


Figure 2-1 A simple and classic RFID system [3]

The simplest RFID transponder consists of two parts: an antenna for sending and receiving signals, and an RFID chip (or IC) that stores the transponder ID and other information. RFID transponders are roughly divided into two types.

One type are active transponders, where an embedded power source is used for operating transponders. For example, it may be a battery or a cell to enhance transponder performance and data transmission. Active transponders are mainly used for monitoring physical parameters (such as temperature, humidity, movement). [3]

The other type are passive transponders. Compared with active transponders, passive transponders do not include any embedded power source. As an alternative, the radiated wave from the reader is used as a power source for the chip. When the transponder receives an electric field from the reader, the energy is converted to an

Alternating Current (AC) voltage through the antenna of the transponder and then is rectified as Direct Current (DC) to power the chip. The energy activates the chip, which then modulates the energy with the desired information, and then backscatters a signal back towards the reader.

A common modulation type used in RFID system, is Amplitude Shift Keying (ASK) where the chip impedance switches between two states: one is matched to the antenna (chip collects power in this state) and the other one is strongly mismatched. [4] However, the passive transponders do not actively spread power. Therefore, a high output power of the reader is necessary so that the transponder can still be supplied with power from a distance.

2.2 Microstrip and Coplanar Waveguide (CPW)

Microstrip and CPW are two types of electrical planar transmission line which can be fabricated using PCB technology and is used to convey microwave-frequency signals.

Microstrip consists of a conducting track separated from a ground plane by a dielectric layer known as the substrate, as shown in Figure 2-2. Microstrip is much cheaper than traditional waveguides and being far lighter and more compact. However, compared with traditional waveguide, microstrip is the generally lower power handling capacity and higher losses. Since microstrip is not enclosed, it is also susceptible to crosstalk and accidental radiation.

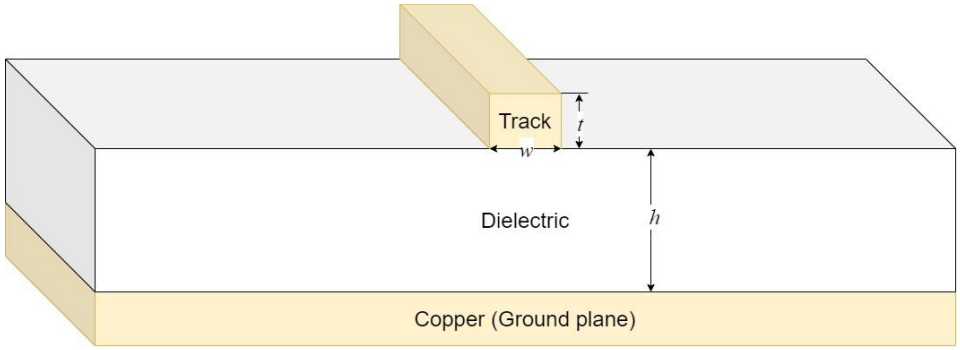


Figure 2-2 Model of Microstrip

The model of Microstrip is shown in Figure 2-2. w is the track width; t is the track thickness; h is the dielectric thickness. A closed-form approximate expression for the quasi-static characteristic impedance Z_0 of a microstrip line was proposed by Hammerstad [5]:

Effective width W and thickness H:

$$W = w + \frac{t}{\pi}\left[\ln\left(\frac{2h}{t}\right) + 1\right] \tag{2.1}$$

$$H = h - 2t \tag{2.2}$$

For $\frac{W}{H} < 1$:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12\frac{H}{W}}} + 0.04\left(1 - \frac{W}{H}\right)^2\right] \tag{2.3}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}}\ln\left(\frac{8H}{W} + \frac{W}{4H}\right)\ \Omega \tag{2.4}$$

For $\frac{W}{H} \geq 1$:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12\frac{H}{W}}} \tag{2.5}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W}{H} + 1.393 + \frac{2}{3}\ln\left(\frac{W}{H} + 1.444\right)\right]}\ \Omega \tag{2.6}$$

CPW usually contains a single conducting track printed onto a dielectric substrate, and a pair of return conductors on both sides of the track. These three conductors are on the same side of the substrate. Coplanar waveguide with lower

ground plane (CPWG) is a common variant of CPW in which the ground layer covers the backside of the substrate. The ground plane on the backside serves as a third return conductor. Compared with microstrip, CPW and CPWG can greatly increase the copper area on the surface of PCB, thereby improving the heat dissipation of PCB. The model of CPWG is shown in Figure 2-3. w is the track width; g is gap (spacing) between the track and ground plane; h is dielectric thickness.

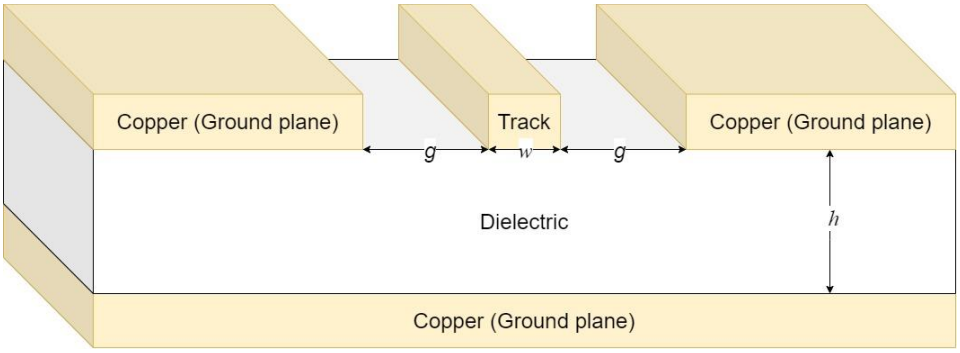


Figure 2-3 Model of CPWG

The characteristic impedance Z_0 of a CPWG is given as Equation (2.7) [6]:

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(kl)}{K(kl')}} \ \Omega \tag{2.7}$$

Where:

$$K(k) = F\left(\frac{\pi}{2}, k\right) = \int_0^{\frac{\pi}{2}} \frac{d\theta}{\sqrt{1 - k^2 \sin^2\theta}} \tag{2.8}$$

$$k = \frac{w}{w + g}, \qquad k' = \sqrt{1 - k^2} \tag{2.9}$$

$$kl = \frac{\tanh(\frac{\pi w}{4h})}{\tanh(\frac{\pi(w+g)}{4h})}, \qquad kl' = \sqrt{1-kl^2} \tag{2.10}$$

$$\varepsilon_{eff} = \frac{1 + \varepsilon_r \frac{K(k')}{K(k)} + \frac{K(kl)}{K(kl')}}{1 + \frac{K(k')}{K(k)} + \frac{K(kl)}{K(kl')}} \tag{2.11}$$

2.3 Scattering Parameters (S-parameters)

S-parameters represent the electrical properties of linear electrical components and networks in small-signal behavior with the help of wave quantities. The S-parameters are used in the dimensioning and calculation of input and output levels in the field of high-frequency technology and telecommunications systems.

In comparison to other parameter representations such as the Z- and Y-parameters, S-parameters use matched loads instead of open or short circuit conditions to characterize the linear network, because open and short terminations are difficult to achieve at high frequencies. Besides, power is much easier to be quantified than current and voltage in RF networks. Furthermore, S-parameters change with the measurement frequency, so frequency must be specified for any S-parameters measurements stated, as well as the characteristic impedance or system impedance. In practice, the S-parameters are measured as a function of frequency by network analyzer. The S-parameters are dimensionless complex numbers, which are specified by amount in decibels (dB) and phase in degrees (°).

The S-parameter matrix for the 2-port network is probably the most commonly used and serves as the basic building block for generating the higher order matrices for larger networks. [7]

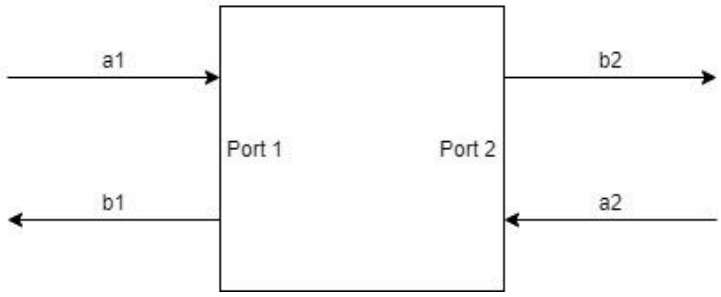


Figure 2-4 Incident and reflected power waves in a 2-port network

As shown in Figure 2-4, a_1 is the incident power wave of gate 1, a_2 is the incident power wave of gate 2. b_1 is the reflected power wave of gate 1, b_2 is the reflected power wave of gate 2. Then, the relationship between the incident, reflected power waves and the S-parameter matrix is given by:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.12}$$

1. the input port power reflection coefficient S_{11}

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \tag{2.13}$$

2. the output port power reflection coefficient S_{22}

$$S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0} \tag{2.14}$$

3. the forward power gain S_{21}

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} \tag{2.15}$$

4. the reverse power gain S_{12}

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} \tag{2.16}$$

2.4 Thermal Conductivity and Thermal Resistance

All materials conduct heat to some degree. Thermal conductivity is the standard measure of the ability of materials to conduct heat. Values of thermal conductivity κ are typically specified in unit of watts per meter kelvin ($\frac{\mathrm{W}}{\mathrm{m \cdot K}}$). When a temperature difference exists across a material, heat flows from high temperature areas to low temperature areas. This process is similar to an electric current flowing through a circuit from a higher potential to a lower potential. Thermal resistance is a material property and a measurement of a temperature difference by which an object or material resists a heat flow.

The thermal resistance R_t of the volume of that material is calculated as follows:

$$R_t = \frac{L}{\kappa \cdot A} \tag{2.17}$$

L is the length or thickness of the material in m.

κ is the thermal conductivity of the material in $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$.

A is the cross-sectional area in m^2.

Using the analogy that heat flow is equivalent to an electrical current flow, the temperature difference across a material with thermal resistance and a heat current flowing through it is as follows:

$$\Delta T = Q \cdot R_t \tag{2.18}$$

ΔT is the temperature difference across the material in K or °C.

Q is the heat current in W.

R_t is the thermal resistance of the material in $\frac{\mathrm{K}}{\mathrm{W}}$ or $\frac{^{\circ}\mathrm{C}}{\mathrm{W}}$.

2.5 RF Power Amplifier and SE5004L

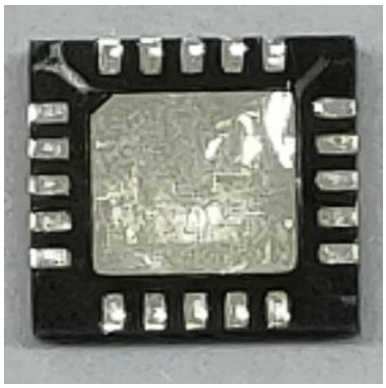
An RF-power amplifier is a type of electronic amplifier that converts a low-power RF signal into a higher power signal. Typically, RF-power amplifiers drive the antenna of

a transmitter. The basic principle of the power amplifier is that the DC power drawn from the power supply is converted into an AC voltage signal delivered to the load. Design goals of an RF-power amplifier usually include gain, power output, bandwidth, input and output impedance matching, and heat dissipation.

The chip SE5004L involved in this thesis is a kind of RF-power amplifier. It features an integrated power detector for closed loop monitoring and the control of the output power. For wireless LAN applications, the device delivers approximately 26 dBm of linear output power at 5 V supply voltage. 2.85 V reference voltage is all that is required to enable or disable the power amplifier. [2]

In Figure 2-5 are the physical pictures and pin diagram of the chip. The absolute maximum ratings of parameters of the chip are shown in Table 2-1.

a) *b)*



c)

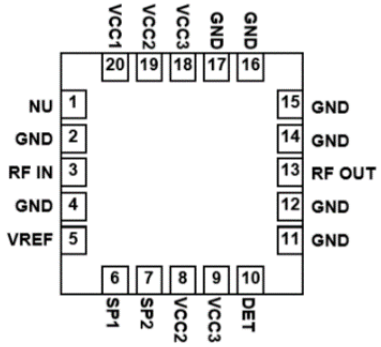


Figure 2-5 The physical pictures *a)* top view *b)* bottom view and *c)* pin diagram [2] of the chip

Symbol	Definition	Minimum	Maximum	Unit
$V_{CC1}/V_{CC2}/V_{CC3}$	Supply voltage on pin V_{CC1},V_{CC2}, V_{CC3}	-0.3	+6	V
V_{REF}	Power amplifier enable and reference voltage	-0.3	+3.6	V
RF IN	RF Input Power	-	6	dBm
T_j	Maximum junction temperature	-	160	°C

Table 2-1 The absolute maximum ratings of parameters of the chip [2]

3 Simulation and Analysis

In this chapter, a basic PCB designed for the RF-power amplifier will be introduced first. Then, based on the results of its thermal simulation and a simple modeling of two-layer PCB, some cost-effective solutions are analyzed and designed to optimize heat dissipation. Finally, these solutions are compared through thermal simulation.

3.1 Basic PCB of the RF Power Amplifier

The important electrical characteristics of the chip SE5004L in the wireless LAN application are given from the data sheet, as shown in Table 3-1.

Symbol	Definition	Minimum	Typical	Maximum	Unit
f	Frequency range	5.15	-	5.85	GHz
$P_{1\mathrm{dB}}$	Output 1dB compression point	30	34	-	dBm
S_{21}	Gain	30	32	-	dB
I_{CC}	Supply current	-	600	800	mA

Table 3-1 The important electrical characteristics of the chip SE5004L in the wireless LAN application [2]

Through the data analysis in Table 3-1, it can be determined that, the power amplifier basically satisfies the requirements of the application in this thesis. Although the highest frequency (5.85 GHz) is slightly lower than the required frequency (5.875GHz), the frequency range can be enlarged or moved through proper matching.

Therefore, the transmission line should be designed according to the material characteristics and frequency requirements. The material chosen here is RO4003C with the thickness of 813 µm, because it is quickly available from IMS. In addition, CPWG is more suitable than Microstrip for the RF-power amplifiers because of excellent stability and low loss in the SHF band. With the help of “LineCalc” tool in Advanced Design System (ADS) software, the parameters of CPWG can be easily calculated. Figure 3-1 is an example of using “LineCalc” tool in ADS software to calculate the parameter of CPWG.

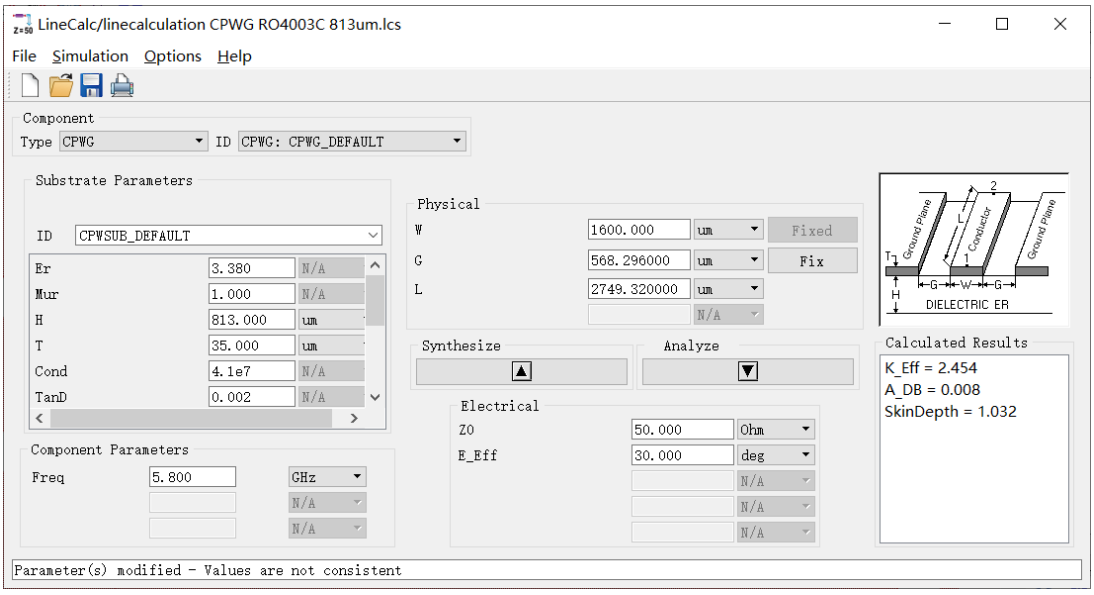


Figure 3-1 Example for using “LineCalc” tool in ADS software

During the internship at IMS, through the above parameters of CPWG, some PCBs have been designed and manufactured to study the circuit. According to the measurement as well as the research and analysis during the internship, the PCB layout and physical pictures shown in Figure 3-2, has the best electrical characteristics.

The specific measurement circuit of S-parameters will be introduced in Section 4.2. The measurement result of S-parameters of the PCB with “30 dB” attenuator is shown in Figure 3-3. The analysis of the result will be introduced in Section 5.1.1.

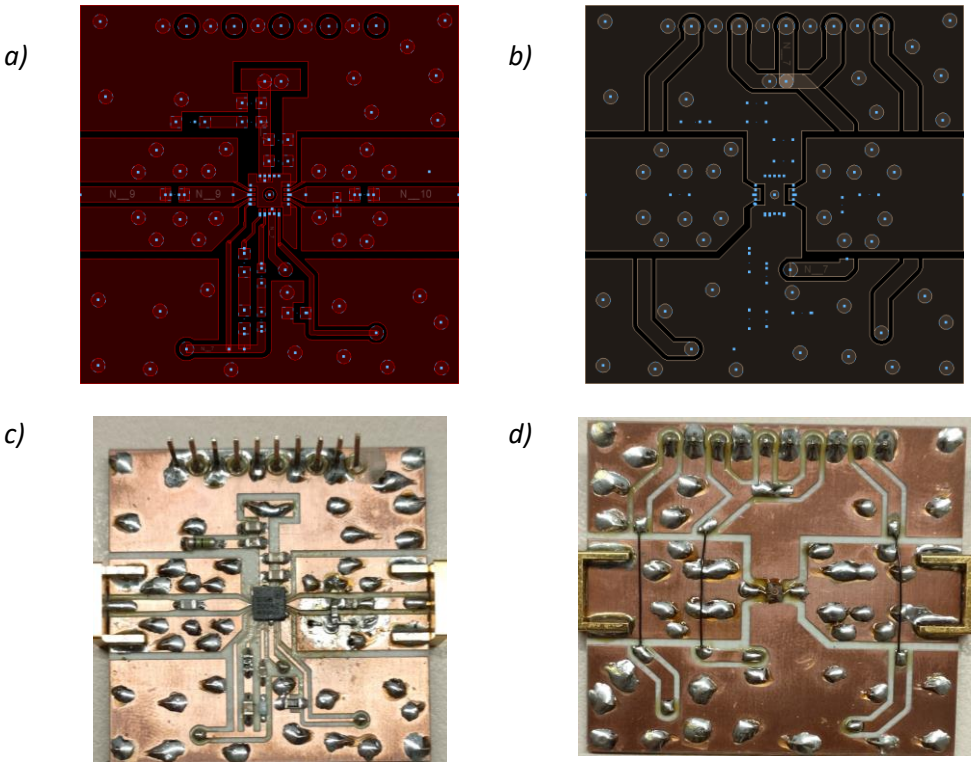


Figure 3-2 The layout *a)* top layer *b)* bottom layer and physical pictures *c)* top view *d)* bottom view of the basic PCB

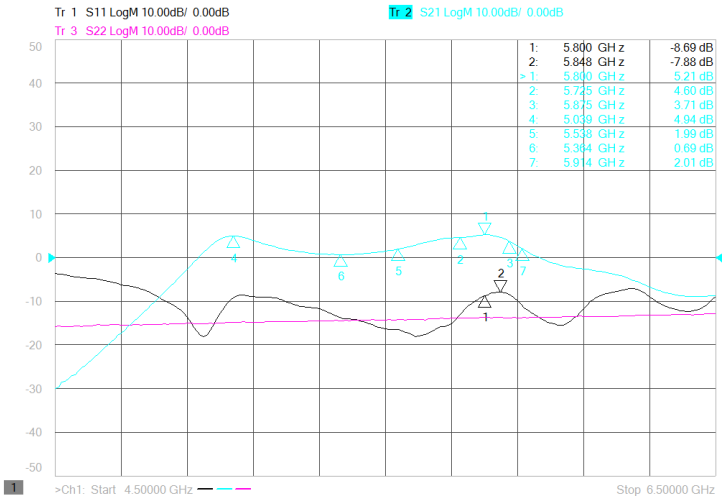


Figure 3-3 Measurement result of S-parameters of the basic PCB with “30 dB” attenuator

3.2 Thermal Simulation of the Basic PCB

With the help of “SIPro/PIPro” function in ADS software, the thermal properties of the chip and the entire PCB can be roughly simulated. According to the layout of the basic PCB, the thermal model can be established in “SIPro/PIPro”, as shown in Figure 3-4.

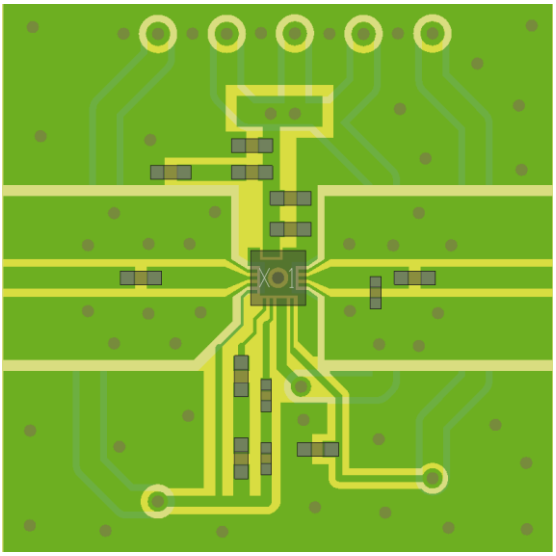


Figure 3-2 Thermal model of the basic PCB in “SIPro/PIPro”

In order to do the thermal simulation, the approximate heat dissipation of the chip needs to be determined. It is assumed that the output power of power amplifier is 33 dBm the same as the requirement. In addition, the DC power supply voltage of the chip is 5 V, and the current is assumed to be 800 mA. Therefore, the input power P_{input} and the output power P_{output} of the chip are:

$$P_{\text{input}} = U \cdot I = 5\ \text{V} \cdot 800\ \text{mA} = 4\ \text{W} \tag{3.1}$$

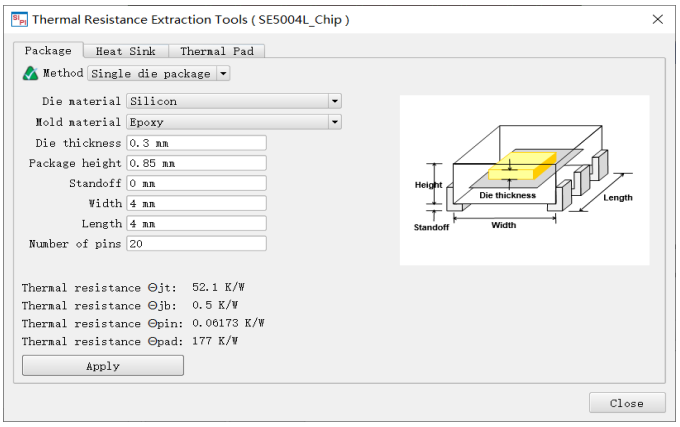
$$P_{\text{output}} = 33\ \text{dBm} \approx 2\ \text{W} \tag{3.2}$$

The approximate heat dissipation P_{heat} of the chip can be calculated as:

$$P_{\text{heat}} \approx P_{\text{input}} - P_{\text{output}} = 4\ \text{W} - 2\ \text{W} = 2\ \text{W} \tag{3.3}$$

According to chip size parameters, the thermal resistance of the chip can be calculated by “Thermal Resistance Extraction Tools” in “SIPro/PIPro”. Through “Thermal Resistance Editor”, the calculated thermal resistance can be applied to the chip model. “Thermal Resistance Extraction Tools” and “Thermal Resistance Editor” are shown in Figure 3-5.

a)



b)

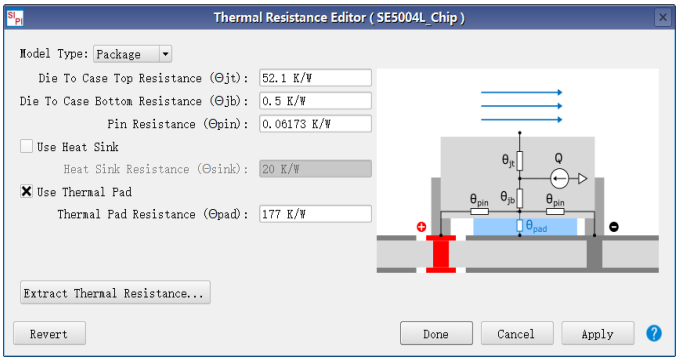


Figure 3-3 *a)* “Thermal Resistance Extraction Tools” and *b)* “Thermal Resistance Editor”

After the thermal model of the basic PCB is completely established and the heat dissipation as well as thermal resistance of the chip are determined, the thermal simulation of the PCB is run. The thermal simulation results of the basic PCB are shown in Figure 3-6.

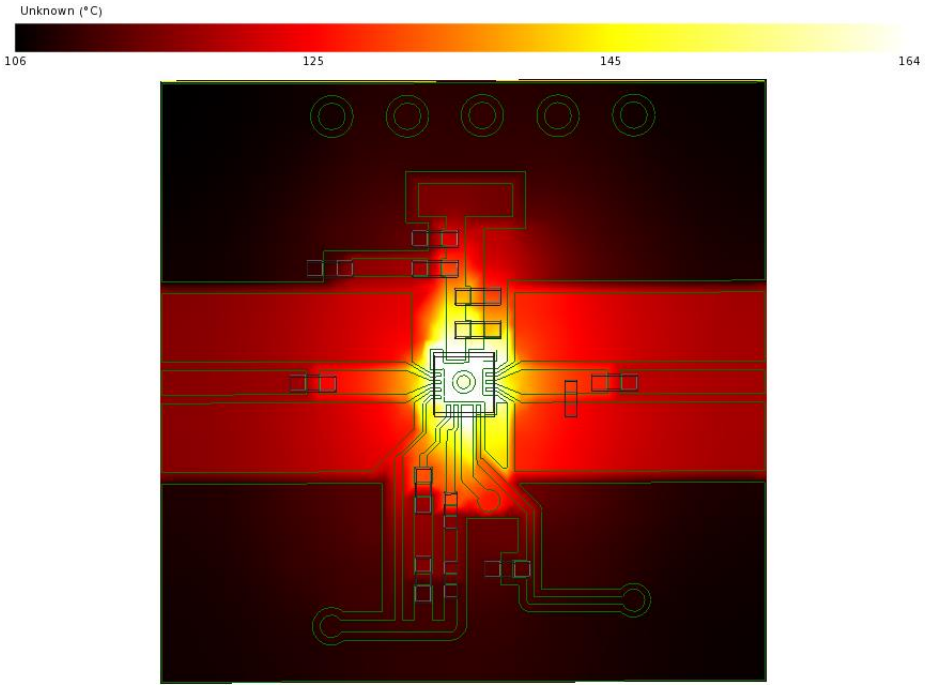


Figure 3-4 Temperature distribution on the PCB

From the thermal simulation result, under the assumption that the heat dissipation of the chip is 2 W, the maximum temperature on the basic PCB is 164 °C. It exceeds the maximum junction temperature 160 °C specified in the data sheet, so it is very catastrophic for the chip. The chip cannot work normally on the basic PCB and will lead to malfunction or even destruction soon.

Therefore, it is necessary to improve the thermal properties on the basis of the basic PCB. Since it can be seen from Figure 3-6 that the heat on the basic PCB cannot be conducted well due to the separate copper ground planes, it is necessary to connect separate ground copper layers together to make heat conduction better.

In addition, PCB should be thermally analyzed. After that, several different solutions should be designed according to the analysis results to improve the thermal properties of PCB.

3.3 Thermal Analysis of PCB

First of all, the thermal conductivity of the three materials that are involved in the basic PCB should be analyzed.

Material	Copper	Air	RO4003C
Thermal conductivity	$395\ \frac{\mathrm{W}}{\mathrm{m{\cdot}K}}$	$0.0297\ \frac{\mathrm{W}}{\mathrm{m{\cdot}K}}$	$0.71\ \frac{\mathrm{W}}{\mathrm{m{\cdot}K}}$

Table 3-2 Thermal conductivity of copper, air [8] and RO4003C [1] at 80 °C

From Table 3-2, it can be easily found that the thermal conductivity of copper is much higher than that of dielectric material RO4003C and air. Therefore, to improve the thermal properties of the PCB without adding other components like heatsink, it is very important to consider the thickness and area of the copper plating on the PCB.

Firstly, increasing the thickness of the copper plating on the PCB can reduce the thermal resistance in the horizontal direction of the PCB to a certain extent. However, the two-layer PCB currently considered is very thin, so the recommended thickness of copper plating on the PCB is usually 1 ounce (oz.), i.e., 35 µm. If the thickness of copper is increased to, say 2 oz., i.e., 70 µm, it will not only be difficult in the production process, but also increase the production cost.

Therefore, the area of the copper plating on the PCB should be mainly considered here. Since CPWG has been used in the basic design, the copper area has been greatly increased, so it is difficult to make big improvement on the basic design. Consequently, it needs to be considered from the area of the PCB.

Not only that, the number of copper layers of the PCB can also be increased, such as four copper layers. By this way, the total copper area is increased, so that the heat dissipation of the PCB is improved.

In addition, it can also be analyzed from the thermal resistance in the vertical direction of the PCB to improve heat dissipation. The thermal resistance of the PCB is complex and often nonlinear with temperature. Therefore, the thermal model of

the PCB is developed by using finite element analysis. In Figure 3-7 *a)* is a simple thermal model of two-layer PCB. The corresponding equivalent circuit to analyze thermal resistance in the vertical direction of the PCB is shown in Figure 3-7 *b)*.

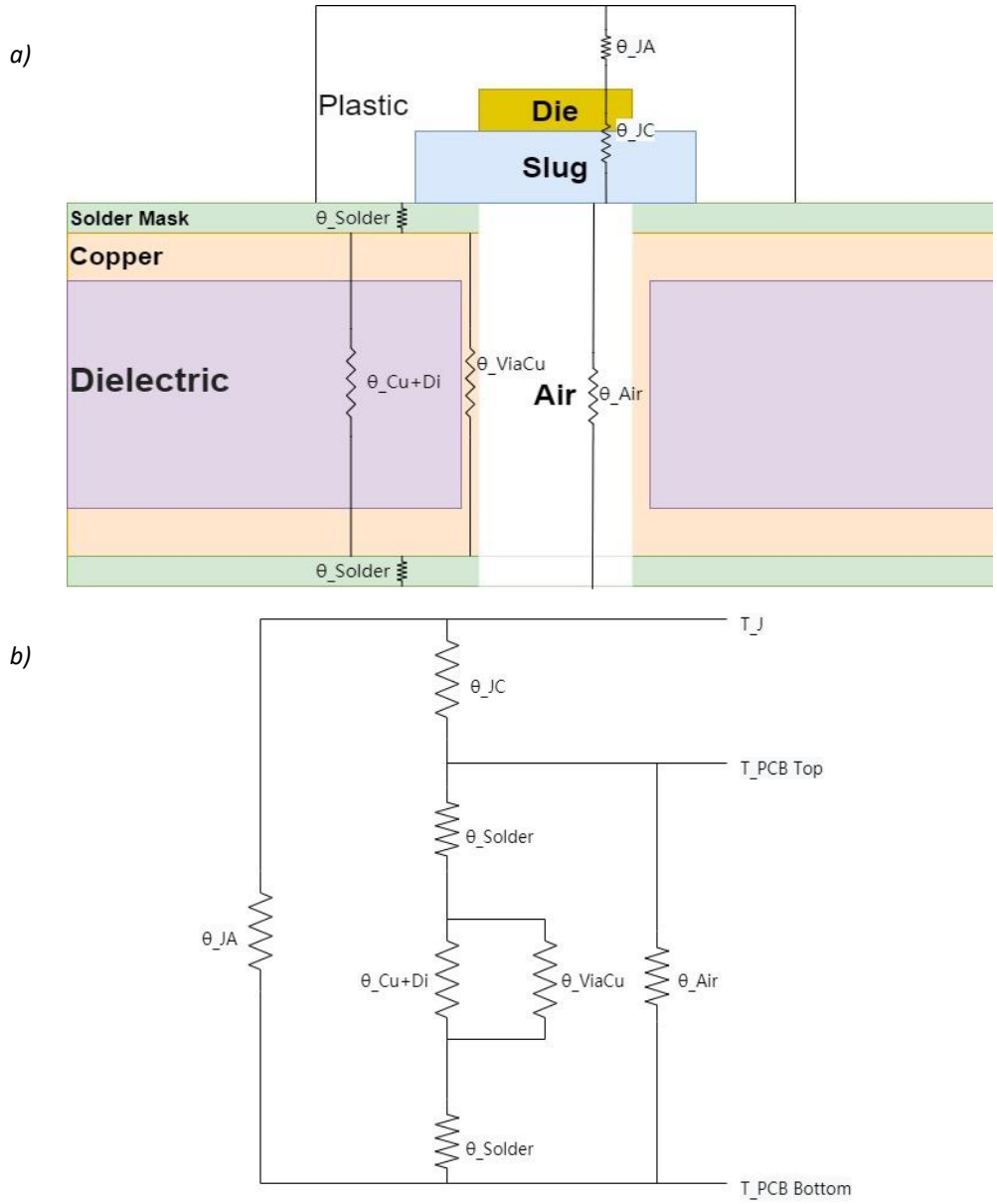


Figure 3-5 *a)* A Simple thermal model and *b)* equivalent circuit of two-layer PCB

The definitions of each symbol in Figure 3-7 are as follows:

θ_{JA} is the thermal resistance from the chip junction to the air around the top of the package.

θ_{JC} is the thermal resistance from the chip junction to the case, which is the metal slug on the bottom of the package.

θ_{Solder} is the thermal resistance of the solder.

$\theta_{\mathrm{Cu+Di}}$ is the thermal resistance of the copper plating on the PCB and dielectric.

θ_{ViaCu} is the thermal resistance of the copper plating of the via.

θ_{Air} is the thermal resistance of the air in the PCB.

Among them, θ_{JA} and θ_{JC} are system parameters, in other words, they cannot be changed without changing the chip. θ_{Solder} is determined by the manufacturer's material, which is usually fixed and its effect on heat dissipation of the PCB is relatively small. Additionally, by comparing the thermal conductivity of materials, the thermal conductivity of air is much smaller than that of dielectric and copper. Therefore, the heat dissipated by the air in Via can be ignored in comparison. Conversely, $\theta_{\mathrm{Cu+Di}}$ and θ_{ViaCu} are of great significance for improving the thermal resistance in the vertical direction of the PCB.

Firstly, according to Equation (2.6), the thermal resistance in the vertical direction of the PCB can be reduced by reducing the thickness of the dielectric, namely reducing the thickness of the PCB.

Besides, there are many vias that are equivalently connected in parallel in the PCB. Therefore, the thermal resistance in the vertical direction of the PCB can also be reduced by increasing the density of vias. In addition, increasing the thickness of copper plated through vias can also reduce the thermal resistance. However, the thickness of copper plated through vias is usually determined by the production process. Hence, the thickness of the PCB and the density of vias are of more comparative significance in simulation and in practice.

Of course, there are also other options, such as insulated metal substrate circuit boards and active cooling. However, in practice the production costs must be taken into consideration. Thus, it is more cost-effective to consider from the area and thickness of the PCB, the density of vias and four-layer structure to reduce the thermal resistance of the PCB.

3.4 Different Designs of PCB

According to the previous analysis, it is necessary to design different PCBs in the simulation to compare the effect of each of the four aspects on improving heat dissipation of the PCB.

3.4.1 The Thickness of PCB

First of all, it is considered to improve heat dissipation by reducing the thickness of the PCB, namely the thickness of the dielectric.

On the basic design, the thickness of the dielectric is 813 µm. According to the material thickness that the manufacturer has provided, the thinner 508 µm can be chosen. Although there are thinner than 508 µm materials to choose from, the thinner the material, the easier it is to bend or even break. In order to consider the stability of the PCB in the actual situation, only these two thicknesses of the dielectric, namely 813 µm and 508 µm, are considered here for the two-layer PCB structure.

Because the thickness of the dielectric is changed, CPWG needs to be recalculated and designed. In the same way, the new parameters of CPWG can also be obtained according to “LineCalc” tool. Figure 3-8 shows two substrates with different thicknesses of the dielectric.

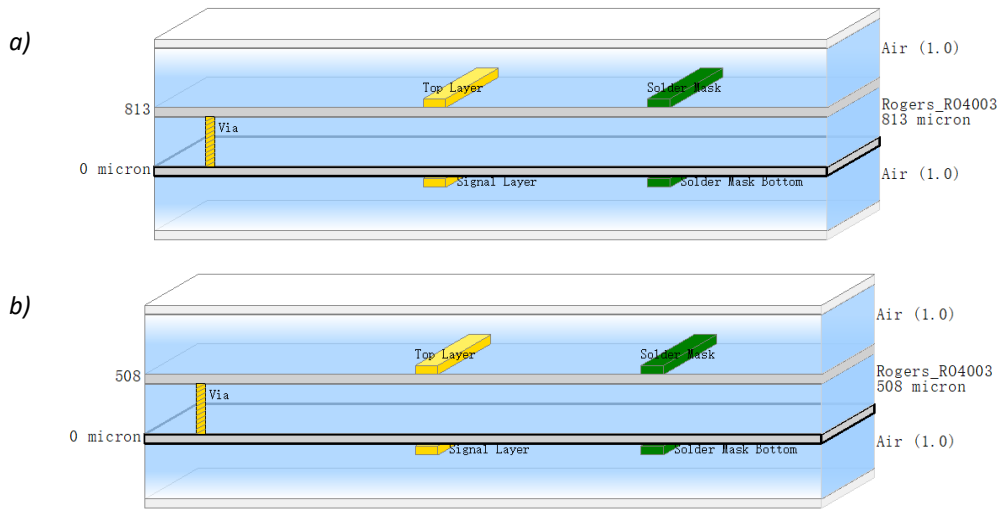


Figure 3-6 Two substrates with *a)* 813um and *b)* 508um dielectric

3.4.2 The Area of PCB

Secondly, it is considered to improve heat dissipation by increasing the area of the PCB.

The area of the basic design is 4 cm×4 cm. Therefore, the area of the PCB can be increased to 5 cm×5 cm and 6 cm×6 cm. Figure 3-9 shows the top layer of three PCBs with different area.

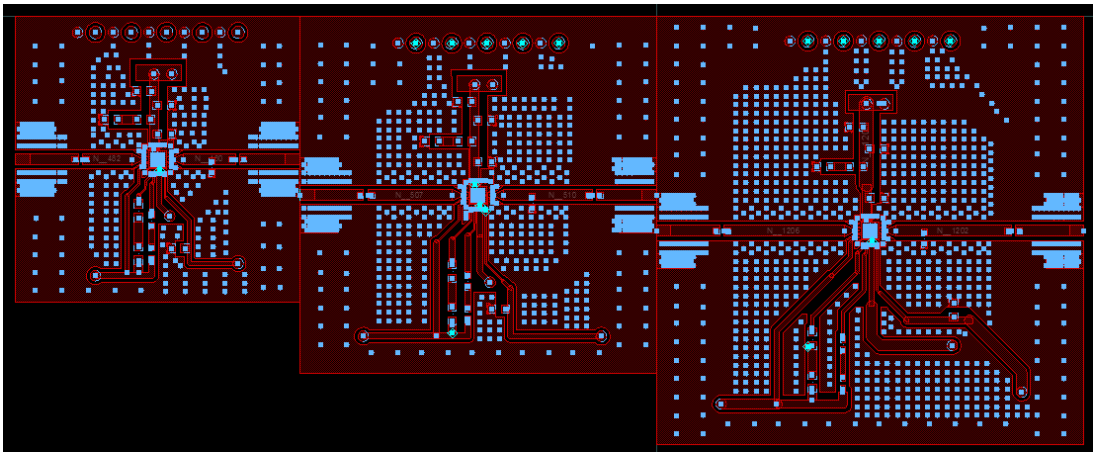


Figure 3-7 Top layer of PCBs with different area of 4 cm×4 cm, 5 cm×5 cm and 6 cm×6 cm

3.4.3 The density of vias around the chip

Thirdly, it is considered to improve heat dissipation by increasing the density of the vias around the chip.

Since the vias in the PCB are equivalently connected in parallel, increasing the density of vias can effectively reduce the equivalent thermal resistance in the vertical direction. The increasing number of vias will result in decreasing thermal resistance [9]. Therefore, it is necessary to place more vias than in the basic PCB under or around the chip, which is the biggest heat source on the PCB. As the density of vias increases, the via-to-via spacing is naturally decreased. Thus, the via-to-via spacing should be designed possibly small [10]. Considering technical limitations of the manufacturer, two types of via-to-via spacing around the chip are designed, as shown in

Figure 3-10. The diameter of the vias is all 300 µm, which is the standard via size of the manufacturer for HF PCB.

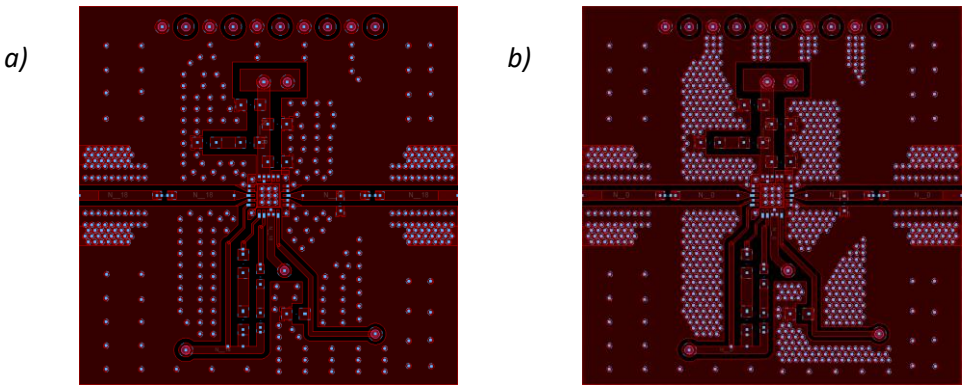


Figure 3-8 Top layer of *a)* 900 µm and *b)* 400 µm via-to-via spacing around the chip

3.4.4 Four-layer Structure

Lastly, it is considered to improve heat dissipation from the layer structure.

The basic design is a two-layer structure, namely two copper layers. Therefore, the four-layer PCB can also be designed to increase the number of copper layers, so that the heat dissipation of the PCB is improved. As shown in Figure 3-11, in the substate, the four copper layers are all of 35 µm, and three dielectric layers are all of 508 µm. The second and fourth copper layers are ground planes. Since the thickness of the first dielectric layer is of 508 µm, the parameters of the CPWG of the four-layer PCB is the same as the parameters of the two-layer PCB with 508 µm dielectric.

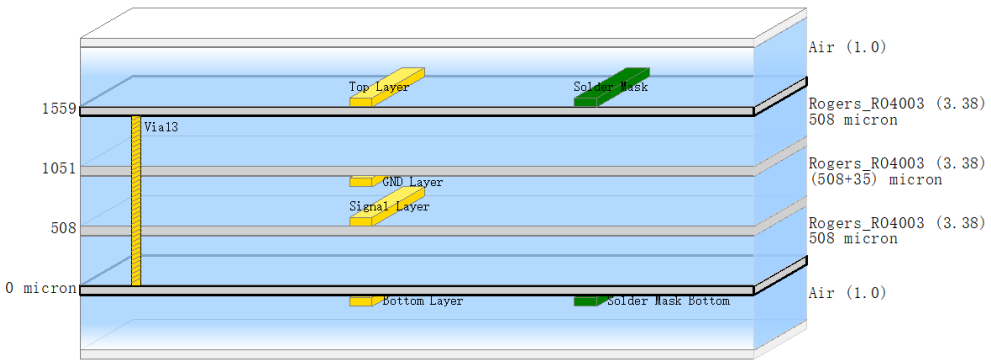


Figure 3-9 Substrate of four-layer PCB

3.5 Thermal Simulation of Different Designs

According to the previous analysis and design, considering from four different aspects, there are totally 18 different PCB designs in ADS software for comparison. Similar to the thermal simulation of basic PCB in chapter 3.2, the thermal model of each PCB in “SIPro/PIPro” is established and simulated.

3.5.1 Results of Thermal Simulation

After thermal simulation, the maximum temperature on each PCB is summarized in Table 3-3 below for comparison. The temperature distribution on each PCB will be shown in Figure A-1, A-2 and A-3 in Appendix.

Area of PCB	Via-to-via spacing	Two-layer		Four-layer
		813 µm dielectric	508 µm dielectric	
4 cm×4 cm	900 µm	145 °C	141 °C	124 °C
	400 µm	140 °C	136 °C	119 °C
5 cm×5 cm	900 µm	109 °C	106 °C	89.4 °C
	400 µm	99.6 °C	97.4 °C	82.8 °C
6 cm×6 cm	900 µm	89.4 °C	87.0 °C	71.9 °C
	400 µm	80.2 °C	79.2 °C	67.1 °C

Table 3-3 The maximum temperature on different PCBs in thermal simulation

3.5.2 Comparison and Evaluation of Thermal Simulation Results

According to the simulation results in Table 3-3, the effect of each of four aspects on maximum temperature on the PCB can be compared thoroughly.

Firstly, the effect of the thickness and the four-layer structure of the PCB can be compared with each other. Comparing the data horizontally, it is known that when the area of PCB and the via-to-via spacing are the same, the maximum temperature is the highest on the PCB with 813 µm dielectric and the lowest on the PCB with the four-layer structure. The maximum temperature on the PCB has a relatively nuance between the dielectric thickness of 813 and 508 µm. For example, when the area is 4 cm×4 cm and the via-to-via spacing is 900 µm, the difference is 4 °C. However, the maximum temperature on the PCB has a relatively large difference between the two-layer structure and the four-layer structure. For example, when the area is 4 cm×4 cm and the via-to-via spacing is 900 µm, the difference between the two-layer structure with 508 µm and the four-layer structure is 17.0 °C. Besides, these differences become smaller when the via-to-via spacing becomes smaller or/and the area becomes larger. For example, when the area is 6 cm×6 cm and the via-to-via spacing is 400 µm, the difference of the maximum temperature on the PCB between the dielectric thickness of 813 and 508 µm is only 1.0 °C; the difference between the two-layer structure with 508 µm and four-layer structure is 12.1 °C. In conclusion, as analyzed in Section 3.3, when the dielectric thickness is reduced from 813 to 508 µm, the thermal resistance of the PCB is improved, so that the heat dissipation is increased. In addition, using the four-layer structure can better optimize heat dissipation of the PCB.

Secondly, the effect of two via-to-via spacing around the chip can be compared. From the data in Table 3-3, it can be seen that when the area is 4 cm×4 cm and the dielectric thickness as well as the structure are the same, the maximum temperature of 400 µm via-to-via spacing around the chip is 5 °C lower than that of 900 µm via-to-via spacing. However, when the area is 5 cm×5 cm or 6 cm×6 cm, the difference will be larger. For example, when the area is 5 cm×5 cm (or 6 cm×6 cm) and the dielectric thickness is 813 µm, the difference is 9.4 °C (or 9.2 °C). Besides, when the dielectric thickness is changed from 813 to 508 µm or/and the structure is changed

from two-layer to four-layer, the difference becomes smaller. In conclusion, as analyzed in Section 3.3, when the via-to-via spacing around the chip is reduced from 900 to 400 μm, the thermal resistance of the PCB is improved, so that the heat dissipation is increased. Although more vias in the PCB can better conduct heat from the top layer to the bottom layer of the PCB, the heat conducted from the both layers to air is limited by the area. Therefore, when area of the PCB is 4 cm×4 cm, the effect of reducing the via-to-via spacing around the chip, namely increasing the number of vias, is not as good as 5 cm×5 cm and 6 cm×6 cm.

Lastly, the effect of the area of the PCB can be compared. By comparing the data longitudinally, it can be seen that when the other aspects are the same, the maximum temperature decreases greatly as the area of the PCB increases. When the area changes from 4 cm×4 cm to 5 cm×5 cm, the difference of the maximum temperature is approximately 35 °C. However, when the area changes from 5 cm×5 cm to 6 cm×6 cm, the difference of the maximum temperature is only approximately 18 °C. From Equation (2.17), it can be seen that thermal resistance is an inversely proportional function of area. Therefore, as the area increases, the improvement effect of thermal resistance decreases. In conclusion, as analyzed in Section 3.3, when the area of the PCB is increased, the thermal resistance of the PCB is improved, so that the heat dissipation is increased. In addition, according to the maximal junction temperature of the chip, the PCB with area 4 cm×4 cm may be able to meet the requirements. Obviously, if the area of PCB is larger, the temperature safety margin is higher.

In summary, the simulation results are basically consistent with the previous analysis of the effect of the four aspects. Although there are some inaccuracies in the simulation, such as the inability to accurately determine the heat dissipation of the chip, and the lack of some parameters of chip package, so that it is difficult to accurately calculate the specific thermal resistance of the chip, etc., these results still largely reflect the difference in heat dissipation between the various designs and can provide a reference value for subsequent production and measurements.

4 Production and Measurements

In this chapter, the production of PCBs will be introduced at first. Then, the performance of the PCBs, which is divided into electrical characteristics and thermal properties, will be measured. The measurement circuits and measurement procedures will be introduced separately.

4.1 Production

Through the previous analysis and simulation, the effect of each of four aspects on the heat dissipation of the PCB can be roughly determined. It is then necessary to produce and measure the actual PCB for verification and evaluation of the electrical characteristics and thermal properties.

After the comparison of prices and production processes, the selected manufacturer is “LeitOn”. It is impossible and unnecessary for all previous designs to be produced because of production costs. Therefore, only several typical designs with comparative significance should be produced. Since the production cost of the PCB of four-layer structure is much more expensive than that of the PCB of two-layer structure, the PCB designs with two-layer structure are mainly considered to be produced. Besides, since this PCB needs to be installed in the overall structure of the front end of the reader in the RFID system, the area of the PCB needs to be relatively small, so the PCB with the area of 4 cm×4 cm is mainly considered.

In summary, the following PCB designs are finally produced. In the following, 2L (or 4L) represents two-layer structure (or four-layer structure); 8D (or 5D) represents 813 µm dielectric (or 508 µm dielectric); 4A represents area of 4 cm×4 cm; 9S (or 4S) represents 900 µm via-to-via spacing (or 900 µm via-to-via spacing).

1. Two-layer structure with 813 µm dielectric, 4 cm×4 cm area and 900 µm via-to-via spacing around the chip (2L8D4A9S)
2. Two-layer structure with 813 µm dielectric, 4 cm×4 cm area and 400 µm via-to-via spacing around the chip (2L8D4A4S)
3. Two-layer structure with 508 µm dielectric, 4 cm×4 cm area and 900 µm via-to-via spacing around the chip (2L5D4A9S)
4. Two-layer structure with 508 µm dielectric, 4 cm×4 cm area and 400 µm via-to-via spacing around the chip (2L5D4A4S)
5. Four-layer structure with 4 cm×4 cm area and 400 µm via-to-via spacing around the chip (4L4A4S)

Another two PCBs (the PCB of two-layer structure with 813 µm dielectric, 5 cm×5 cm area and 400 µm via-to-via spacing around the chip and the PCB of two-layer structure with 813 µm dielectric, 6 cm×6 cm area and 400 µm via-to-via spacing around the chip) are also selected for production to compare the effect of the PCB area. However, since these two PCBs cannot arrive in time, they cannot be measured before the submission of the thesis.

After the PCB is milled from the manufacturer, it is further processed in IMS, such as soldering components, pin header and Subminiature version A (SMA) connector.

When the above processes are completed, the next step is the measurement phase of the PCBs, which is divided into the measurement of electrical characteristics and thermal properties. These two measurement processes will be introduced in detail in chapters 4.2 and 4.3 respectively.

4.2 Measurement of Electrical Characteristics

In this section, the measurement circuit and the measurement procedures of electrical characteristics of the PCB will be introduced.

4.2.1 Measurement Circuit of Electrical Characteristics

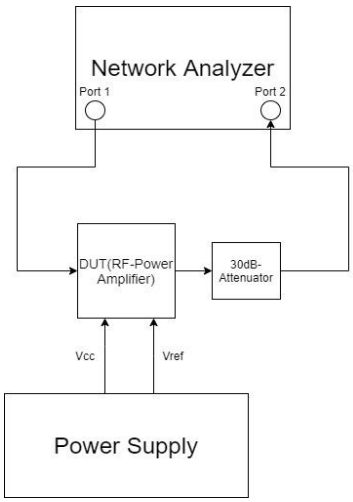
The electrical characteristics of power amplifier are mainly represented by its S-parameters, as described in Section 2.3. In order to obtain the S-parameters of the power amplifier, network analyzer is of necessity.

In addition, the power amplifier needs DC power to amplify the RF signal. Thus, DC power supply is also required.

With the purpose of preventing the output signal of power amplifier from damaging the Network Analyzer, a “30 dB” attenuator is added after the power amplifier to reduce the output power.

The schematic and physical diagram of the measurement circuit of electrical characteristics are shown in Figure 4-1.

a)



b)

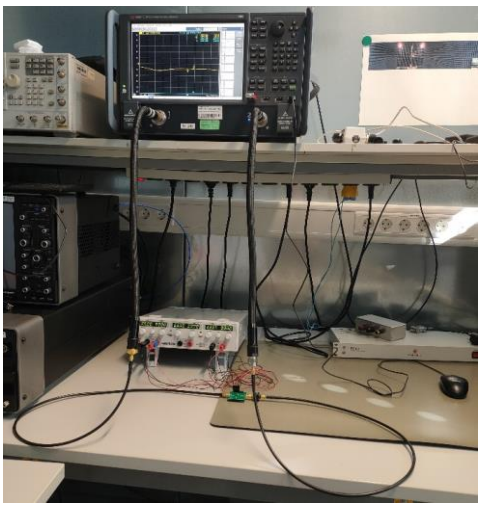


Figure 4-1 *a)* Schematic and *b)* physical diagram of measurement circuit of electrical characteristics

4.2.2 Measurement of the “30 dB” Attenuator

Before measuring, the network analyzer and wire need to be calibrated with the aid of “Electronic Calibration Module”. After calibration, the “30 dB” attenuator is connected to the measurement circuit. Since the interface between the “30 dB” attenuator and the wire needs to be connected by an adapter, it is also necessary to measure the S-parameters of the adapter separately, as shown in Figure 4-2.

a) *b)*

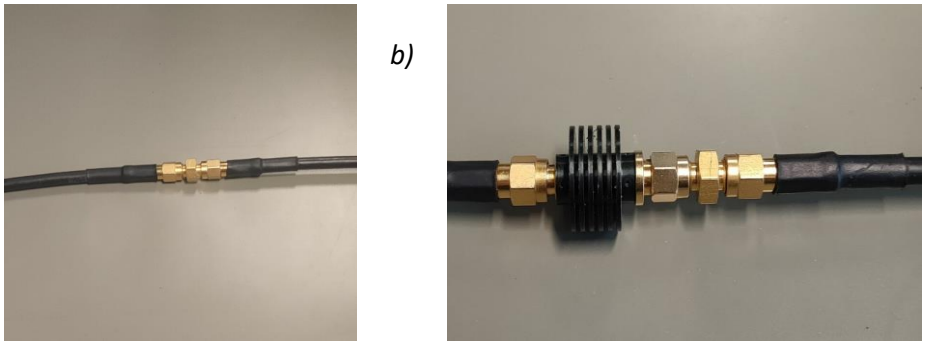


Figure 4-2 Measurement of *a)* the adapter and *b)* the “30 dB” attenuator with adapter

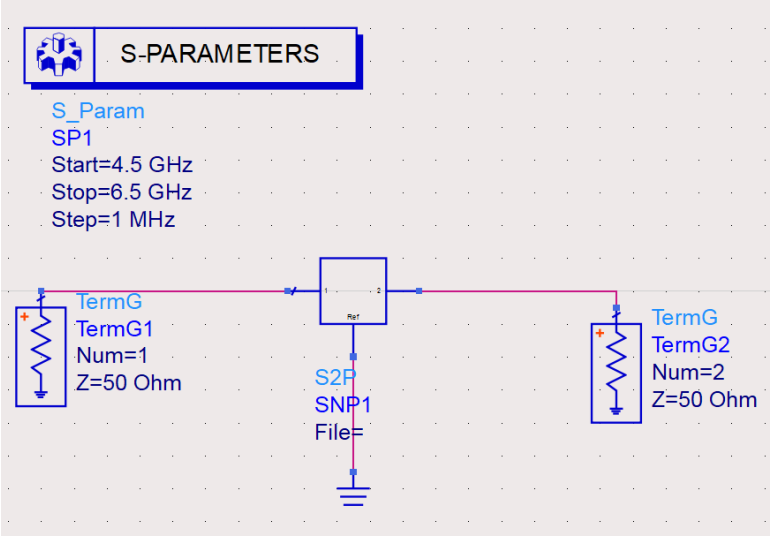


Figure 4-3 Schematic diagram for displaying the S-parameters in ADS software

After the measurement is completed, the result is saved in the form of “s2p” file. This allows the results to be displayed and analyzed in ADS software later. Figure 4-3

is the schematic diagram for displaying the measurement results of S-parameters in ADS software.

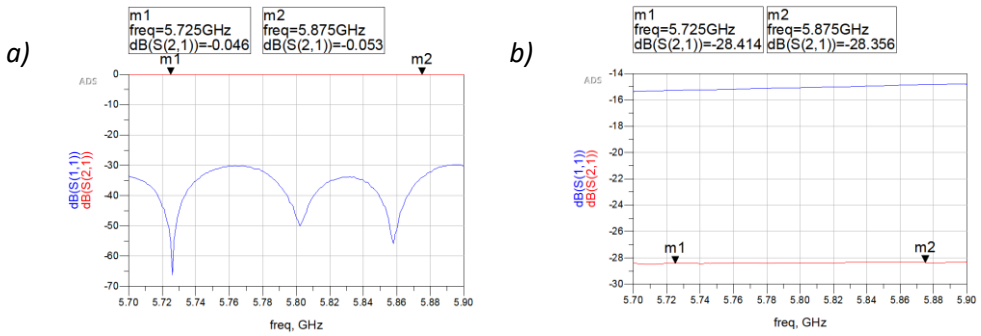


Figure 4-4 S-parameters of *a)* adapter and *b)* "30 dB" attenuator with adapter

The S-parameters of adapter and "30 dB" attenuator with adapter are shown in Figure 4-4.

It can be concluded from Figure 4-4 that in the frequency range from 5.725 to 5.875 GHz, S_{21} can be roughly regarded as linear. Because the value changes very little, the average value can be used to represent the S_{21}, namely the attenuation, in the frequency range from 5.725 to 5.875 GHz.

$$A_{\text{adapter}} = \frac{0.046\ \text{dB} + 0.053\ \text{dB}}{2} \approx 0.050\ \text{dB} \tag{4.1}$$

$$A_{\text{attenuator}} + A_{\text{adapter}} = \frac{28.414\ \text{dB} + 28.356\ \text{dB}}{2} = 28.385\ \text{dB} \tag{4.2}$$

$$A_{\text{attenuator}} = 28.385\ \text{dB} - 0.050\ \text{dB} = 28.335\ \text{dB} \tag{4.3}$$

According to Equation (4.1), (4.2) and (4.3), in the frequency range from 5.725 to 5.875 GHz, the attenuation of "30 dB" attenuator can be regarded as -28.335 dB, and the attenuation of adapter can be regarded as -0.050 dB.

4.2.3 Measurement of S-parameters

After calibration of the network analyzer and wire, the PCBs are connected in the measurement circuit separately, as shown in Figure 4-1 *b)*. According to the data sheet of the chip introduced before, the voltage V_{CC1}, V_{CC2} and V_{CC3} should be 5 V. Besides, the voltage V_{REF} should be 2.85 V. The input power from network analyzer is set to 0 dBm. Then, the S-parameters of the power amplifiers can be measured by network analyzer. The measurement results of each PCB will be shown and compared in Chapter 5.

4.3 Measurement of Thermal Properties

In this section, the measurement circuit and the measurement procedures of thermal properties of the PCB will be introduced.

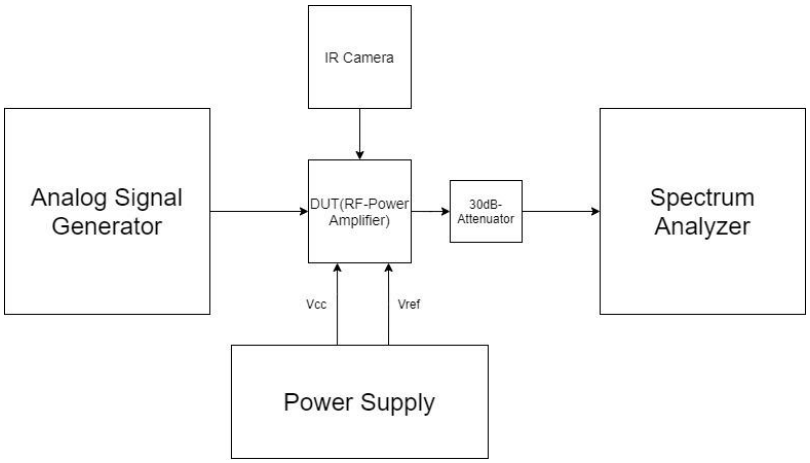
4.3.1 Measurement Circuit of Thermal Properties

The thermal properties of the power amplifier are mainly represented by its temperature distribution on the PCB under operation. Therefore, the IR camera is needed to measure the temperature distribution on the PCB. Besides, the power amplifier also needs DC power supply to amplify the RF signal for operation.

In the practical application of the power amplifier, the frequency of the RF signal to be amplified is in the frequency range from 5.725 to 5.875 GHz. This is because in the practical application, the transponder will be embedded in mechanical tools and placed in metallic environments, the resonance frequency of transponder will shift around 5.8 GHz. Thus, analog signal generator is needed to simulate the RF input signal of the power amplifier from 5.725 to 5.875 GHz. In addition, it is also needed to use the spectrum analyzer to observe the power of the output signal from the power amplifier to see if the power can reach required 33 dBm, so that in the practical application, the amplified signal can be successfully received in some distance by the transponder.

With the purpose of preventing the output signal of power amplifier from damaging the spectrum analyzer, a “30 dB” attenuator is also added after the power amplifier to reduce the output power. The schematic and physical diagram of the measurement circuit of thermal properties are shown in Figure 4-5.

a)



b)

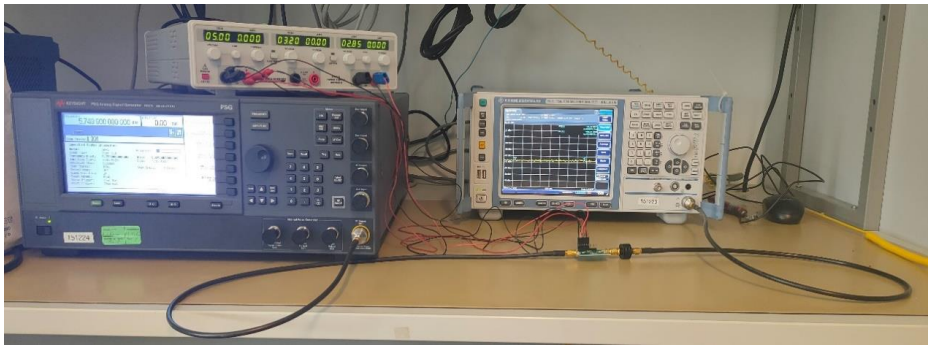


Figure 4-5 *a)* Schematic and *b)* physical diagram of measurement circuit of thermal properties

4.3.2 Measurement of the Wire

Since the measurement circuit cannot be calibrated directly, the attenuation of the wire from analog signal generator to power amplifier and from the “30 dB” attenuator to spectrum analyzer need to be measured. The measurement is similar as in chapter 4.2.2. Here, an adapter is required at each of the two interfaces. The measurement and measurement result of the attenuation of the wire are shown in Figure 4-6.

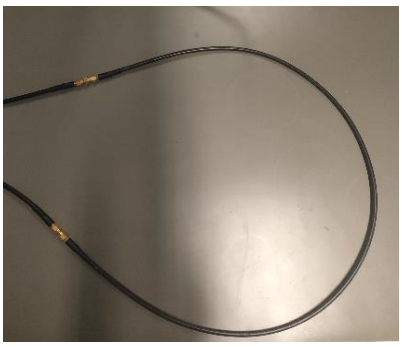
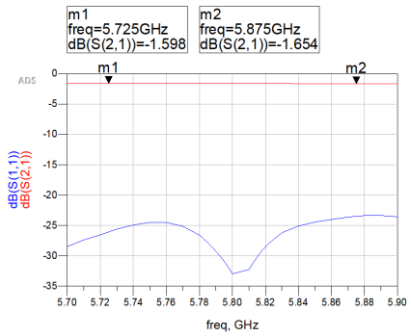
a)  *b)* 

Figure 4-6 *a)* Measurement and *b)* measurement result of the wire

It can be concluded from Figure 4-6 *b)* that in the frequency range from 5.725 to 5.875 GHz, S_{21} can also be roughly regarded as linear. Due to very small value changes, the average value can be used to represent the S_{21}, namely the attenuation, in the frequency range from 5.725 to 5.875 GHz.

$$A_{\text{wire}} + 2 \cdot A_{\text{adapter}} = \frac{1.598\ \text{dB} + 1.654\ \text{dB}}{2} = 1.626\ \text{dB} \tag{4.4}$$

According to the previous measurement of the adapter in Section 4.2.2 and Equation (4.1) and (4.3), the attenuation of the wire and "30 dB" attenuator with wire can be calculated as:

$$A_{\text{wire}} = 1.626\ \text{dB} - 2 \cdot 0.050\ \text{dB} = 1.526\ \text{dB} \tag{4.5}$$

$$\begin{aligned} A_{\text{attenuator with wire}} &= A_{\text{attenuator}} + A_{\text{wire}} = 28.335\ \text{dB} + 1.526\ \text{dB} \\ &= 29.861\ \text{dB} \end{aligned} \tag{4.6}$$

Therefore, in the frequency range from 5.725 to 5.875 GHz, the attenuation of the wire can be regarded as 1.526 dB, and the attenuation of "30 dB" attenuator with wire can be regarded as 29.861 dB.

4.3.3 Measurement of Temperature Distribution

The PCBs are connected into the measurement circuit separately, as shown in Figure 4-5 *b)*. In order to make the chip work like in the practical application, the voltage V_{CC1}, V_{CC2} and V_{CC3} should be 5 V. Besides, the voltage V_{REF} should be 2.85 V.

The power of the input signal from the analog signal generator is initially set to 0 dBm, and its frequency constantly sweeps between 5.725 and 5.875 GHz. Then, the power spectrum of output signal in the analyzer are observed. According to Equation (4.6), the attenuation of "30 dB" attenuator with wire is approximately -29.861 dB between 5.725 and 5.875 GHz, so the power measured by the spectrum analyzer only needs to be approximately 3.139 dBm. Then, the power of the input signal is increased by 0.5 dBm each time, until the power spectrum in the spectrum analyzer can reach approximately 3 dBm between 5.725 and 5.875 GHz.

Since the frequency of the input signal is constantly sweeping, the output signal is also constantly changing. Therefore, recording the maximum value needs to be set in the spectrum analyzer. The example power spectrum is shown in Figure 4-7. The temperature distribution on the PCBs can be then measured by using IR camera. The measurement results will be specifically shown and compared in Chapter 5.

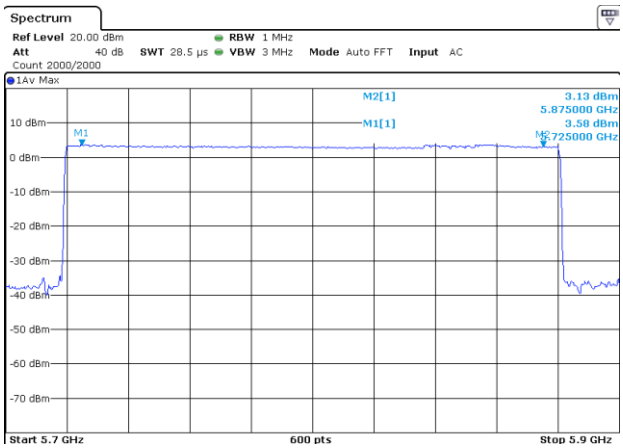


Figure 4-7 Example power spectrum of output signal

5 Measurement Results and Evaluation

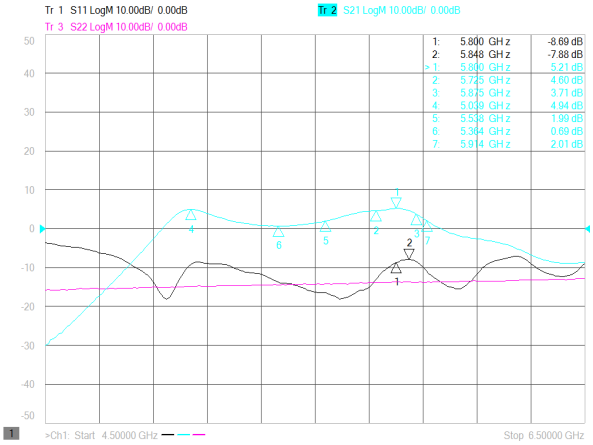
In this chapter, the basic PCB and the other five produced PCBs will be measured at first. The measurement results will be then calculated and analyzed. Finally, the electrical characteristics and thermal properties of the six PCBs will be compared and evaluated.

5.1 Measurement Results

According to the introductions in Section 4.2 and 4.3, the electrical characteristics and thermal properties of the basic PCB and other five PCBs produced to improve heat dissipation are measured separately. The measurement results are shown separately in the following sections. Through the analysis and calculation of the measurement results, some characteristic parameters of the PCB can be obtained for subsequent comparison and evaluation.

5.1.1 Measurement Results of the Basic PCB

a)



b)

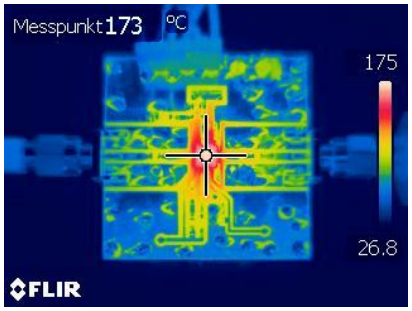


Figure 5-1 *a)* S-parameters of the basic PCB with "30 dB" attenuator and *b)* temperature distribution on the basic PCB

From Figure 5-1 *a)*, it can be seen that S_{11} is approximately -10 dB and S_{21} is approximately 4.5 dB in the frequency range from 5.725 to 5.875 GHz. According to Equation (4.3), the gain of the basic PCB in the electrical measurement $G_{\text{Basic PCB in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{Basic PCB in EM}} = S_{21} + A_{\text{attenuator}} \approx 4.5\ \text{dB} + 28.3\ \text{dB} = 32.8\ \text{dB} \qquad (5.1)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is very good, approximately 10% of the input power is reflected back. Besides, the gain of the basic PCB in the electrical measurement is also great. Theoretically, when the input power of the basic PCB is approximately 0.2 dBm, the output power of the basic PCB can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power from analog signal generator is 0 dBm and the frequency is between 5.725 GHz and 5.875 GHz, the power spectrum of output signal in the spectrum analyzer can only reach approximately -5 dBm. At this time, the temperature distribution on the basic PCB is shown in Figure 5-1 *b)*. Since the temperature of the chip has exceeded the maximum junction temperature (160 °C), the input power has not been continuously increased to make the power spectrum of output signal reach 3 dBm, as analyzed in Section 4.3.3. Nevertheless, the gain of the basic PCB in the thermal measurement can be calculated as:

$$P_{\text{ouput}}^{\text{dBm}} = P_{\text{input}}^{\text{dBm}} - A_{\text{wire}} + G_{\text{Basic PCB in TM}} - A_{\text{attenuator with wire}} \tag{5.2}$$

According to Equation (4.5), (4.6) and (5.2), the gain of the basic PCB in the thermal measurement $G_{\text{Basic PCB in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{Basic PCB in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} + A_{\text{wire}} + A_{\text{attenuator with wire}} \\ &\approx 26.4\ \text{dB} \end{aligned} \tag{5.3}$$

According to Equation (5.3), it can be seen that the gain of the basic PCB in the thermal measurement is only approximately 26.4 dB, which is approximately 6.4 dB smaller than the gain in the electrical measurement (32.8 dB). This indicates that the chip cannot work normally on the basic PCB in the thermal measurement.

The copper ground planes are separate on the basic PCB. From the temperature distribution on the basic PCB, as shown in Figure 5-1 *b)*, it can be seen that the heat on the basic PCB cannot be conducted well. It is consistent with the thermal simulation result of the basic PCB, as shown in Figure 3-6 *a)*. In addition, the measured maximum temperature of the chip (175 °C) is 11 °C higher than the maximum temperature in the thermal simulation (164 °C). The reason may be due to the inability to conduct plating via in IMS, so copper wires are used to achieve electrical and thermal connections between the upper and lower sides of the PCB. However, the heat conduction of copper wire is worse than that of plating via. Besides, at the connection, the heat might not conduct well due to the bad contact between the copper wire and the copper plane.

5.1.2 Measurement Results of the 2L8D4A9S

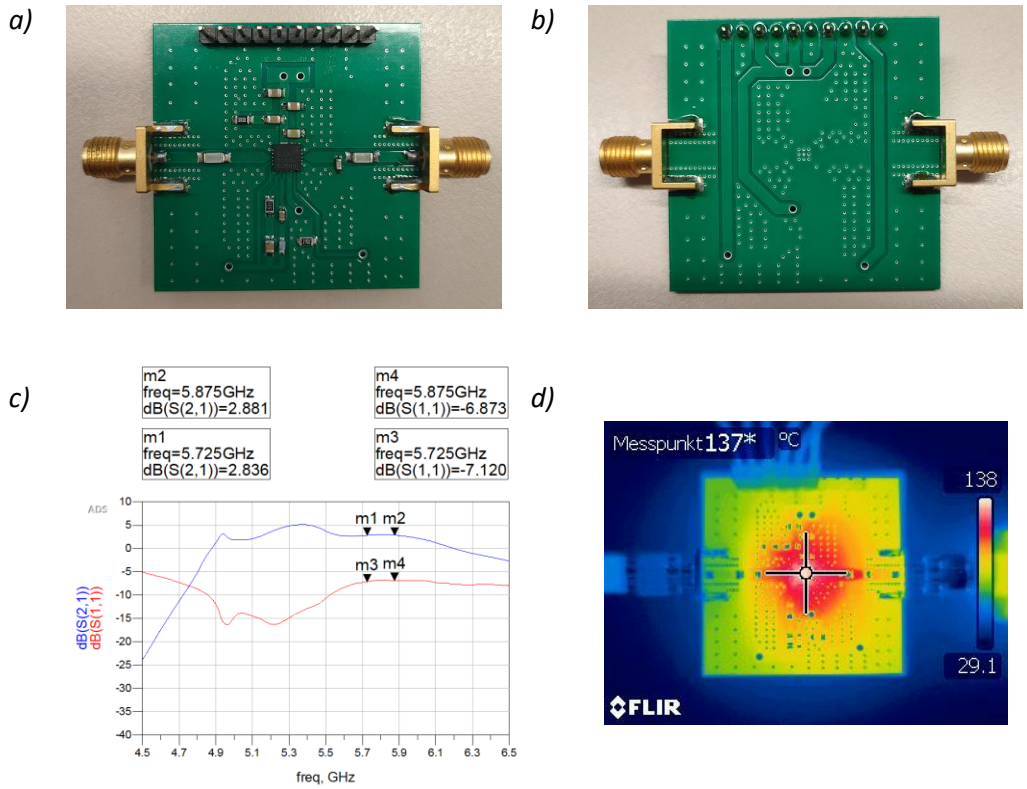


Figure 5-2 Physical pictures *a)* top view *b)* bottom view of the 2L8D4A9S, *c)* S-parameters of the 2L8D4A9S with "30 dB" attenuator and *d)* temperature distribution on the 2L8D4A9S

From Figure 5-2 *c)*, it can be seen that S_{11} is approximately -7.0 dB and S_{21} is approximately 2.8 dB in the frequency range from 5.725 to 5.875 GHz. Similarly, the gain of the 2L8D4A9S in the electrical measurement $G_{\text{2L8D4A9S in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{2L8D4A9S in EM}} = S_{21} + A_{\text{attenuator}} \approx 2.8\ \text{dB} + 28.3\ \text{dB} = 31.1\ \text{dB} \qquad (5.4)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is critical, approximately 20% of the input power is reflected back. Besides, the gain of the 2L8D4A9S in the electrical measurement is not bad. Theoretically, when the

input power is approximately 1.9 dBm, the output power can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power is 5.5 dBm and the frequency is between 5.725 and 5.875 GHz, the power spectrum of output signal can reach approximately 3 dBm, as analyzed in Section 4.3.3. Similarly, the gain of the 2L8D4A9S in the thermal measurement $G_{\text{2L8D4A9S in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{2L8D4A9S in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} + A_{\text{wire}} + A_{\text{attenuator with wire}} \\ &\approx 28.9 \text{ dB} \end{aligned} \tag{5.5}$$

According to Equation (5.5), it can be seen that the gain of the 2L8D4A9S in the thermal measurement is 28.9 dB, which is approximately 2.2 dB smaller than the gain in the electrical measurement (31.1 dB).

The copper ground planes are connected together on the 2L8D4A9S. From the temperature distribution on the 2L8D4A9S, as shown in Figure 5-2 *d)*, it can be seen that the heat on the 2L8D4A9S can be conducted better, compared with the basic PCB. The measured maximum temperature of the chip (138 °C) is 7 °C lower than the maximum temperature in the thermal simulation (145 °C). The reason may be that in “SIPro/PIPro” of ADS software, the heat dissipation on components such as SMA connectors cannot be considered. In fact, the SMA connector is directly connected to the top and bottom copper layers of the PCB, so it can also conduct some heat well.

5.1.3 Measurement Results of the 2L8D4A4S

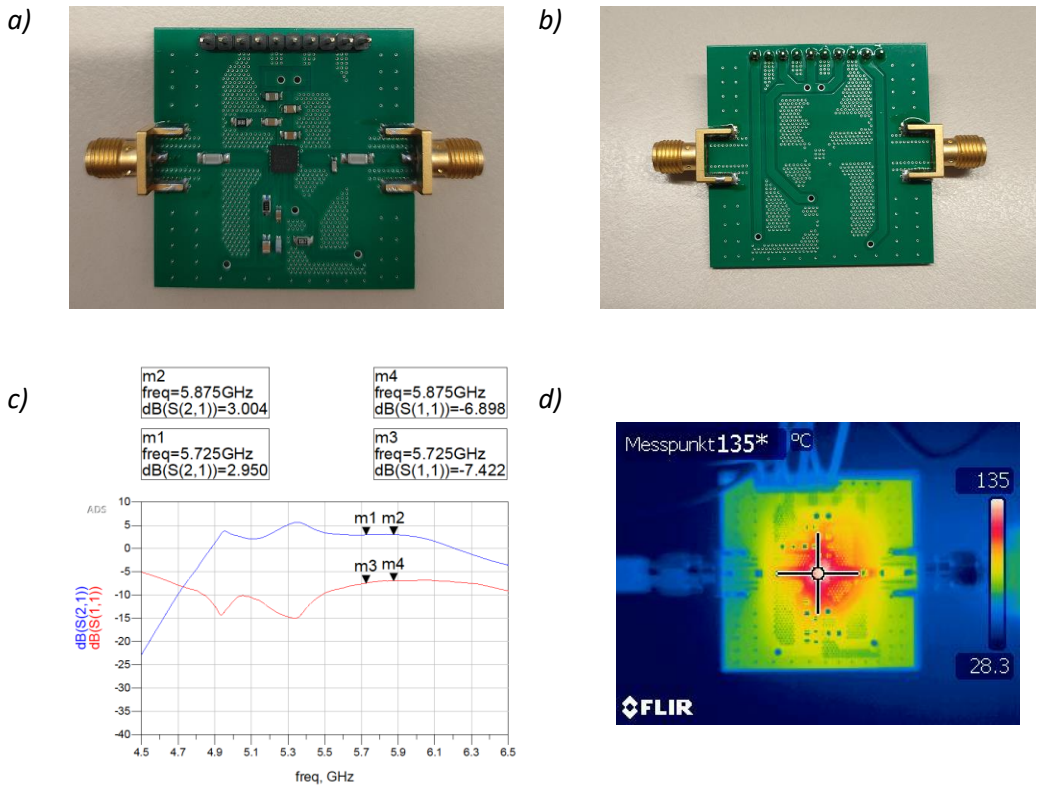


Figure 5-3 Physical pictures *a)* top view *b)* bottom view of the 2L8D4A4S, *c)* S-parameters of the 2L8D4A4S with "30 dB" attenuator and *d)* temperature distribution on the 2L8D4A4S

From Figure 5-3 *c)*, it can be seen that S_{11} is approximately -7.2 dB and S_{21} is approximately 3.0 dB in the frequency range from 5.725 to 5.875 GHz. Similarly, the gain of the 2L8D4A4S in the electrical measurement $G_{\text{2L8D4A4S in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{2L8D4A4S in EM}} = S_{21} + A_{\text{attenuator}} \approx 3.0\ \text{dB} + 28.3\ \text{dB} = 31.3\ \text{dB} \qquad (5.6)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is acceptable, approximately 19% of the input power is reflected back. Besides, the gain of the 2L8D4A4S in the electrical measurement is not bad. Theoretically, when

the input power is approximately 1.7 dBm, the output power can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power is 5 dBm and the frequency is between 5.725 and 5.875 GHz, the power spectrum of output signal can reach approximately 3 dBm, as analyzed in Section 4.3.3. Similarly, the gain of the 2L8D4A4S in the thermal measurement $G_{\text{2L8D4A4S in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{2L8D4A4S in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} + A_{\text{wire}} + A_{\text{attenuator with wire}} \\ &\approx 29.4 \text{ dB} \end{aligned} \tag{5.7}$$

According to Equation (5.7), it can be seen that the gain of the 2L8D4A4S in the thermal measurement is only 29.4 dB, which is approximately 1.9 dB smaller than the gain in the electrical measurement (31.3 dB).

The copper ground planes are also connected together on the 2L8D4A4S. From the temperature distribution on the 2L8D4A4S, as shown in Figure 5-3 *d)*, it can be seen that the heat on the 2L8D4A4S can also be conducted better, compared with the basic PCB. The measured maximum temperature of the chip (135 °C) is 5 °C lower than the maximum temperature in the thermal simulation (140 °C). The reason is the same as in Section 5.1.2.

5.1.4 Measurement Results of the 2L5D4A9S

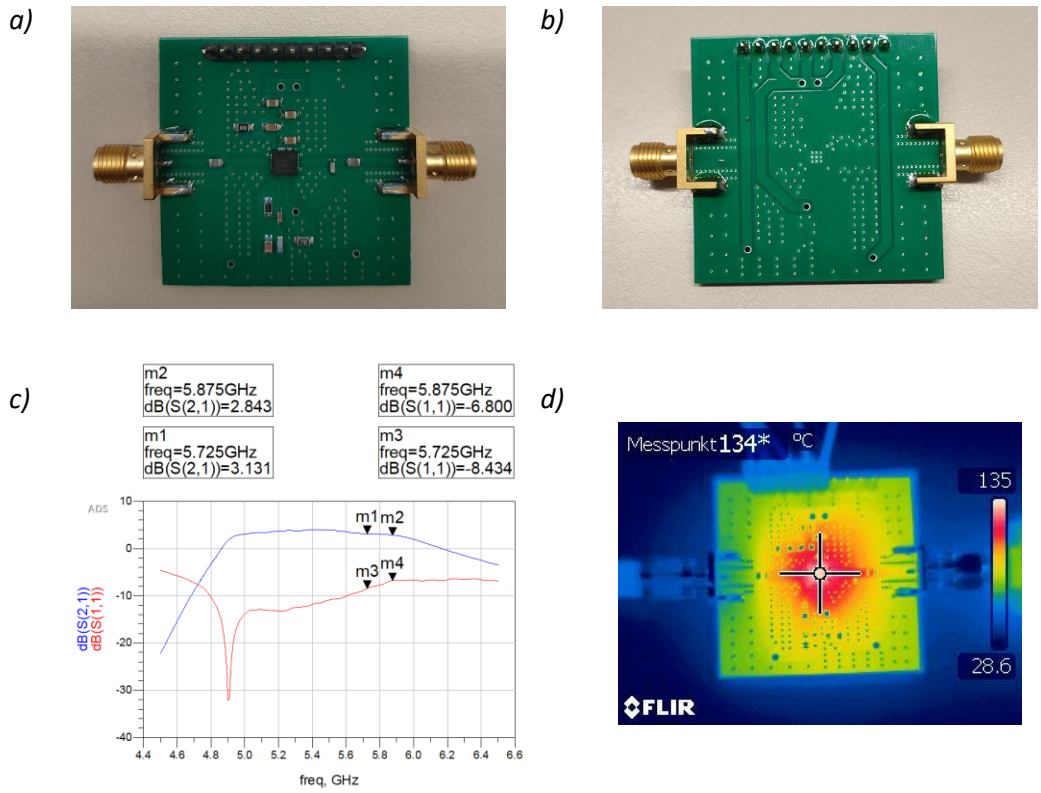


Figure 5-4 Physical pictures *a)* top view *b)* bottom view of the 2L5D4A9S, *c)* S-parameters of the 2L5D4A9S with "30 dB" attenuator and *d)* temperature distribution on the 2L5D4A9S

From Figure 5-4 *c)*, it can be seen that S_{11} is approximately -7.6 dB and S_{21} is approximately 3.0 dB in the frequency range from 5.725 to 5.875 GHz. Similarly, the gain of the 2L5D4A9S in the electrical measurement $G_{\text{2L5D4A9S in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{2L5D4A9S in EM}} = S_{21} + A_{\text{attenuator}} \approx 3.0\ \text{dB} + 28.3\ \text{dB} = 31.3\ \text{dB} \qquad (5.8)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is not bad, approximately 17% of the input power is reflected back. Besides, the gain of the 2L5D4A9S in the electrical measurement is also not bad. Theoretically, when

the input power is approximately 1.7 dBm, the output power can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power is 5 dBm and the frequency is between 5.725 and 5.875 GHz, the power spectrum of output signal can reach approximately 3 dBm, as analyzed in Section 4.3.3. Similarly, the gain of the 2L5D4A9S in the thermal measurement $G_{\text{2L5D4A9S in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{2L5D4A9S in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} + A_{\text{wire}} + A_{\text{attenuator with wire}} \\ &\approx 29.4\text{dB} \end{aligned} \tag{5.9}$$

According to Equation (5.9), it can be seen that the gain of the 2L5D4A9S in the thermal measurement is only 29.4 dB, which is approximately 1.9 dB smaller than the gain in the electrical measurement (31.3 dB).

The copper ground planes are also connected together on the 2L5D4A9S. From the temperature distribution on the 2L5D4A9S, as shown in Figure 5-4 *d)*, it can be seen that the heat on the 2L5D4A9S can also be conducted better, compared with the basic PCB. The measured maximum temperature of the chip (135 °C) is also slightly lower than the maximum temperature in the thermal simulation (141 °C). The reason is the same as in Section 5.1.2.

5.1.5 Measurement Results of the 2L5D4A4S

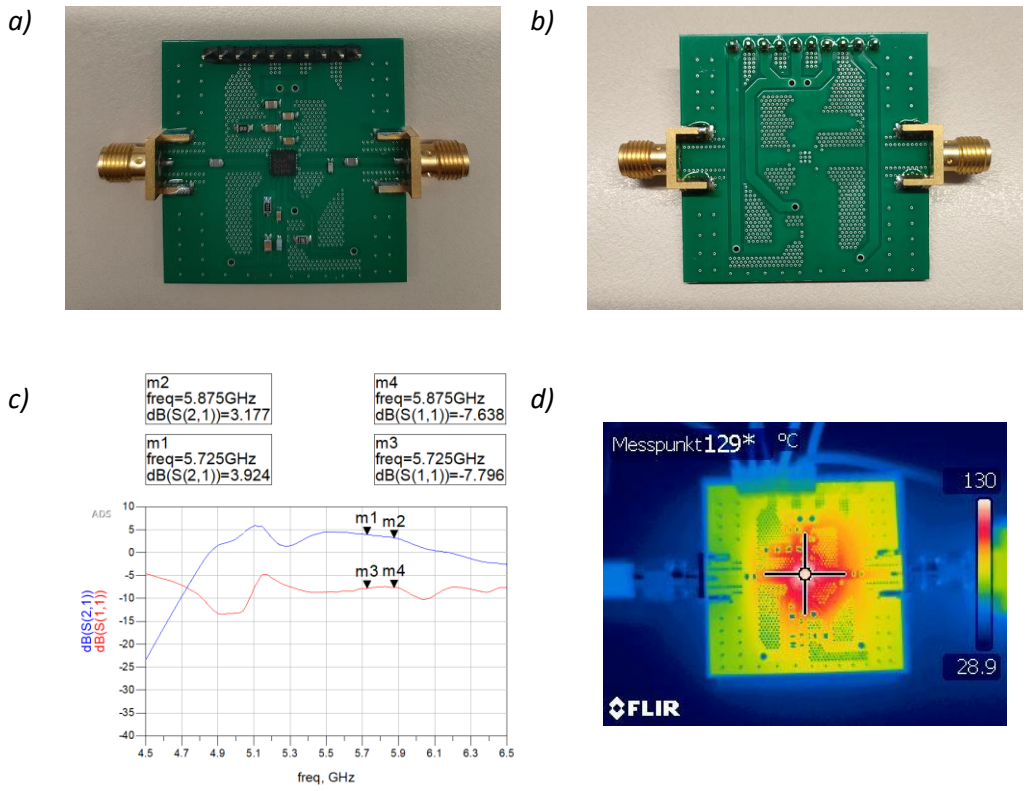


Figure 5-5 Physical pictures *a)* top view *b)* bottom view of the 2L5D4A4S, *c)* S-parameters of the 2L5D4A4S with "30 dB" attenuator and *d)* temperature distribution on the 2L5D4A4S

From Figure 5-5 *c)*, it can be seen that S_{11} is approximately -7.7 dB and S_{21} is approximately 3.6 dB in the frequency range from 5.725 to 5.875 GHz. Similarly, the gain of the 2L5D4A4S in the electrical measurement $G_{\text{2L5D4A4S in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{2L5D4A4S in EM}} = S_{21} + A_{\text{attenuator}} \approx 3.6\ \text{dB} + 28.3\ \text{dB} = 31.9\ \text{dB} \quad (5.10)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is not bad, approximately 17% of the input power is reflected back. Besides, the gain

of the 2L5D4A4S in the electrical measurement is good. Theoretically, when the input power is approximately 1.1 dBm, the output power can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power is 4.5 dBm and the frequency is between 5.725 and 5.875 GHz, the power spectrum of output signal can reach approximately 3 dBm, as analyzed in Section 4.3.3. Similarly, the gain of the 2L5D4A4S in the thermal measurement $G_{\text{2L5D4A4S in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{2L5D4A4S in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} - G_{\text{wire}} - G_{\text{attenuator with wire}} \\ &\approx 29.9 \text{ dB} \end{aligned} \tag{5.11}$$

According to Equation (5.11), it can be seen that the gain of the 2L5D4A4S in the thermal measurement is approximately 29.9 dB, which is 2.0 dB smaller than the gain in the electrical measurement (31.9 dB).

The copper ground planes are also connected together on the 2L5D4A4S. From the temperature distribution on the 2L5D4A4S, as shown in Figure 5-5 *d)*, it can be seen that the heat on the 2L5D4A4S can also be conducted better, compared with the basic PCB. The measured maximum temperature of the chip (130 °C) is 6 °C lower than the maximum temperature in the thermal simulation (136 °C). The reason is the same as in Section 5.1.2.

5.1.6 Measurement Results of the 4L4A4S

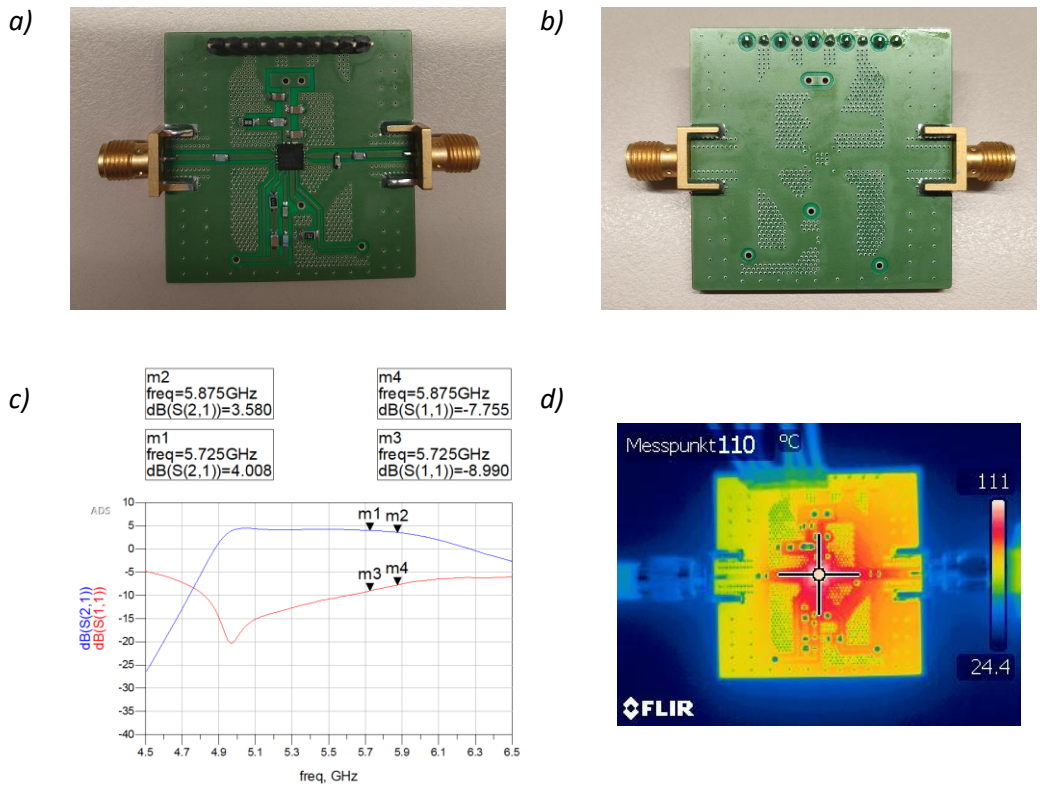


Figure 5-6 Physical pictures *a)* top view *b)* bottom view of the 4L4A4S, *c)* S-parameters of the 4L4A4S with "30 dB" attenuator and *d)* temperature distribution on the 4L4A4S

From Figure 5-6 *c)*, it can be seen that S_{11} is approximately -8.4 dB and S_{21} is approximately 3.8 dB in the frequency range from 5.725 to 5.875 GHz. In addition, by comparing the S-parameters of the other PCBs, it can be seen that there is basically no fluctuation in the S_{11} and S_{21} curves of the 4L4A4S. This indicates that the anti-interference ability of the 4L4A4S is better. Similarly, the gain of the 4L4A4S in the electrical measurement $G_{\text{4L4A4S in EM}}$ in the frequency range from 5.725 to 5.875 GHz can be calculated as:

$$G_{\text{4L4A4S in EM}} = S_{21} + A_{\text{attenuator}} \approx 3.8\ \text{dB} + 28.3\ \text{dB} = 32.1\ \text{dB} \qquad (5.12)$$

In other words, the impedance matching of the basic PCB to the 50 Ohm-system is good, approximately 14% of the input power is reflected back. Besides, the gain of the 4L4A4S in the electrical measurement is also good. Theoretically, when the input power is approximately 0.9 dBm, the output power can reach approximately 33 dBm.

In the measurement of thermal properties, when the input power is 4 dBm and the frequency is between 5.725 and 5.875 GHz, the power spectrum of output signal can reach approximately 3 dBm, as analyzed in Section 4.3.3. Similarly, the gain of the 4L4A4S in the thermal measurement $G_{\text{4L4A4S in TM}}$ can be calculated as:

$$\begin{aligned} G_{\text{4L4A4S in TM}} &= P_{\text{ouput}}^{\text{dBm}} - P_{\text{input}}^{\text{dBm}} - G_{\text{wire}} - G_{\text{attenuator with wire}} \\ &\approx 30.4\ \text{dB} \end{aligned} \tag{5.13}$$

According to Equation (5.13), it can be seen that the gain of the 4L4A4S in the thermal measurement is only approximately 30.4 dB, which is 1.7 dB smaller than the gain in the electrical measurement (32.1 dB).

The copper ground planes are also connected together on the 4L4A4S. From the temperature distribution on the 4L4A4S, as shown in Figure 5-6 *d)*, it can be seen that the heat on the 4L4A4S can also be conducted better, compared with the basic PCB. The measured maximum temperature of the chip (111 °C) is 8 °C lower than the maximum temperature in the thermal simulation (119 °C). The reason is the same as in Section 5.1.2.

5.2 Comparison and Evaluation

In this section, the measurement results of the six PCBs will be summarized and compared. Similarly, the performance of the PCBs will be evaluated respectively from two aspects: electrical characteristics and thermal properties.

5.2.1 Comparison and Evaluation of Electrical Characteristics

According to the measurements and calculations in Section 5.1, the input reflection coefficient S_{11} and the gain in the electrical measurement $G_{\text{in EM}}$ as well as in the

thermal measurement $G_{\text{in TM}}$ of each PCB are summarized in Table 5-1 for comparison.

PCB Name	S_{11} in dB	$G_{\text{in EM}}$ in dB	$G_{\text{in TM}}$ in dB
Basic	-10.0	32.8	26.4*
2L8D4A9S	-7.0	31.1	28.9
2L8D4A4S	-7.2	31.3	29.4
2L5D4A9S	-7.3	31.3	29.4
2L5D4A4S	-7.7	31.9	29.9
4L4A4S	-8.4	32.1	30.4

Table 5-1 The input reflection coefficient and gain in the electrical measurement as well as in the thermal measurement of each PCB

The first electrical parameter to be compared is S_{11}. In the frequency range from 5.725 to 5.875 GHz, the S_{11} of the basic PCB is the lowest, approximately -10 dB. In other words, compared with the other five PCBs, the impedance matching of the basic PCB to the 50 Ohm-system is the best. The reason is that, AC ground and DC ground are separated on the basic PCB, so there is almost no interference between the AC signal and the DC signal. In addition, the impedance of the transmission line is more consistent with the calculation. Since AD ground and DC ground are not separated on the other PCBs for better heat conduction, the S_{11} of the other five PCBs are slightly worse. They are all between -7.0 and -8.4 dB. But there are some differences among them. By comparing the S_{11} of 2L8D4A9S and 2L5D4A9S (or 2L8D4A4S and 2L5D4A4S), it can be concluded that the S_{11} of the PCB with 508 µm dielectric is slightly lower (approximately 0.3 dB) than that of the PCB with 813 µm dielectric. The reason is that the signal return path becomes shorter, so that the impedance of the signal return path is smaller. The matching of the transmission line is then better. By comparing the S_{11} of 2L8D4A9S and 2L8D4A4S (or 2L5D4A9S and 2L5D4A4S), it can

be concluded that the S_{11} of the PCB with 400 µm via-to-via spacing is slightly lower than that of the PCB with 900 µm via-to-via spacing. The reason is that the signal return path becomes shorter and the potential difference between the upper and lower ground is smaller, so that the matching of the transmission line is better. By comparing S_{11} of 2L5D4A4S and 4L4A4S, it can be concluded that S_{11} of the four-layer PCB is lower than that of the two-layer PCB. The reason is that there are two complete ground planes in the four-layer structure, so the impedance of the signal return path is smaller and some interference can also be reduced. Thus, the impedance matching of the transmission line is better.

The second electrical parameter to be compared is $G_{\mathrm{in\ EM}}$. The $G_{\mathrm{in\ EM}}$ of these six PCBs are all consistent with the parameters from the data sheet, as shown in Table 3-1. Generally, for an RF-power amplifier, the better the impedance matching of the transmission line, the higher the gain. Therefore, the differences of the $G_{\mathrm{in\ EM}}$ among different PCBs is similar to the differences of the S_{11} among different PCBs. Similarly, the $G_{\mathrm{in\ EM}}$ of the basic PCB is the highest, approximately 32.8 dB. The $G_{\mathrm{in\ EM}}$ of the other five PCBs are slightly worse. They are all between 31.1 and 32.1 dB. But there are also some differences among them. By comparing the data in Table 5-1, it can also be concluded that the PCB with 508 µm (compared with 813 µm) dielectric, the PCB with 400 µm (compared with 900 µm) via-to-via spacing and four-layer (compared with two-layer) PCB have higher $G_{\mathrm{in\ EM}}$. The reason is similar to the analysis of the S_{11}.

The last electrical parameter to compare is $G_{\mathrm{in\ TM}}$. As mentioned in Section 5.1.1, the temperature of the chip on the basic PCB has exceeded the maximum junction temperature before the output power reaches 33 dBm. Thus, it is not comparable with $G_{\mathrm{in\ TM}}$ of the other PCBs. However, it can be seen that the $G_{\mathrm{in\ TM}}$ of the basic PCB is significantly lower than its $G_{\mathrm{in\ EM}}$. This indicates that the chip cannot work normally on the basic PCB due to the high temperature. For the $G_{\mathrm{in\ TM}}$ of the other five PCBs, the differences of the $G_{\mathrm{in\ TM}}$ among them is similar as differences of the $G_{\mathrm{in\ EM}}$ among them. By comparing the data in Table 5-1, it can also be concluded that the PCB with 508 µm (compared with 813 µm) dielectric, the PCB with 400 µm (compared with 900 µm) via-to-via spacing and four-layer (compared with two-layer) PCB have higher $G_{\mathrm{in\ TM}}$. The reason is similar to the analysis of the S_{11}. In addition, the

$G_{\text{in TM}}$ of these five PCBs is approximately 2 dB lower than their $G_{\text{in EM}}$. This indicates that in the practical application, the gain of the PCB might be reduced due to heating.

In summary, the electrical characteristics of the basic PCB in electrical measurement are better than the other five boards. However, the heat of the chip on the basic PCB cannot be conducted well, so that the chip cannot work normally due to high temperature in the thermal measurement, namely in the practical application. Although the impedance matching of the transmission line and the gain in the electrical measurement of the other five PCBs are slightly worse than that of the basic PCB, they can make the output power of the PCB reach required 33 dBm. In the practical application, the gain might be reduced by approximately 2 dB due to heating. Among the two-layer PCBs, the PCB with 508 µm dielectric, 4 cm×4 cm area and 400 µm via-to-via spacing around the chip has the best electrical characteristics in the practical application. Besides, the four-layer structure can further optimize the electrical characteristics of the PCB.

5.2.2 Comparison and Evaluation of Thermal Properties

PCB Name	$T_{max\,\text{in TM}}$ in °C	$T_{max\,\text{in TS}}$ in °C
Basic	175*	164
2L8D4A9S	138	145
2L8D4A4S	135	140
2L5D4A9S	135	141
2L5D4A4S	130	136
4L4A4S	111	119

Table 5-2 The maximum temperature in the thermal measurement and in the thermal simulation

According to the measurements and calculations in Section 3.5 and 5.1, the maximum temperature in the thermal measurement $T_{max\,\mathrm{in\,TM}}$ and in the thermal simulation $T_{max\,\mathrm{in\,TS}}$ are summarized in Table 5-2 for comparison.

As mentioned in Section 5.1.1, the temperature of the chip on the basic PCB has exceeded the maximum junction temperature before the output power reaches 33 dBm. Thus, it is not comparable with the $T_{max\,\mathrm{in\,TM}}$ on the other PCBs. Compared with the $T_{max\,\mathrm{in\,TS}}$ on the basic PCB, the $T_{max\,\mathrm{in\,TM}}$ has also greatly exceeded the expectation of the thermal simulation. The reason has been analyzed in Section 5.1.1.

For the $T_{max\,\mathrm{in\,TM}}$ on the other five PCBs are all approximately 6 °C lower than $T_{max\,\mathrm{in\,TS}}$. The reason has been analyzed in Section 5.1.2. Therefore, for the effects of different aspects, the temperature difference in $T_{max\,\mathrm{in\,TM}}$ is very similar to that in $T_{max\,\mathrm{in\,TS}}$. Consequently, the comparison and evaluation of the $T_{max\,\mathrm{in\,TM}}$ is similar to the comparison and evaluation of the $T_{max\,\mathrm{in\,TM}}$, as analyzed in chapter 3.5.2.

In summary, except the basic PCB, the chips on the other five PCBs can work normally below the maximum junction temperature. Among the two-layer PCBs, the PCB with 508 µm dielectric, 4 cm×4 cm area and 400 µm via-to-via spacing around the chip has the best thermal properties in the practical application. Similarly, the four-layer structure can further optimize the thermal properties of the PCB.

5.3 Conclusion of Measurement

Through the comparison of the measurement results, among 4 cm×4 cm area of the PCBs, the PCB of the four-layer structure with 400 µm via-to-via spacing around the chip have the best electrical characteristics and thermal properties. However, the production cost of the four-layer PCB is about 4 times more expensive than the two-layer PCB, so the PCB of two-layer structure with 508 µm dielectric, 4 cm×4 cm area and 400 µm via-to-via spacing around the chip is also a good and cost-effective choice.

6 Summary and Conclusion

In this bachelor thesis, on the basis of previous internship at IMS, a number of layouts of the PCB for RFID applications in the SHF band are designed. Through the analysis of a simple PCB thermal model, some cost-effective solutions are first proposed to improve the thermal performance of PCB. After that, the different layouts of the PCB are modeled and thermally simulated by using “SIPro/PIPro” function in ADS software. The simulation results are basically consistent with the analysis. Considering the production cost and the requirements in the practical application, five different designs with the area of 4 cm×4 cm are produced to measure and evaluate their electrical characteristics and thermal properties. The thermal measurement results of the PCB are basically consistent with the thermal simulation results.

Through the thermal simulation results and measurement results, it can be concluded that the AC ground and DC ground on the PCB of the RF-power amplifier have a great influence on the electrical characteristics and thermal properties. When AC ground and DC ground are separated, there is almost no interference between the AC signal and the DC signal. Therefore, the gain and impedance matching of transmission line is good. However, the heat on the PCB cannot be conducted well in the practical application, so the temperature of the chip might be too high, thereby degrading the electrical characteristics of the chip or even damaging the chip. On the contrary, when AC ground and DC ground are not separated, the electrical characteristics of the PCB are slightly worse, while the thermal characteristics are greatly improved. Therefore, the design requirements need to be specifically considered in

practice. In addition, increasing the density of the vias (reducing the via-to-via spacing) around the chip or appropriately reducing the thickness of the PCB can slightly improve the electrical characteristics and thermal properties of the PCB. Based on the consistency of the measurement results and the simulation results, it can be inferred that if the area is increased, the thermal performance will be significantly improved, similar to the results of the thermal simulation in Section 3.5. Therefore, in the practical application, if the front end of the RFID reader has more space left for the RF-power amplifier, it can also be considered to separate the AC ground from the DC ground on the PCB with larger area, such as 5 cm$\times$5 cm.

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Appendix

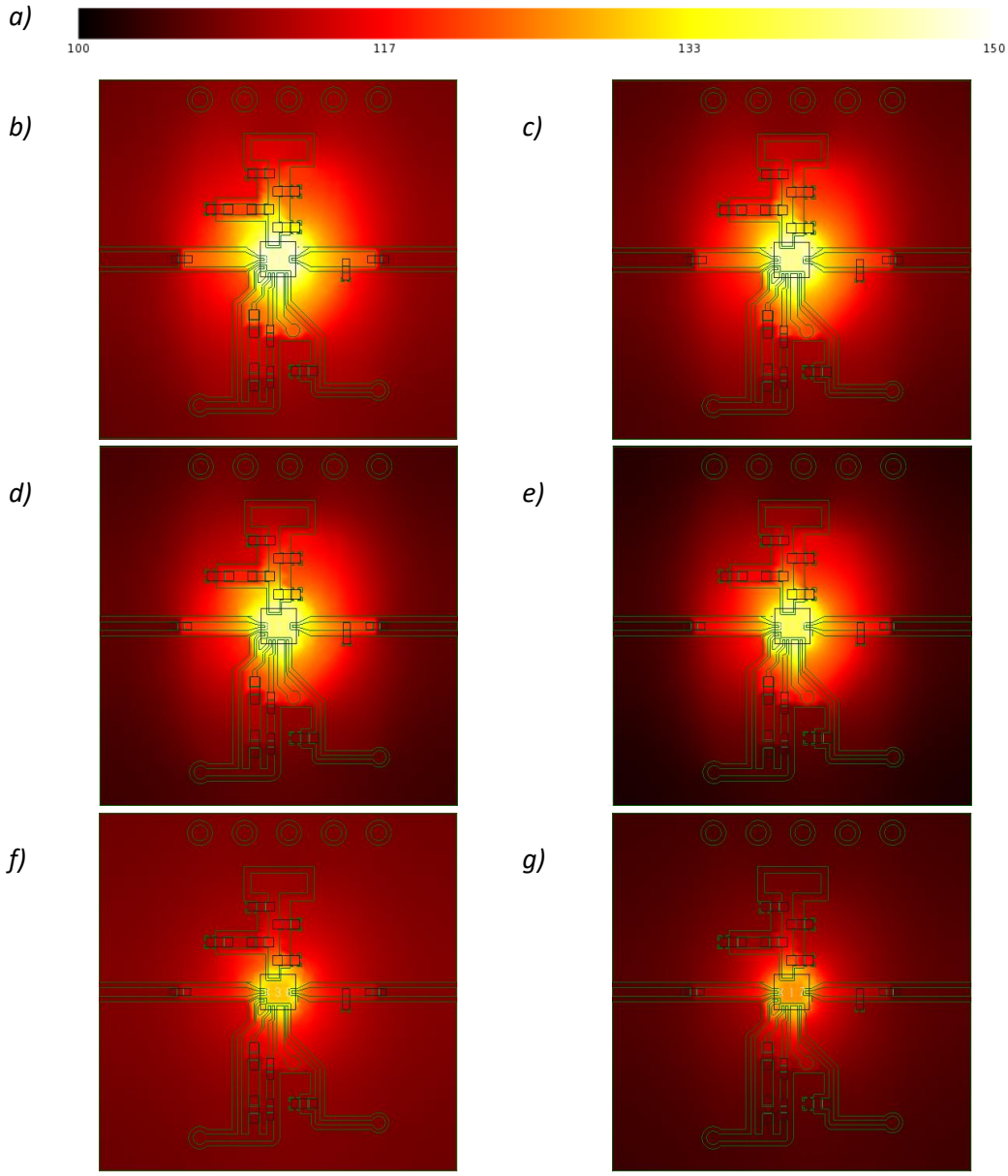

Figure A-1 The temperature distribution on the different PCBs with the same area of 4 cm×4 cm in the thermal simulation. *a)* scaling for the PCBs with the area of 4 cm×4 cm *b)* two-layer structure with 813 µm dielectric and 900 µm via-to-via spacing *c)* two-layer structure with 813 µm dielectric and 400 µm via-to-via spacing *d)* two-layer structure with 508 µm dielectric and 900 µm via-to-via spacing *e)* two-layer structure with 508 µm dielectric and 400 µm via-to-via spacing *f)* four-layer structure with 900 µm via-to-via spacing *g)* four-layer structure with 400 µm via-to-via spacing

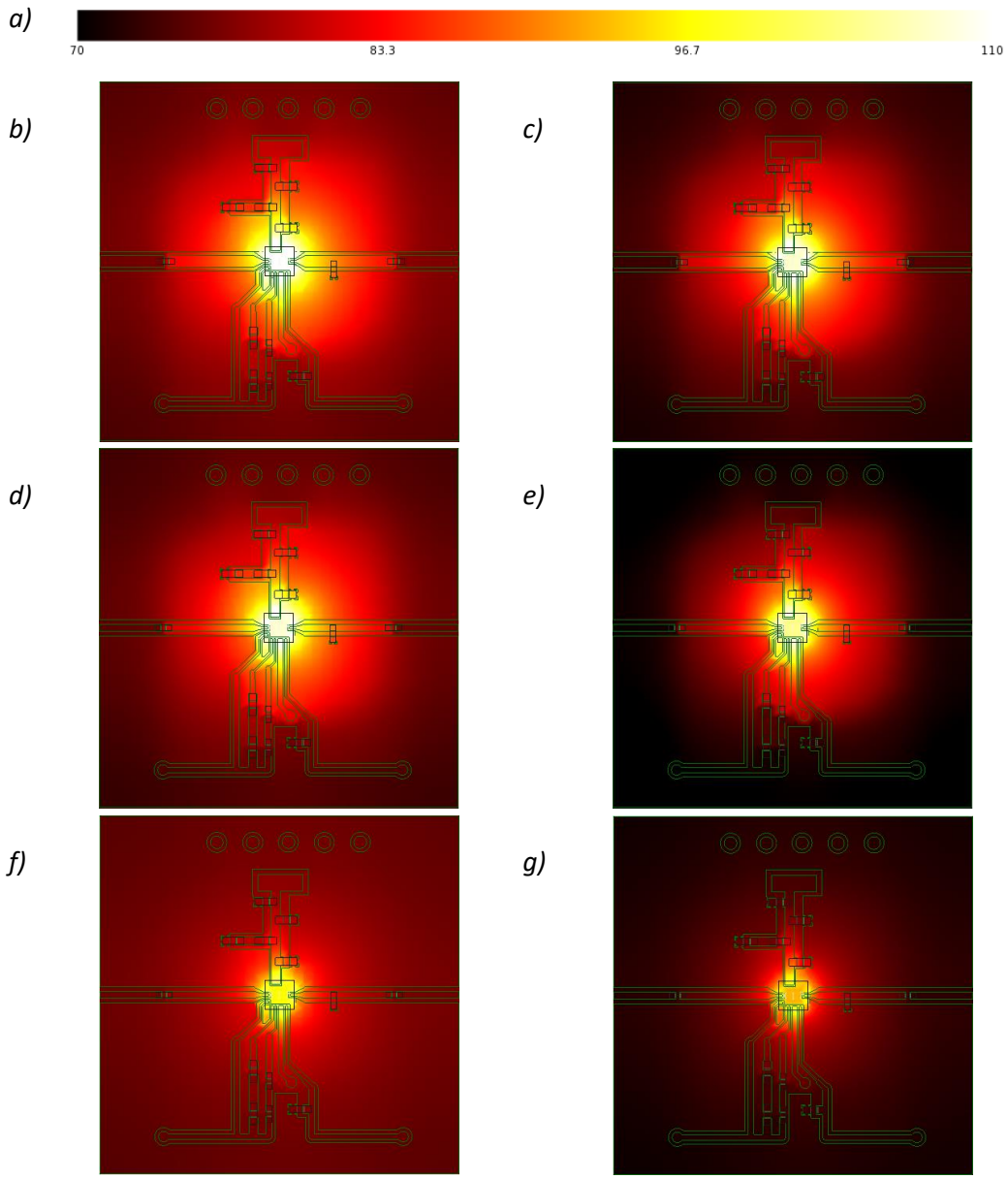

Figure A-2 The temperature distribution on the different PCBs with the same area of 5 cm×5 cm in the thermal simulation. *a)* scaling for the PCBs with the area of 5 cm×5 cm *b)* two-layer structure with 813 µm dielectric and 900 µm via-to-via spacing *c)* two-layer structure with 813 µm dielectric and 400 µm via-to-via spacing *d)* two-layer structure with 508 µm dielectric and 900 µm via-to-via spacing *e)* two-layer structure with 508 µm dielectric and 400 µm via-to-via spacing *f)* four-layer structure with 900 µm via-to-via spacing *g)* four-layer structure with 400 µm via-to-via spacing

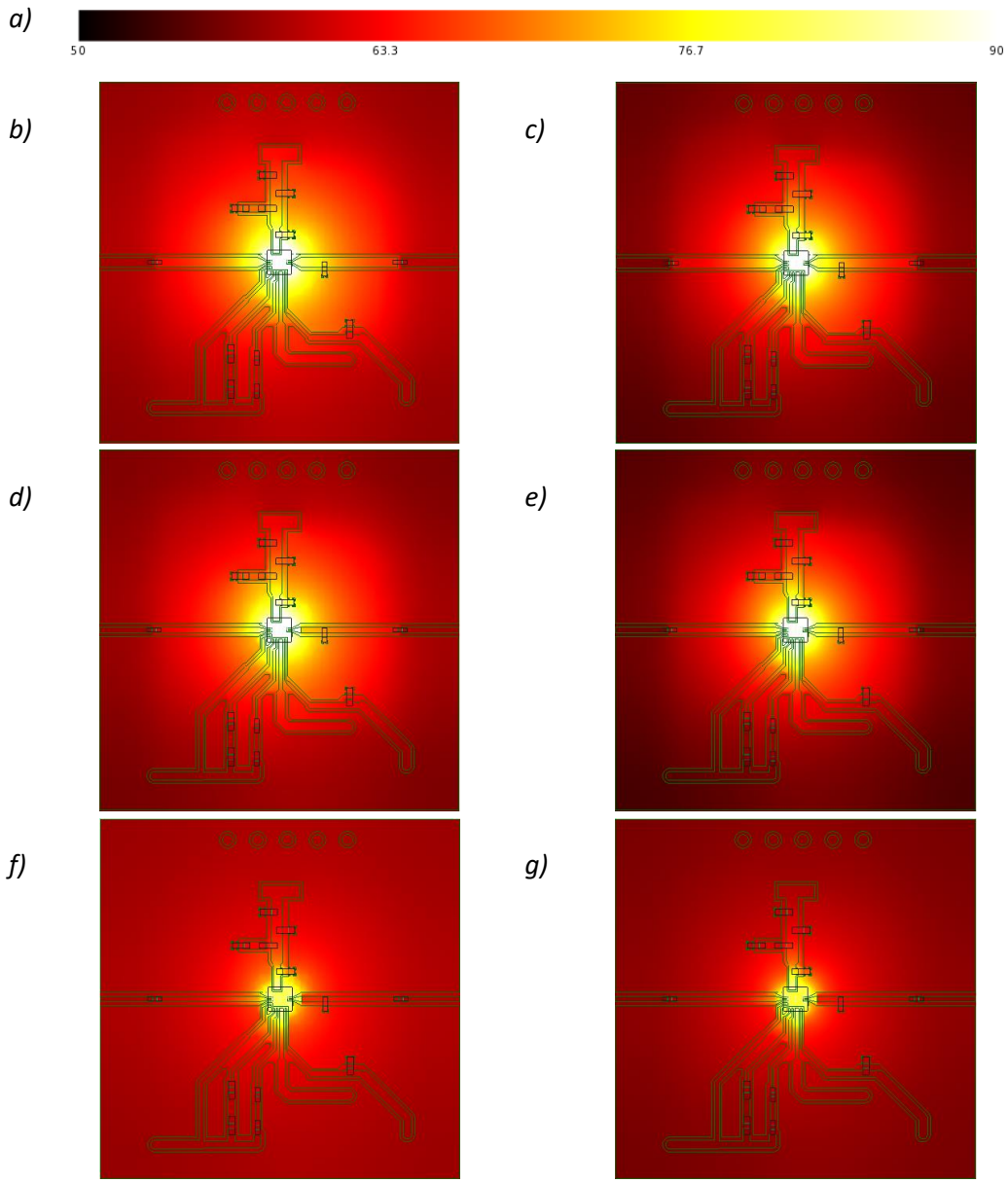

Figure A-3 The temperature distribution on the different PCBs with the same area of 6 cm×6 cm in the thermal simulation. *a)* scaling for the PCBs with the area of 6 cm×6 cm *b)* two-layer structure with 813 µm dielectric and 900 µm via-to-via spacing *c)* two-layer structure with 813 µm dielectric and 400 µm via-to-via spacing *d)* two-layer structure with 508 µm dielectric and 900 µm via-to-via spacing *e)* two-layer structure with 508 µm dielectric and 400 µm via-to-via spacing *f)* four-layer structure with 900 µm via-to-via spacing *g)* four-layer structure with 400 µm via-to-via spacing

Statutory Declaration

I,

Family Name, First Name: Cao, Jimin,
Matriculation number: [redacted]

hereby formally declare that I have written the submitted thesis “Design of an RF-power amplifier and optimization of the thermal properties” independently. I did not use any outside support except for the quoted literature and other sources mentioned in the thesis.
I clearly marked and separately listed all of the literature and all of the other sources which I employed when producing this academic thesis, either literally or in content. The thesis in the same or similar form has not been submitted to any examination body and has not been published. This thesis was not yet, even in part, used in another examination or as a course performance.

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