Development of a MEMS Technology for the Monolithic Post-CMOS Integration of Capacitive Pressure Sensors

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Abstract

This thesis deals with the development, fabrication and characterisation of CMOS-compatible pressure sensor diaphragms. The approach of the post-CMOS integration of MEMS is adopted, which allows for monolithic fabrication of sensors above integrated CMOS circuits on silicon wafers. The overall objective is to reduce the pressure sensor geometry while simultaneously increasing the functionality of the electronics which is associated with the integration density of the CMOS technology. With such a separation of MEMS and CMOS circuits, standard CMOS foundries can be utilised to fabricate the CMOS wafers, thus, even more efficient technologies can be adapted in the future.

Essential challenges in the fabrication of post-CMOS pressure sensor elements are on the one hand caused by a temperature limit of about 400 °C which is necessary for maintaining the properties of CMOS circuits and prevents the use of typical MEMS materials like poly-Si. On the other hand, there are challenges related to sacrificial layer technology, such as the avoidance of sticking, the protection of CMOS circuits and the sealing of diaphragms.

The developed technology enables the process-independent adaptation of the pressure measuring ranges of capacitive pressure sensors by varying the diaphragm diameter. The targeted pressure ranges require highly sensitive pressure sensing elements with diameters from 100 µm to 300 µm and diaphragm thicknesses between 0.5 µm and 1.5 µm determined by modelling.

An appropriate process control based on a sacrificial layer technology released with vapour phase etching, and methods of surface micromachining could be successfully validated on diaphragms up to 300 µm diameter. The diaphragms consist of boron-doped PECVD SiGe and undoped CVD SiGe and have high sensitivities of up to 14 nm/hPa. The application of intense mechanical and thermal stress has showed a remarkable reliability. For these diaphragms, a gas permeability of about $8 \times 10^{-20}\,\mathrm{m^2/s}$ was determined with leakage tests using He.

The developed technology enables the CMOS-compatible fabrication of SiGe diaphragms for the use in capacitive pressure sensors.

Zusammenfassung

Die vorliegende Arbeit zeigt die Entwicklung, Herstellung und Charakterisierung von CMOS-kompatiblen Drucksensor-Membranen. Es wird der Ansatz der post-CMOS Integration von MEMS verfolgt, welcher die monolithische Fertigung von Sensoren oberhalb von CMOS Schaltkreisen auf Silicium-Wafern ermöglichen soll. Das Übergeordnete Ziel liegt in der Reduzierung der Drucksensorgeometrie bei gleichzeitiger Erhöhung der Funktionalität der Elektronik, welche mit der Integrationsdichte der CMOS Technologie einhergeht. Einhergehend mit einer solchen Separierung von MEMS und CMOS Schaltkreisen können zukünftig noch leistungsfähigere Technologien adaptiert werden.

Wesentliche Herausforderungen in der Herstellung von post-CMOS Drucksensorelementen sind zum einen bedingt durch eine Temperaturobergrenze von etwa 400 °C, welche zur Erhaltung der Eigenschaften von CMOS Schaltkreisen erforderlich ist und den Einsatz typischer MEMS Materialien wie poly-Si verhindert. Zum anderen sind Herausforderungen mit Bezug zur Opferschichttechnologie zu nennen, wozu die Vermeidung von Sticking, der Schutz von CMOS Schaltkreisen sowie die Verschließbarkeit von Membranen zählen.

Die entwickelte Technologie ermöglicht die prozessunabhängige Anpassung der Druckmessbereiche von kapazitiven Drucksensoren durch eine Variation der Membrandurchmesser. Die anvisierten Druckmessbereiche erfordern hochsensitive Drucksensorelemente mit Durchmessern von 100 µm bis 300 µm und Membrandicken zwischen 0.5 µm und 1.5 µm, die durch Modellierung ermittelt wurden.

Eine geeignete Prozessführung basierend auf einer Opferschichttechnologie mit Gasphasenätzen und Verfahren der Oberflächenmikromechanik konnte erfolgreich anhand von Membranen mit bis zu 300 µm Durchmesser validiert werden. Die Membranen bestehen aus dotiertem PECVD SiGe und undotiertem CVD SiGe und weisen hohe Sensitivitäten von bis zu 14 nm/hPa auf. Durch intensive mechanische und thermische Stressbeanspruchung konnte eine bemerkenswerte Zuverlässigkeit festgestellt werden. He-Dichtigkeitsprüfungen der verschlossenen Membranen lassen auf eine Gaspermeabilität von $8 \times 10^{-20}\,\mathrm{m^2/s}$ schließen.

Die entwickelte Technologie ermöglicht somit die CMOS-kompatible Fertigung von SiGe Membranen für den Einsatz in kapazitiven Drucksensoren.

CONTENTS

List of Symbols and Acronyms

List of Acronyms

3**DSiC**	**3−D**imensional **S**tacked **i**ntegrated **C**ircuit
ALD	**A**tomic **L**ayer **D**eposition
AMAT	***A**pplied **Mat**erials*
BAP	**B**arometric **A**bsolute **P**ressure
BPSG	**B**oro**p**hospho**s**ilicate **G**lass
BHF	**B**uffered **H**ydro**F**luoric acid
CAGR	**C**ompound **A**nnual **G**rowth **R**ate
C2D	**C**apacitance to **D**igital converter
C2V	**C**apacitance to **V**oltage converter
C2W	**C**hip to **W**afer
CAP	**cap**acitive
CLCC44	44 pad **C**eramic **L**eaded **C**hip **C**arrier
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CMP	**C**hemical **M**echanical **P**olishing
CPP	**C**ontact **P**ressure **P**oint
CTE	**C**oefficient of **T**hermal **E**xpansion
CVD	**C**hemical **V**apour **D**eposition
DR	**D**ynamic **R**ange
EEPROM	**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory
EGR	**E**xhaust **G**as **R**ecirculation
FSO	**F**ull **S**cale **O**utput
FOM	**F**igure **O**f **M**erit
HVAC	**H**igh **vac**uum

IC	**I**ntegrated-**C**ircuit
ICP	**I**nductively **C**oupled **P**lasma
IMD	**I**nter-**M**etal **D**ielectric
KGD	**K**nown **G**ood **D**ie
LPCVD	**L**ow **P**ressure **C**hemical **V**apour **D**eposition
MEMS	**M**icro **E**lectro **M**echanical **S**ystem
MAP	**M**anifold-**A**ir **P**ressure
NTGF	**N**ormalised **T**otal **G**as **F**low
OPS	**O**il **P**ressure **S**ensor
PECVD	**P**lasma-**E**nhanced **C**hemical **V**apour **D**eposition
PSG	**P**hosphorus **S**ilicate **G**las
PVD	**P**hysical **V**apour **D**eposition
PZR	**p**ie**z**o**r**esistive
RF	**R**adio **F**requency
ROIC	**R**ead **O**ut **I**ntegrated **C**ircuit
SACVD	**S**ub-**A**tmospheric **C**hemical **V**apour **D**eposition
SiP	**S**ystem-**I**n **P**ackage
SNR	**S**ignal to **N**oise **R**atio
SoC	**S**ystem-**O**n-**C**hip
TSV	**T**hrough-**S**ilicon **V**ias
TPMS	**T**yre **P**ressure **M**onitoring **S**ystems
TCS	**T**emperature **C**oefficient of **S**ensitivity
TCO	**T**emperature **C**oefficient of **O**ffset
USG	**U**ndoped **S**ilicate **G**lass
vHF	**V**apour **H**ydro **F**luoric acid
VIP	**V**acuum **I**nsulation **P**anels
W2W	**W**afer to **W**afer

Symbols

A	Area
BW	Bandwidth
C_{n-c}	Capacitance in non-contact mode
C_c	Capacitance in contact mode
C_{iso}	Capacitance of electrodes separated by an isolation layer
d	cavity height
d_{ea}	Diameter of etch access channels
E	Young's modulus
ϵ_0	Absolute permittivity
ϵ_r	Relative permittivity
F	Force
f	focus
I_n and J_n	Bessel functions of order n
K	Gas permeability coefficient
κ	Gas permeability coefficient for a normalised pressure difference of 1013 hPa
k_B	Boltzmann constant
ν	Poisson ratio
l_e	Edge length
$NTGF$	(total gas flow)/(1364 sccm)
ω_0	Resonant frequency
P	Pressure
P_b	Bombing pressure during in leak test
P_{cav}	Pressure inside the cavity
P_{CPP}	Pressure for contact pressure point
p_n	Noise equivalent pressure
Q	Mechanical quality of the diaphragm resonance
R	Universal gas constant
R^2	Coefficient of determination
R_0	Nominal resistance
r_0	Nominal radius

$R_{\mathrm{GeH_4}}$	(Flowrate GeH_4)/(Flowrate GeH_4+Flowrate SiH_4)
R_{PZR}	Equivalent resistor of a resistor bridge
r_{n-c}	Diaphragm radius not in contact with bottom electrode
Res_{CAP}	Resolvable change of a capacitive pressure sensor
Res_{PZR}	Resolvable change of a piezoresistive pressure sensor
S	Sensitivity
σ_i	Intrinsic stress
$\acute{\sigma_i}$	Dimensionless intrinsic stress
t_{cap}	Thickness of diaphragm cover layer
t_{cavity}	Thickness of deposition in diaphragm cavity
t_{bottom}	Thickness of deposition at the bottom of a diaphragm cavity
t_{iso}	Thickness of an isolation layer
V_{cav}	Volume of a cavity
V_{out}	Output voltage
V_s	Source voltage
w	deflection
$w_{\sigma_i,c}$	Deflection due to intrinsic stress
w_{slit}	Width of circular segments

1 Introduction

This thesis describes the development of an absolute pressure sensor technology with respect to the co-integration of a **M**icro **E**lectro **M**echanical **S**ystem (MEMS) and **C**omplementary **M**etal **O**xide **S**emiconductor (CMOS) by methods of surface micromachining. The most common approaches of integrating MEMS and CMOS are compared. The question why capacitive is preferred to piezoresistive pressure sensing is addressed, also in consideration with measuring (ultra) low pressures. Some recent developments for capacitive pressure sensor systems in the field of medical applications are presented to discuss the demand for higher degrees of integration. The chapter concludes with the objectives of this thesis.

1.1 Motivation

The total MEMS market forecasts an ongoing growth from about 20 000 million units in 2016 to far more than 70 000 million units in 2022. Amongst others, MEMS pressure sensors hold a significant market share in this field. A **C**ompound **A**nnual **G**rowth **R**ate (CAGR) of more than 11 % for MEMS pressure sensors in units and 5 % in value, respectively, is predicted. [1]. The pressure sensor market can be divided into five application fields: automotive, consumer, medical and industrial, listed in a descending order due to the market shares. A forecast for the individual application fields is drawn in Figure 1.1.
In the field of automotive, MEMS pressure sensors are utilised for more than 18 applications. Here, **T**yre **P**ressure **M**onitoring **S**ystems (TPMS) drive the market volume. The industrial market, and recently the consumer market, use pressure sensors to improve positioning by more accurate information about the altitude. For example, they are used in wearables and smartphones to improve the accuracy of fitness/sports algorithms. Here, the number of integrated devices will probably increase most. In medical applications, moreover, MEMS sensors are increasingly

adopted because of the trend toward miniaturisation and portability [1].

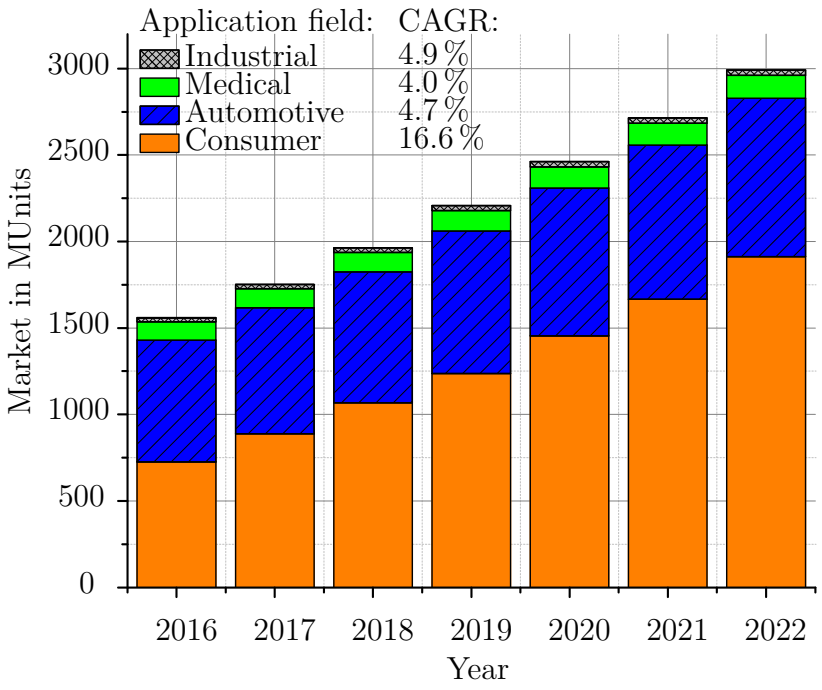


Figure 1.1: MEMS pressure sensor market forecast in units after [1].

As miniaturisation of standard CMOS devices is primarily limited due to costs, the idea of constructing **S**ystem-**O**n-**C**hip (SoC) solutions using monolithic MEMS and **I**ntegrated-**C**ircuit (IC) integration to extend the functionality of ICs by an additional dimension becomes more and more attractive. This alternative to Moore's law [2] is called 'more than Moore' [3–6]. Simultaneously, an increasing demand for highly integrated, miniaturised and multifunctional MEMS sensors can be observed throughout various fields, such as the automotive, medical devices, consumer electronic and industrial automation [7].
Amongst them, the fields of medical and industrial devices are identified as relatively vacant niche markets for pressure sensors. For example vacuum ranges are rarely addressed by miniaturised absolute pressure sensors. With vacuum, or ultra-low pressure, measurement is greatly needed in fields such as high-vacuum environment monitoring or process control [8–10]. In these fields, for example, an active or passive sensor-sensor-transponder system for the integration in a **V**acuum **I**nsulation **P**anels (VIP) represents an application of interest. Here, miniaturised, absolute pressure sensing and wireless communication through en-

capsulating environment are some of the primarily requirements.
The requirements of medical devices, especially medical implants, correspond to these. Additionally, implants show some of the highest demands regarding size or reliability. Any implantable system has to operate under challenging conditions inside the human body at about 37 °C potentially in contact with proteins, enzymes, cells, and ions. Long-term *in vivo* pressure monitoring is particularly demanding because the pressure sensitive part of the sensor must be in direct or indirect physical contact with the medium [11]. Because pressure is an important physiological parameter in medical diagnostics, highly miniaturised and low power consuming pressure sensors show high potential for the integration in medical applications such as implants. The monitoring of blood pressure for patients suffering from chronic heart insufficiency, hypertension, cranial pressure in the hydrocephalus, intra ocular pressure in glaucoma or bladder pressure in incontinence represent some of the recent aims in implant development [12–14]. The most important requirements of implantable pressure sensor systems are at the highest degree of miniaturisation for instance, to enable even more minimal invasiveness of medical pressure sensor implants or a more frequent use of catheter-tip pressure monitoring during hospitalisation [15], on-chip readout electronics and minimum power consumption to enable telemetric communication. Simultaneously, a high resolution in absolute pressure monitoring is beneficial as a pre-requirement to achieve required accuracies. Regarding miniaturisation, a first question is how it affects the sensor performance itself.

1.1.1 Scaling limits of diaphragm-based pressure sensors

Electromechanical pressure sensor devices can be fabricated by well known methods of IC fabrication [16]. For example to detect ambient pressure, different sensing techniques can be used, such as piezoresistive, capacitive, piezoelectric, optical or resonant sensing [17, 18]. All of these techniques show advantages and disadvantages. Amongst them, piezoresistive pressure sensors have become the most popular choice in various applications due to their small size, high sensitivity, low cost, and simple fabrication. These advantages have also paved the way for them to become the preferred choice in the commercial front [19, 20]. In the field of medical pressure sensor applications, the downsizing of the sensor diaphragms utilised for capacitive or piezoresistive sensor types has reached

a minimum in rectangle length and width or diameter in the order of 100 µm, as drawn in Figure 1.2. Sensors designed for barometric pressures in medical applications are considered.

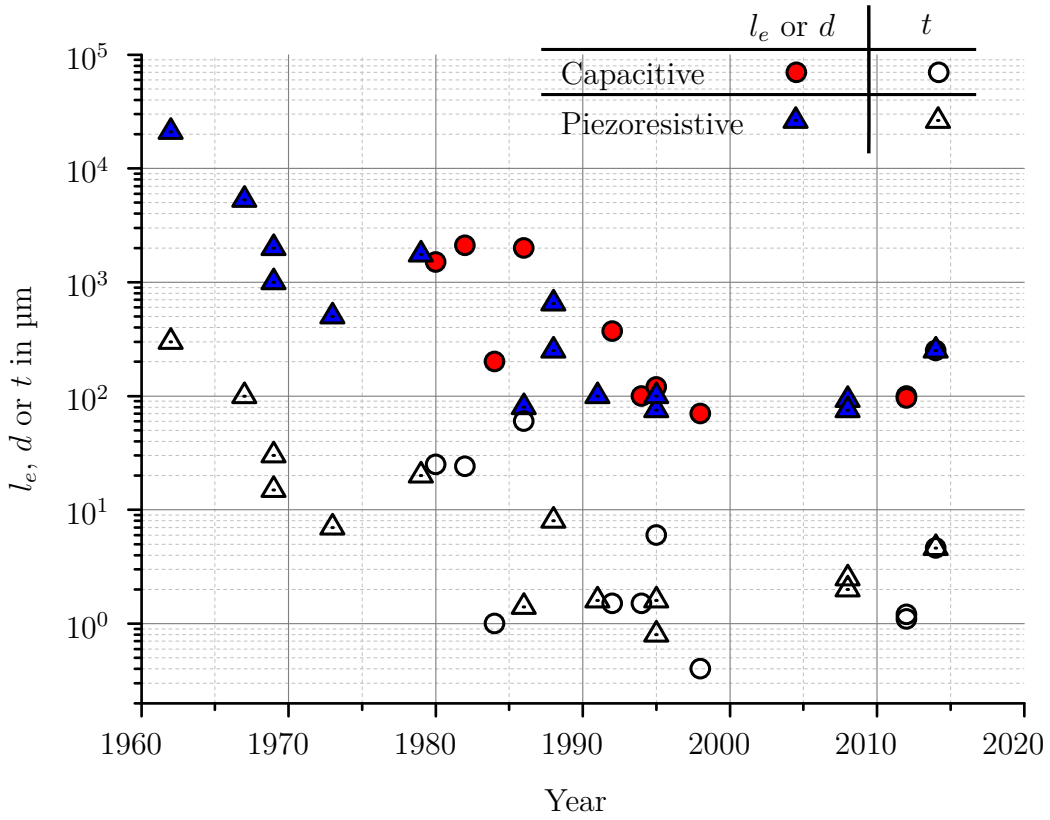


Figure 1.2: Evolution of the edge length l_e or the diameter d, respectively, and the thickness t of capacitive and piezoresistive pressure sensors designed as absolute pressure sensors for implantation as medical device, corrected and continued after [15]. Details and references are listed in Table 1.1.

The ratio of the diaphragm edge length l_e or diameter d over the diaphragm thickness t is relatively stable at 80 : 1. This ratio is, amongst other reasons, limited due to stretching effects under deflection, which introduces non-linear behaviour.

In Table 1.1 the geometric evolution of diaphragm characteristics of **cap**acitive (CAP) and **p**ie**z**o**r**esistive (PZR) pressure sensors are summarised after [15].

Moreover, the scaling limits of the capacitive and the piezoresistive sensing method reveal some advantages and disadvantages of both. The scaling for capacitive sensing is predominantly limited by a rapidly decreasing effective change in ca-

pacitance, which becomes hardly resolvable in magnitudes of few fF. Therefore, capacitive sensors with diaphragms in the magnitude of 100 µm in diameter d or edge length l_e usually require many single diaphragms arranged in arrays to increase the effective sensing capacitance [21]. Contrary to capacitive sensing, piezoresistive sensing is less sensitive with the downsizing, thus single diaphragms are sufficient [17, 22].

Table 1.1: Evolution of CAP and PZR pressure sensors designed for medical implantation, corrected and continued after [15].

Year	Method of Micromachining	Sensor Type	Material	l_e or d in µm	t in µm	Ratio l_e or d/t	Reference
1962	Early	PZR	Mono−Si	21000	300	70	[23]
1963	Early	PZR	Mono−Si	2250	–	–	[24]
1966	Early	PZR	Ti	5300	100	53	[25]
1969	Bulk	PZR	Mono−Si	2000	30	67	[26]
1969	Bulk	PZR	Mono−Si	1000	15	67	[26]
1973	Bulk	PZR	Mono−Si	500	7	71	[27]
1979	Bulk	PZR	Mono−Si	1750	20	88	[28]
1980	Bulk	CAP	Mono−Si	1500	25	60	[29]
1982	Bulk	CAP	Mono−Si	2100	24	88	[30]
1984	Surface	CAP+PRZ	Poly−Si	200	1.0	200	[31]
1986	Surface	CAP	Si_3N_4	80	1.4	57	[32]
1986	Bulk	CAP	Mono−Si	2000	60	33	[33]
1988	Bulk	PZR	Mono−Si	650	8	81	[34]
1988	Bulk	PZR	Mono−Si	250	–	–	[34]
1991	Surface	PZR	Si_3N_4	100	1.6	63	[35]
1992	Bulk	CAP	Mono−Si	370	1.5	247	[36]
1994	Surface	CAP	Poly−Si	96	1.1	67	[37]
1995	Surface	CAP	SiO_2	120	6	20	[21]
1995	Surface	PZR	Si_3N_4	75	0.8	94	[17]
1998	Surface	PZR	Various Si stack	100	1.6	63	[18]
1998	Surface	PZR	Poly−Si	103	–	–	[22]
1998	Surface	CAP	Poly−Si	70	0.4	175	[38]
2008	Bulk	PZR	Mono−Si	92	2.5	37	[39]
2008	Surface	CAP	Poly−Si	75	2	38	[40]
2012	Surface	CAP	Poly−Si	96	1.1	87	[41]
2012	Surface	CAP	Poly−SiGe	100	1.2	83	[42]
2014	Surface	CAP+PRZ	Poly−SiGe	250	4.6	54	[43]

However, piezoresistive sensor types with minimal diaphragm areas suffer from

serious stress effects and relatively large offsets and drifts [44]. Here, perfect resistor matching and an almost perfect temperature compensation are required. Further, in piezoresistive sensing a limitation of the thickness is given by the junction depth of the resistor wells placed at the edges of a diaphragm. A scaling of the diaphragm thickness t below 1 µm is therefore critical.
The achievable resolution for pressure sensors is limited due to fundamental noise, which primarily depends on the compensation and **R**ead **O**ut **I**ntegrated **C**ircuit (ROIC) [44]. Some kinds of noise are related to piezoresistive pressure sensors, which can be separated into Brownian noise, thermal noise, flicker noise and circuit noise. Here, flicker and thermal noise represent the decisive limits with regard to the achievable resolution. According to an empirical $1/f$ noise model [45], high resolution as a consequence of reduced noise is achievable by high doping and long annealing at higher temperatures [20].
Despite the disadvantage in linearity, the capacitive sensing method is therefore more attractive for a number of applications that require highly sensitive pressure sensors. Regarding the required miniaturisation, factors other than large sensor arrays are sources of additional bulk elements: bonding pads, the area of an on-chip ROIC, required support thickness or unused space on the perimeter of the chip.

1.1.2 Hybrid or monolithic integration?

A further miniaturisation can either be achieved by monolithic or by hybrid integration of MEMS and CMOS. Both show advantages and disadvantages. The monolithically integrated surface micromachined capacitive pressure sensor technology can be classified as intermediate MEMS and CMOS processing. Here, MEMS and CMOS areas are placed side by side. This integration method enables single-chip solutions with all functions integrated on one device. A major advantage is a minimised open interface area exposed to assembling and encapsulation materials. Parasitic electrical effects, for example due to bond-wires to connect MEMS and CMOS, are minimised.
Unfortunately, despite highly miniaturised sensor diameters in the magnitude of 100 µm arranged in arrays of sensing and reference elements, the total chip areas remain relatively large, for example in the magnitude of 0.7 mm x 5.6 mm with an

area consumption of the diaphragms of about 30 % [13,41,46]. Since the reported monolithic integration is established for a standard CMOS technology with a relatively large minimal structure width of 1.2 µm, the CMOS area is relatively large for the given examples. A further disadvantage is an increased current consumption due to 1.2 µm CMOS. This sensor system is presented in Figure 1.3 a. as an example.

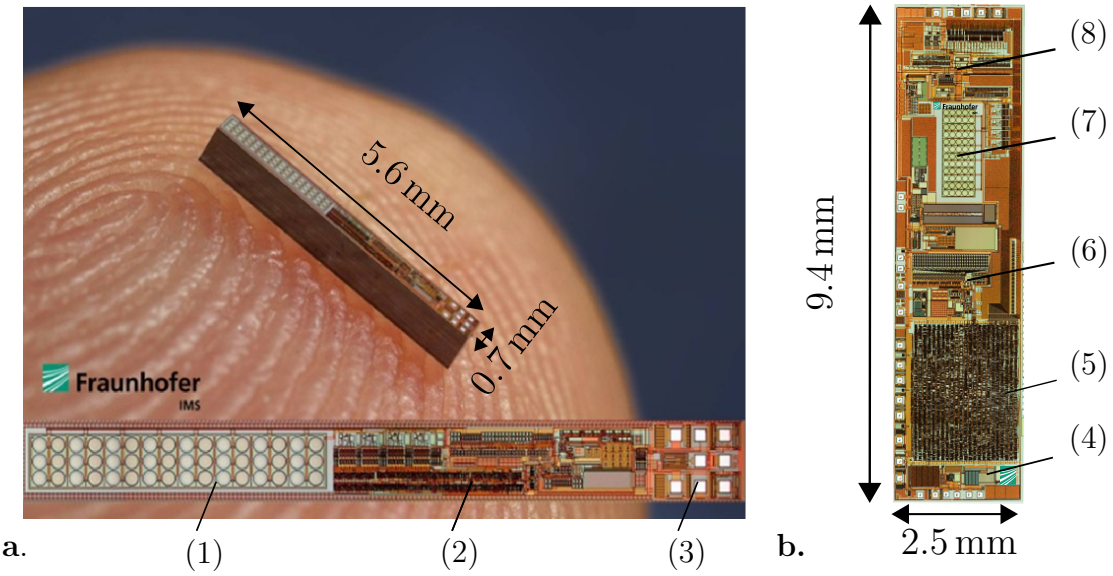


Figure 1.3: Two examples for monolithic intermediate integration as duo-device and mono-device, designed for the integration into implantable systems: a. absolute capacitive pressure sensor system developed for wireless monitoring of hypertension patients placed on a finger tip to show the shares in area of diaphragms (1), CMOS-ROIC (2) and interface (3) to an additional communication ASIC (not shown), after [13, 41]; b. comprises parts for wireless communication (4), digital logic (5), EEPROM (6), diaphragms (7) and C2D circuitry (8) all in one device. [47, 48].

In Figure 1.3 b. another implantable sensor system to measure liquor pressure of a ventricular drainage system is shown [47, 48]. This example represents a passive pressure sensor transponder with all functions completely integrated in a monolithic device system. The functions comprise of a wireless communication front-end (4), a digital logic (5), an **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory (EEPROM) (6), diaphragms (7) and a **C**apacitance to **D**igital converter (C2D) circuitry (8). Here, the pressure sensor diaphragm area is less than 7 %. In contrast, the example presented in Figure 1.3 a. requires an additional ASIC for wireless communication, which is not shown here.

Unfortunately a monolithic intermediate MEMS integration is linked to the CMOS technology for which it is developed. Thus, each time smaller CMOS technologies are desired to be used for monolithic intermediate MEMS integration, immense development expenses arise. Although the fabrication can rely on standard CMOS processes, the fabrication flows are affected by some limitations due to MEMS specific metrology, handling restrictions, or a reduced variety of further applicable process steps once some MEMS processes are applied.
More flexibility regarding the CMOS technology is granted by hybrid integration. A separation of CMOS and MEMS to different die levels enables a fabrication by independent technologies. More advanced CMOS technologies can be used for the fabrication of the ROIC to reduce the CMOS area while improving performance. This is sketched in Figure 1.4.

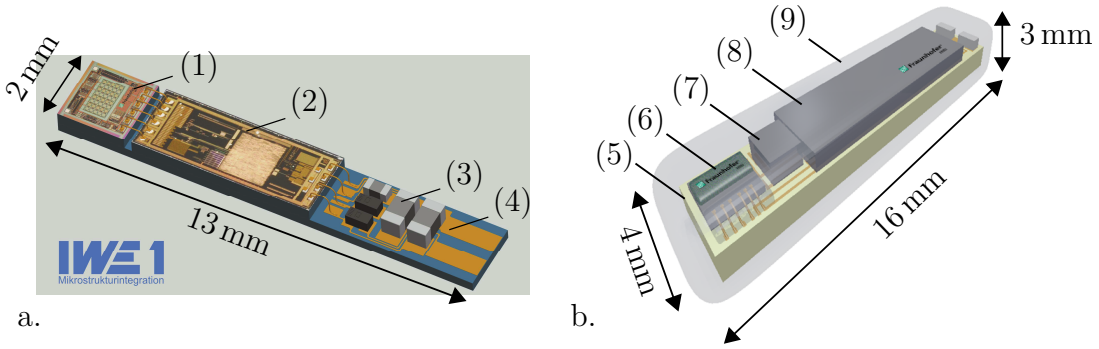


Figure 1.4: Two examples for hybrid integration of implantable absolute capacitive pressure sensor systems: a. A pressure sensor with integrated C2V (1) and ROIC (2) connected with wire bonds, both plus some discrete components (3) mounted on an interposer (4) [49]. A third interface ASIC for communication is not shown. b. A schematic of a highly integrated, encapsulated multi sensor implant. An interposer with integrated antenna (5) carries a pressure sensor with integrated C2V (6), an accelerometer MEMS (7), and an 350 nm CMOS ASIC (8) for signal conditioning of several sensors and wireless communication. The encapsulation of the whole system is also indicated (9), after [50].

In each a. and b., a pressure sensor MEMS with integrated **C**apacitance to **V**oltage converter (C2V) fabricated in a 1.2 µm CMOS technology is wire-bonded to an ASIC fabricated in a 350 nm standard CMOS technology. The implantable pressure sensor system shown in Figure 1.4 a. includes another interface ASIC for wireless communication apart from the implant position[1]. However, the approach

[1]pulmonary artery pressure in patients with heart insufficiency

in Figure 1.4 b. is more functional. Here, more sensor functions are included (accelerometer and others [50]) and the communication interface is also integrated in the present ROIC, as well as an antenna in the interposer.
In Table 1.2 the effective ASIC areas are presented for some monolithically and hybrid integrated pressure sensor systems for medical applications. From Table 1.2 the trend can be observed that the total ASIC area is increasing, since even more functions are added to the system. Even though if smaller technologies are utilised for ROICs in hybrid solutions, as shown in Figure 1.4 b., a large area is consumed by the ROIC. In this example, the ROIC is equipped with interfaces for signal conditioning of several sensors and wireless communication and, thus, consumes about 24 mm^2. In contrast to miniaturisation demands, also the pressure sensor area continuously consumes a significant share. Both observations enhance the demands for integration approaches, which enable an increase of functionality and sensitivity on the one hand, but also support an ongoing miniaturisation of pressure sensor systems on the other.
Thus the disadvantageous need of increasing area consumption of highly integrated ROICs may be turned into an advantage. Using most of this area for pressure sensor diaphragms would lead to an increased effective capacitive change, thus higher resolution can be achieved [2].

Table 1.2: Cumulated areas of capacitive pressure sensor and ROIC systems in relation to the effective diaphragm area of some devices or systems, respectively.

Year	Integration of pressure sensor and ROIC	CMOS technology in µm	Total area of ASIC in mm^2	Pressure sensor area in mm^2	Reference
1994	monolithic	3.0	4.9	0.6	[37]
2000	monolithic	1.2	9.0	0.3	[51, 52]
2008	hybrid	n.A.	0.7	0.3	[40]
2011	monolithic	1.2	6.8	0.2	[13]
2011	hybrid	0.35	12.2	0.9	[49]
2012	monolithic	1.2	3.9	1.2	[41]
2014	monolithic	1.2	23.5	1.6	[47, 48]
2017	hybrid	0.35	27.2	0.9	[50]

[2] If the ROIC shown in Figure 1.4 b. is fabricated in a 150 nm technology instead of 350 nm an area of approx. 8 mm^2 can be covered by pressure sensitive diaphragms due to calculations with assumed scaling factors of $\frac{1}{4}$ for digital parts, $\frac{1}{2}$ for analog parts and $\frac{1}{3}$ for capacitors.

To minimise any extra area required for the MEMS, 3D integration can be chosen. The MEMS is thought to be placed on top of the CMOS level, or vice versa. In hybrid MEMS integration, usually single MEMS are stacked on CMOS dies, either on wafer or on die level.
One method of choice is for example **S**ystem-**I**n **P**ackage (SiP). Via SiP multiple bare dies are vertically stacked and interconnected by means of wire-bonding. A more advanced hybrid integration is **3−D**imensional **S**tacked **i**ntegrated **C**ircuit (3DSiC). Here, **T**hrough-**S**ilicon **V**ias (TSV) are used instead of wires and thus save extra space. Moreover, extra area could be used for sensors, since the CMOS areas are mostly larger than the sensing areas.
In Figure 1.5, two examples for 3DSiC are shown. In Figure 1.5 a. a single *BOSCH BMP* 280 is shown. An opened sensor package (1) reveals a pressure sensor diaphragm with piezoresistive elements at the top level (2). The cross section (3) shows the 3-level stacking with a CMOS-ROIC, which is mounted via flip-chip technology at the bottom level. The MEMS and ROIC are connected with wire bonds from the top of the MEMS layer to the carrier. In b., a multilayer TSV 3D integrated TPMS is shown. This consists of a pressure sensor (4) and its microcontroller-ASIC (5, *here: wafer level*), whereas a communication block comprises a bulk acoustic resonator plus an antenna (6) and a transceiver ASIC (7) [53].

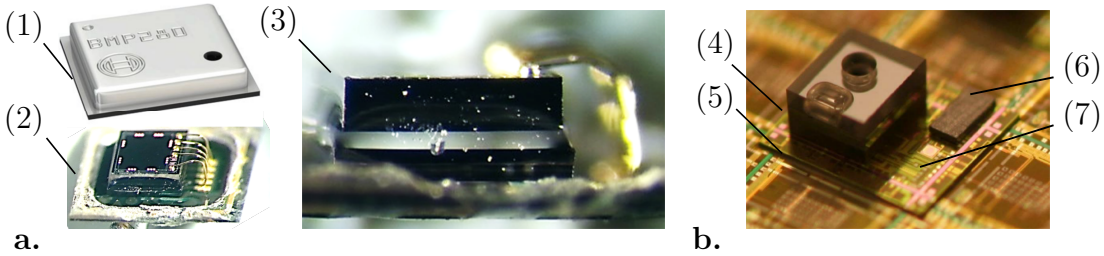


Figure 1.5: a. Photos of an encapsulated (1) and opened (2) pressure sensor by *BOSCH*, connected via flip-chip and bond-wires (3) on an interface board. b. Photo of a 3D integrated TPMS by the use of TSV on wafer level [53]

However, 3D integration via TSV involves component and system designs, packaging assembly and testing, material suppliers, and equipment suppliers. The key enabling technologies for 3D IC integration are, amongst others, electrical, thermal, and mechanical designs and tests, **K**nown **G**ood **D**ie (KGD), TSV forming and filling, wafer thinning and handling, thin-chip strength mea-

surement and improving, lead-free microbump forming and assembly, low temperature **C**hip to **W**afer (C2W), or even **W**afer to **W**afer (W2W) bonding, and thermal management [54]. In summary, the 3D integration methods inevitably generate significant increases in system heights and assembling efforts.
Finally, the total size of any (implantable) system is directly linked to the total packaging size with special requirements regarding biocompatibility and -stability, as well as long term stability of the pressure sensor. Usually, thick-walled metal- or ceramic housings are chosen, which show limits regarding a further implant miniaturisation [50]. Recently developed approaches for 3D encapsulation concepts utilise thin film **A**tomic **L**ayer **D**eposition (ALD) stacks to achieve, amongst others, biocompatibility and biostability [55–57]. These approaches would strongly benefit from a higher integration density, resulting in reduced areas, fewer materials of the exposed surfaces and a reduced number of interfaces on an implantable sensor system. In conclusion, taking the best of both hybrid and monolithic MEMS and CMOS integration would combine the advantageous characteristics:

- Monolithic integration on a single chip for best MEMS and CMOS connection can minimise the assembling efforts, the system heights, and parasitic effects due to any additional bond-wires or connections. The interface surface exposed to further encapsulation materials is therefore minimal.
- Separation of MEMS and CMOS process levels to independently fabricate the CMOS IC in any standard foundry and almost any technology without any limitations due to MEMS processes. This enables the integration of MEMS and even smaller technologies for CMOS, by which, for example, the current consumption can be minimised and the functionality can strongly be increased. The MEMS fabrication sequences rely on only few layers, thus a maximum flexibility is ensured. It will become very cost effective to design MEMS and CMOS integrations for specific applications. By one generic post-CMOS pressure sensor technology, both cost effective CMOS technologies for low cost applications as well as the highest degrees of integration on more advanced CMOS technologies will become possible.
- 3D integration of MEMS and CMOS for a maximum integration density and, thus, minimised total area. A neutralisation of diaphragm scaling

limits and sensor area issues to some magnitude is a consequence. Thus, higher resolution would become possible in capacitive sensing.

All these advantages can be combined with monolithic integration by methods of surface micromachining if MEMS processing will be applied post-CMOS.

1.2 Post-CMOS Integration of MEMS

There are at least the following methods to realise monolithic MEMS and electric circuit integration on the same substrate:

- Pre-CMOS (MEMS-first) processing.
- Intermediate MEMS and CMOS processing.
- Post-CMOS (MEMS-last) processing.

The first two methods obtain some disadvantages compared to the third. The first method inhibits a following standard CMOS fabrication flow, for example due to strict requirements on the surface planarity or material exposure. Amongst others, the method of intermediate MEMS and IC processing obtains limitations regarding the achievable integration density because MEMS and CMOS structures are placed side by side. MEMS on top of monolithically integrated CMOS structures (post-CMOS) allow a maximum integration density and thus a significant cost reduction. One of the main advantages is that standard CMOS foundries can be utilised to fabricate the CMOS wafers. However, the use of CMOS structures as a substrate raises several restrictions for a post-CMOS MEMS process, where the major limitation is the temperature which must stay below 400 °C [58]. There are some examples for the post-CMOS approach: a micromirror device [59], the electroplated ring gyroscope [60], an electroplated acceleration switch [61], or bolometers [62, 63].
These post-CMOS MEMS are fabricated by the use of sacrificial-layer etching. However, MEMS such as absolute pressure sensors show significant differences. With respect to a later sealing of cavities, the access areas to remove the sacrificial layer are much smaller. Further, the ratio of the sacrificial layer height to its width is very small, in the magnitude of 1 : 200, see for example [64]. Here, more demanding requirements regarding the sacrificial layer technology are

identified, such as a residual-free release etch. Either any residuals in the cavity may destroy the mechanical structures, which will hardly be removable due to much smaller cavities and dimensions of the etch accesses. Or the remaining products as residues could promote stiction of the functional layer and the substrate. Furthermore, the addressed geometries can have impact in the appearance of stiction [65]. The stiction of two surfaces is commonly thought to be caused by electrostatic forces, hydrogen bonding, and Van der Waals forces [66]. Among them, hydrogen bonding, which induces water's unique physical properties of relatively high boiling point/melting point and low density in ice, is much stronger than the other two kinds of force.

An attractive capillary force induced by fluids with a hydrophilic contact angle can lead to stiction as well [67]. For this reason, vapour-phase etching [68] is an appropriate technology to release free standing MEMS structures, because stiction can be avoided by controlling the amount of condensed liquid [69, 70]. Additional benefits are the etching in high aspect ratio regions, a highly reduced consumption of aggressive chemicals and improved uniformity [67]. Processing at reduced pressure was found to be beneficial due to a reduction in particles [71].

First steps in the field of post-CMOS pressure sensor developments have been reported [42, 72]. As addressed before, the question about capacitive or piezoresistive pressure sensing is worth being discussed in this context, too. The fabrication of piezoresistive structures usually requires high annealing temperatures. For example [43] reported that the piezoresistivity significantly decreases with decreasing process temperature and becomes relatively moderate. Therefore the capacitive method is assumed to be advantageous regarding the strict temperature limitations in post-CMOS processes. First evaluations of poly-SiGe diaphragm test structures (fabricated by the aid of an established intermediate-CMOS pressure sensor technology) show promising results regarding the mechanical properties under applied pressure. This previous developments have not yet been integrated in a post-CMOS process scheme.

1.3 Objectives of this thesis

The main goal of this work is the development of a technology to fabricate diaphragm-based, absolute MEMS pressure sensors in surface micromachining, which further enables post-CMOS processing. One major focus is to preserve full functionality of any CMOS substrate. Thus, low temperature budgets and protection of CMOS ICs from aggressive media is required. For this purpose, an appropriate protection depending on the sacrificial layer technology is developed in this thesis. Another major focus is to utilise vapour-phase etching as the method to release the sacrificial layer. This requires an appropriate design of etch-access channels of pressure sensitive diaphragms. The fabrication of diaphragms, which utilise capacitive sensing principle due to the improved suitability for highly sensitive applications, has to fulfil the temperature limitations in post-CMOS processing. Further, the diaphragms require completely closed and hermetic surfaces for the exposure in environments that differ from noble gases. The solutions known from the state of the art show general weaknesses, especially with respect to the described demands. Here, appropriate processes have to be developed and evaluated regarding the diaphragm characteristics and its hermeticity. At the aspired level of development an additional bond pad metal stack for wire bonds becomes necessary. This is required for electrical characterisation of discrete pressure sensor elements.

Important applications with a strong demand for miniaturisation of state-of-the-art MEMS pressure sensors are medical implants as outlined. However, more pressure ranges than around the atmospheric pressure shall be addressed by sensor design variations. Vacuum applications, for example, could be considered. Both fields require sensor-transponder systems for the integration/implantation at the monitor site. Further, absolute pressure monitoring is necessary for this kind of applications.

In summary, the fabrication of sensors for different pressure ranges enabled by design variations in a single generic technology is highly desired.

2 State of the Art

What exactly is pressure? Pressure (P) is expressed in Pascal (Pa) and is equal to an applied force F per area A:

$$P = \frac{F}{A} \left[\text{Pa} = \text{N/m}^2\right] \tag{2.1}$$

Equation 2.1 means that the existence of pressure requires at least one medium. In industrial or medical environments pressure is the effect of a force which can be applied onto a clamped area by a gas or a liquid, for example. And because pressure is equal to an applied force per area, it cannot be measured directly. In order to measure pressure indirectly, it is a good idea to detect the mechanical displacement. Pressure sensors are typically divided into three categories: gauge, differential/relative, and absolute. While in gauge pressure sensing the signal is referred to atmospheric pressure, differential pressure sensing compares two different pressures, which are usually applied to different sides of a diaphragm. In turn, the signal of absolute pressure sensors is referred to a vacuum, which is encapsulated by hermetically covering a cavity underneath a diaphragm.
Examples for traditional pressure sensors are a U-Tube manometer and a Bourdon Tube. In Figure 2.1 the principles and corresponding product realisations are shown for both. They have in common that the pressure-induced displacement is optically detected. While the U-Tube manometers became obsolete and are replaced by MEMS pressure sensors, the Bourdon Tube (Figure 2.1 d.) actually still plays an important role in ordinary pressure sensor issues. Because quartz is an almost perfectly elastic material, the Bourdon Tube transducers show lowest hysteresis, excellent repeatability, and long-term stability. Since an electrical output is more practical, *Ruska* designed a feedback-driven design to exploit the special properties of fused quartz to achieve unsurpassed precision of 0.003 % of full scale and stability to 0.005 % of reading over six months [73]. After a period of 50 years, fused-quartz Bourdon Tubes by *Ruska* are for instance still required

in high-precision pressure controllers used for calibration [74, 75].

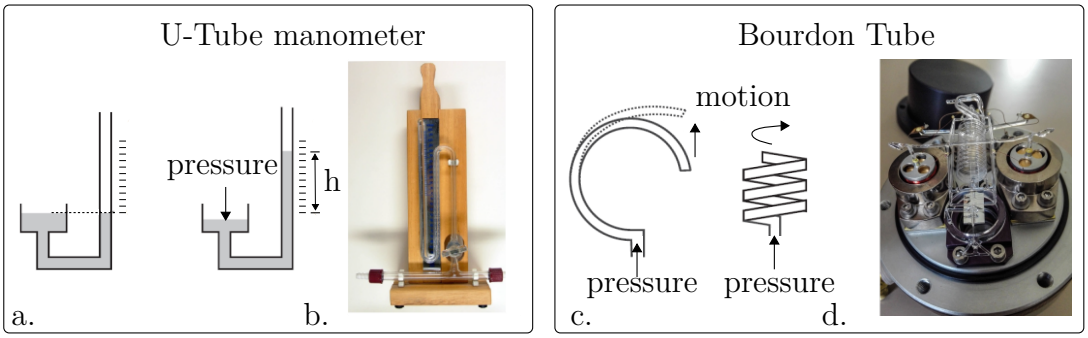


Figure 2.1: Examples of traditional pressure sensors with optical output, a. principle and b. realisation of a U-Tube manometer [76], c. principle and d. product realisation of a fused-quartz Bourdon Tube by *Ruska*.

2.1 Silicon-Based Absolute Pressure Sensors

Analogous to the success of quartz for macroscopic sensors, single-crystal silicon (Si) has been the material of choice for MEMS pressure sensors in the past 5 decades. Due to their main advantages in mechanical and electrical properties [77], most MEMS pressure sensors have been realised with silicon. In Table 2.1 the major fields are listed with some exemplary applications, which all have in common a high demand for miniaturisation.

In these main fields, piezoresistive and capacitive pressure sensors represent the vast majority of micromachined devices. The essential feature of most micromachined pressure sensors is an edge-supported diaphragm that deflects as a result of different pressure loads. This deflection can be detected by measuring either the stresses in the diaphragm, or the displacement of the diaphragm, or both. The stress can be measured by piezoresistors formed at the maximum stress locations of the diaphragm. The deflection, in turn, can be measured as a change in capacitance, if an electrode is located on a substrate with some distance to the diaphragm.

The field of Si-based pressure sensors can further be diversified into bulk and surface micromachining. As outlined in the motivation, this thesis is confined to surface micromachined diaphragm-based pressure sensors. Thanks to advantages such as a maximum integration density, highest degrees of miniaturisation

or minimisation of parasitics, surface micromachining is a prerequisite to enable post-CMOS pressure sensor fabrication. In order to further narrow down the topic barometric pressure ranges of about 1000 hPa ± approximately 500 hPa, and vacuum ranges down to 1 Pa are aimed at. In this chapter state-of-the-art pressure sensors from these categories and for the addressed pressure ranges are briefly introduced to present a general overview. The scaling and resolution limits of capacitive and piezoresistive sensing methods are discussed.

Table 2.1: Present and future applications for MEMS pressure sensors.

Field	Example Applications
Consumer	Altimeters, weather stations, quantify self-monitoring
Automotive	**M**anifold-**A**ir **P**ressure (MAP), **B**arometric **A**bsolute **P**ressure (BAP), TPMS, Dynamic Brake Control, **H**igh **vac**uum (HVAC) fans and hydraulics, fuel tank vapor, turbo boost, secondary air valve, **E**xhaust **G**as **R**ecirculation (EGR), fuel rail, **O**il **P**ressure **S**ensor (OPS), vacuum brake booster, oil transmission, side airbags, pedestrian protection, pinch protection, others
Medical	Intraoccular (Glaucoma), Cranial (Hydrocephalus), Blood (Hypertension, chronic heart insufficiency), Bladder (Incontinence) Catheters (Angioplasty), others
Industrial	Thermal Insulation Panels, HVAC sensors

2.1.1 Piezoresistive Pressure Sensors

MEMS piezoresistive pressure sensors usually have a diaphragm and use a Wheatstone bridge circuit formed by piezoresistors located on the diaphragm, as shown in Figure 2.2. An applied force induces a diaphragm deflection (a.), which causes a well-known stress distribution across the diaphragm as sketched in b.. At these positions the piezoresistors are placed to obtain the maximum output signal (c. and d.), which depends strongly on the direction of the applied force relative to the crystal orientation. The configuration as a Wheatstone bridge (e.) enables the detection of a ΔR terms in relation to R_0, which is desired to be equal for all the piezoresistors.

This configuration is a very accurate method to precisely measure the resistance values. By applying a source voltage V_s, the output voltage V_{out} correlates as

stated in Equation 2.2:

$$V_{out} \approx \frac{(\Delta R_1 + \Delta R_3) - (\Delta R_2 + \Delta R_4)}{4R_0} \cdot V_s. \tag{2.2}$$

This circuitry provides a 1st order temperature-compensated output. Nevertheless, these kind of pressure sensors are highly temperature-dependent and thus require compensation circuits and calibration over temperature. The output delivers an almost linear response for small deflections.

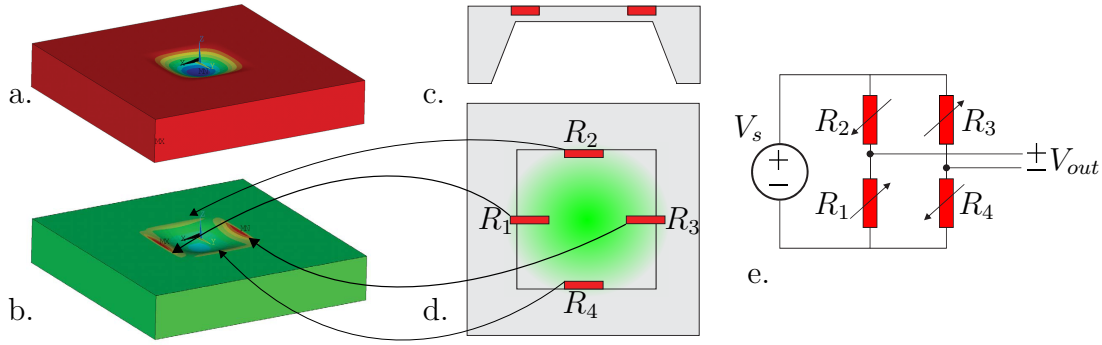


Figure 2.2: Typical configurations of piezoresistors on pressure sensitive diaphragm: a. shows the deflection in z and b. the resulting stress in x direction, which affects the piezoresistors placed at the point of maximum stress (cross-section c., top view d.); e. shows a full bridge configuration, after [78].

2.1.2 Capacitive Pressure Sensors

Capacitive pressure sensors are attractive for many applications because the device performance is tolerant against contact resistance variations. Additionally, wireless sensing schemes can be readily realised to eliminate any potential performance degradation due to wiring parasitic capacitances. These are possible even for high temperature ranges [79–81]. Furthermore, capacitive devices can achieve a high sensitivity, low turn-on temperature drift, and a minimum dependence on side stress and other environmental variations [82].

An ideal capacitive sensor is a parallel plate capacitor, where the distance and the dielectric constant of the medium between the plates are the main factors that define the value of the capacitance. The effect of variation of the dielectric constant is used in many applications, especially in the field of chemical engineering. In this thesis capacitive sensors are developed, which operate on the principle of variation in capacitance due to the change in the distance between the electrodes.

Equation 2.3 shows that the capacitance of a parallel plate capacitor is inversely proportional to the distance between its electrodes.

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d}. \tag{2.3}$$

Here, A is the surface area of the electrodes, d is the distance between the electrodes, ϵ_0 and ϵ_r are the absolute and relative permittivity of vacuum and air, respectively. This inverse proportionality serves as the main principle of operation for inertial MEMS sensors like accelerometers and pressure sensors. Application of force in the form of acceleration or pressure changes the distance between the electrodes of the capacitor. This changes the capacitance between the electrodes inversely. A classification of capacitive pressure sensors is possible by two operation modes: a non-contact and a contact mode. A typical output characteristic for a wide pressure range shows the different regions in Figure 2.3. The transition describes a small pressure range around the **C**ontact **P**ressure **P**oint (CPP). For very large pressures, if even more deflection is hardly possible, the sensor goes into saturation.

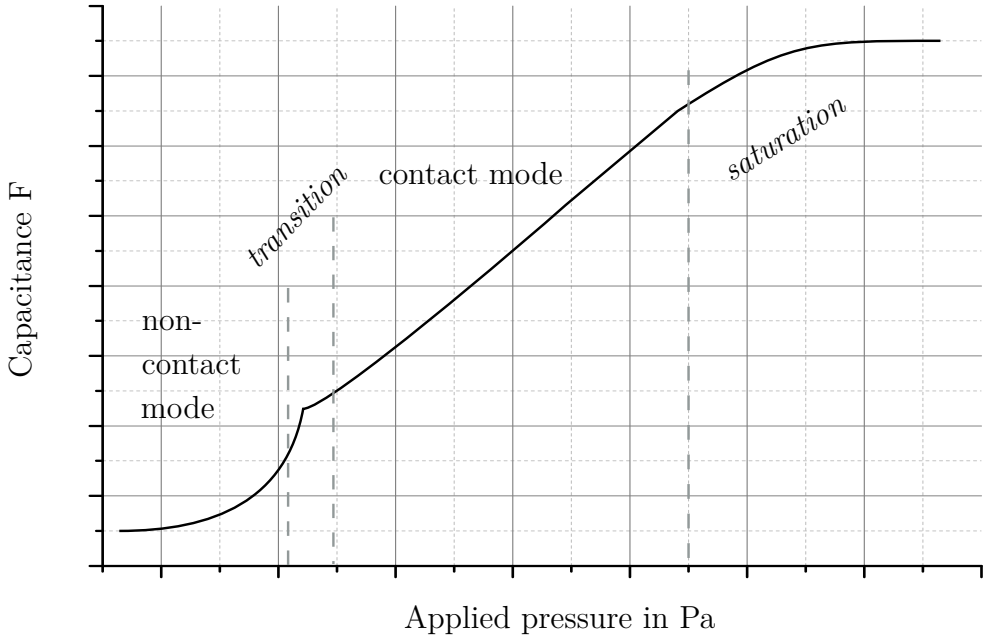


Figure 2.3: Schematic sketch of typical capacitance to pressure characteristic of a capacitive pressure sensor with two operation modes: non-contact (normal), and contact (touch). A transition and saturation region are also characteristic, after [83].

2.1.3 Diaphragms and Performance Characteristics

As introduced, both the piezoresistive and the capacitive approach for pressure sensing require diaphragms which are pressure sensitive. In this chapter, some fundamentals regarding diaphragm characteristics and noise mechanisms are introduced, which are further needed for simulation and pressure sensor evaluation.

Diaphragm Deflection

An appropriate description of the deflection line of pressure sensor diaphragms is a prerequisite e.g. for the design and electrical simulation of integrated capacitive pressure sensors. Uniformly loaded circular-shaped diaphragms are described by the radius r_0 and the thickness t. The mechanical properties of the diaphragms are characterised by isotropic Young's modulus E and the Poisson ratio ν. The deflection w is described as a function of the radial coordinate r and the pressure load P under pure bending condition as a differential equation [84]:

$$D\nabla^2\nabla^2 w = P, \tag{2.4}$$

where the flexural rigidity of the diaphragm D is given by

$$D = \frac{E \cdot t^3}{12(1-\nu^2)}. \tag{2.5}$$

Operation in Non-Contact Mode In the non-contact mode, also called normal mode, the diaphragm is freely movable in z-direction and only limited by the clamping of the edges. For pressure sensors with circular-shaped and rigidly clamped diaphragms, the deflection w is a radius-dependent quantity which can be obtained after solving Equation 2.4 [84]:

$$w(r, r_0, P) = \frac{\Delta P}{64D} \cdot \left[r_0^2 - r^2\right]^2. \tag{2.6}$$

Here, r_0 is the radius of the diaphragm, r is the radial coordinate. In Figure 2.4, all used symbols are drawn in the sketch of a rigidly clamped diaphragm, whose top surface is exposed to an applied pressure.

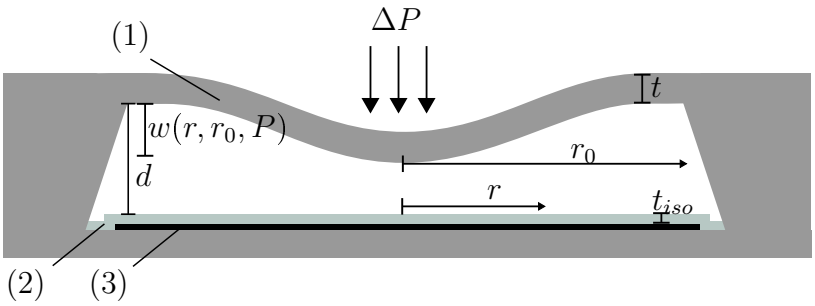


Figure 2.4: Deflection of a rigidly clamped, circular-shaped diaphragm (1) under applied pressure towards the bottom of a cavity, which comprises an isolation layer (2) and a bottom electrode (3), after [83].

The capacitance C_{n-c} in non-contact mode can be calculated with a surface integral over a circular-shaped diaphragm area with

$$C_{n-c}(r, r_0, P) = \epsilon_0 \epsilon_r \int_0^{2\pi} \int_0^{r_0} \frac{r}{t_{iso} + \epsilon_r \left[d - w(r, r_0, P)\right]} dr d\theta, \tag{2.7}$$

where t_{iso} is the thickness of the dielectric layer upon the bottom electrode, ϵ_0 is the vacuum permittivity and ϵ_r is the relative dielectric constant of the isolation layer. Solving the integral [85] leads to

$$\begin{aligned} C_{n-c}(r_0, P) &= C_0 \frac{\tanh^{-1} \xi}{\xi}, \\ \text{where } C_0 &= \frac{\pi \epsilon_0 \epsilon_r {r_0}^2}{d\epsilon_r + t_{iso}} \text{ and } \xi = \frac{w_0}{d\left(\frac{t_{iso}}{d\epsilon_r} + 1\right)}. \end{aligned} \tag{2.8}$$

This mode is usually exploited because hysteresis is hardly an issue and large deflections result in high sensitivity. The inherent non-linearity of the capacitive principle is most probably the greatest disadvantage of the operation in the non-contact mode.

Operation in Contact Mode In contact mode, also called touch mode, the centre deflection of the diaphragm is equal to the cavity height d. Changes in the applied pressure change the area in contact with the bottom electrode. A diaphragm in contact mode is shown in Figure 2.5. This mode is used less frequently, and only a few groups are reporting pressure sensors designed for operation in contact mode [86–93].

Different to the non-contact mode, the **D**ynamic **R**ange (DR) is extended beyond the initial CPP and the capacitive change according to applied pressure

pressure becomes considerably more linear. Compared to the near linear operation in non-contact mode, the operation in contact mode can provide one or two orders of magnitude of higher sensitivity [87]. This effect is because the contact area is nearly proportional to the applied pressure, and results in a nearly linear capacitance to pressure characteristics [83].

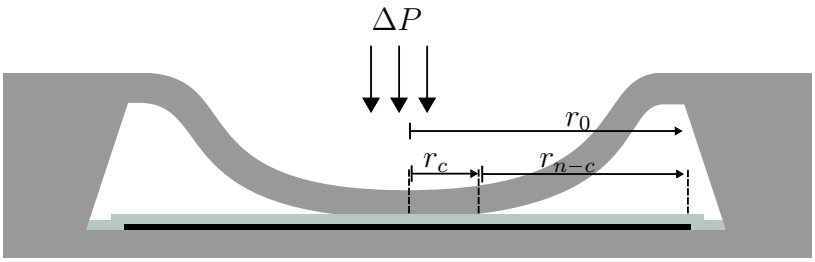


Figure 2.5: Deflection of a rigidly clamped, circular-shaped diaphragm under applied pressure in contact mode, after [83].

The majority of the sensor capacitance is given by the contact area. Here, the effective gap between the diaphragm and the bottom electrode is the thickness t_{iso} of isolation layer. The isolation layer thickness should be very small and should obtain a large dielectric constant. In consequence, the capacitance per unit area is much larger compared to that of the non-contact area.
Also in contact mode the diaphragm deflection can be modelled under the assumption of linear elasticity by Equation 2.6. A good approximation [85, 94, 95] is achieved by

$$w(r, r_0, P) = \begin{cases} d & 0 < r < r_c(P) \\ d\left(1 - \left(\dfrac{r - a_c(P)^2}{a_{n-c}(P)}\right)\right)^2 & r_c(P) < r < r_0. \end{cases} \tag{2.9}$$

The CPP is where the diaphragm touches the bottom of the cavity at the centre point $r = 0$. This pressure can directly be calculated by Equation 2.6. If the equation for the deflection of the diaphragm between the clamped edge and the cavity bottom is assumed to remain valid even for higher pressures, r_0 can be replaced by r_{n-c}. Then

$$r_{n-c}(P)^4 = \frac{64Dd}{P} \Rightarrow P_{CPP} = \frac{64Dd}{r_{n-c}^4}. \tag{2.10}$$

The capacitance C_c for a diaphragm that operates in contact mode can be derived to

$$C_c(r_0, P) = C_{iso}\left\{\sqrt{\frac{P_{CPP}}{P}} - 2\sqrt[4]{\frac{P_{CPP}}{P}} + 1\right\}, \quad \text{where } C_{iso} = \frac{\pi\epsilon_0\epsilon_r {r_0}^2}{t_{iso}} \text{ and for } d\epsilon_r \gg t_{iso}. \tag{2.11}$$

The derivations for the calculation of the capacitance C_c in contact mode can be found in [85, 94, 95].

Residual Stress

In evaluations of pressure sensor diaphragms under applied pressure it is often reported that there are significant deviations with respect to the previously mentioned model of clamped plates (e.g. [64]). Since the deflection model presented before is valid for the assumptions of negligibly small stress in the diaphragm, the observed deviations can be attributed to the residual stress and deviations from the boundary conditions. Residual stress σ_r of deposited layers combines the intrinsic stress σ_i and the thermal stress σ_{th}.

$$\sigma_r = \sigma_i + \sigma_{th} \tag{2.12}$$

Intrinsic stress results from the growth processes and primarily depends on the deposition parameters. The thermal stress results from differences in the coefficients of thermal expansion between the deposited layer and the substrate. A residual stress in a layer deposited on a substrate bends the substrate either upward (concave) or downward (convex), depending on whether the stress is tensile or compressive.

To take intrinsic stress σ_i into account, one can calculate the deflection w by solving the following differential equation:

$$\frac{d^2\varphi}{dr^2} + \frac{1}{r}\frac{d\varphi}{dr} - \left(\frac{\sigma_i \cdot t}{D} + \frac{1}{r^2}\right)\varphi = -\frac{\Delta P \cdot r}{2D}, \tag{2.13}$$

where $\varphi = -dw/dr$ expresses the slope of the deformed diaphragm. Further, a term k is defined for simplification of following equations by

$$k^2 = \frac{|\sigma_i| \cdot r^2 \cdot t}{D} = \frac{12(1-\nu^2) \cdot |\sigma_i| \cdot r_0^2}{E \cdot t^2}. \tag{2.14}$$

The solution of this differential equation by the use of Bessel functions I_n and J_n of the first kind and order n provides values for the centre deflection w_{σ_i}. For the

cases tensile and compressive residual stress [44] these are

$$w_{\sigma_i} = \begin{cases} \dfrac{P \cdot r_0^4 \left[I_0 \frac{k \cdot r}{r_0} - I_0(k) \right]}{2k^3 I_1(k) \cdot D} + \dfrac{P \cdot r_0^2 \left(r_0^2 - r^2\right)}{4k^2 \cdot D} & \text{(tensile)} \\ \dfrac{P \cdot r_0^4 \left[J_0 \frac{k \cdot r}{r_0} - J_0(k) \right]}{2k^3 J_1(k) \cdot D} - \dfrac{P \cdot r_0^2 \left(r_0^2 - r^2\right)}{4k^2 \cdot D} & \text{(compressive).} \end{cases} \tag{2.15}$$

For $r = 0$ the maximum deflection at the centre of the diaphragm, $w_{\sigma_i,c}$ in tension and in compression, is then given by

$$w_{\sigma_i,c} = \begin{cases} \dfrac{P \cdot r_0^4}{4D} \dfrac{[2 - 2I_0(k) + kI_1(k)]}{k^3 I_1(k)} & \text{(tensile)} \\ \dfrac{P \cdot r_0^4}{4D} \dfrac{[2 - 2J_0(k) - kJ_1(k)]}{k^3 J_1(k)} & \text{(compressive).} \end{cases} \tag{2.16}$$

For $k \to 0$ one obtains a term $w_{c,0}$ for the centre deflection without any intrinsic stress which is identical to $w(r = 0, r_0, P)$ in Equation 2.6:

$$w_{c,0} = \frac{P \cdot r_0^4}{64D}. \tag{2.17}$$

Forming the quotient $w_{\sigma_i,c}/w_{c,0}$ of the deflection concerning intrinsic stress (Equation 2.16) and the stress-free deflection (Equation 2.17) leads to

$$w'_{\sigma_i,c} = \frac{w_{\sigma_i,c}}{w_{c,0}} = \begin{cases} \dfrac{16\,[2 - 2I_0(k) + kI_1(k)]}{k^3 I_1(k)} & \text{(tensile)} \\ \dfrac{16\,[2 - 2J_0(k) - kJ_1(k)]}{k^3 J_1(k)} & \text{(compressive).} \end{cases} \tag{2.18}$$

These expressions can be used to evaluate the dependence of a normalised centre deflection with respect to the dimensionless intrinsic stress. An expression for a dimensionless intrinsic stress $\acute{\sigma_i}$ is given by

$$\acute{\sigma_i} = \frac{(1 - \nu^2)\sigma_i \cdot r_0^2}{Et^2}. \tag{2.19}$$

The effects of (dimensionless) residual stress on the normalised centre deflection are drawn in 2.6. As can be seen in Figure 2.6 a linear approximation is reasonable for $\sigma'_{i,c} > 10$ by

$$w'_{\sigma_{i,c>10}} \approx \frac{P \cdot r_0^2}{4\sigma_i t}. \tag{2.20}$$

For example, a tensile stress factor of 1.3 decreases the centre diaphragm deflection by about 50 %. On the contrary, an intrinsic compressive stress results in

a higher deflection compared to the deflection of a stress-free diaphragm. There is a significant difference between tensile and compressive stress: large tensile stresses are tolerable, while relatively low compressive stresses will cause buckling of the diaphragm. This can be described by the following example [44]: A poly-Si diaphragm with a radius r_0 =100 µm, a thickness t =1 µm and a Young's modulus of $E/(1-\nu^2) \approx 53$ GPa has a buckling stress of 6.5 MPa. These sample values result in a dimensionless stress $\acute{\sigma}_i = 1.23$ which corresponds to a very high deflection of the diaphragm as shown in Figure 2.6. This example demonstrates, why compressive stress in diaphragms has usually to be avoided.

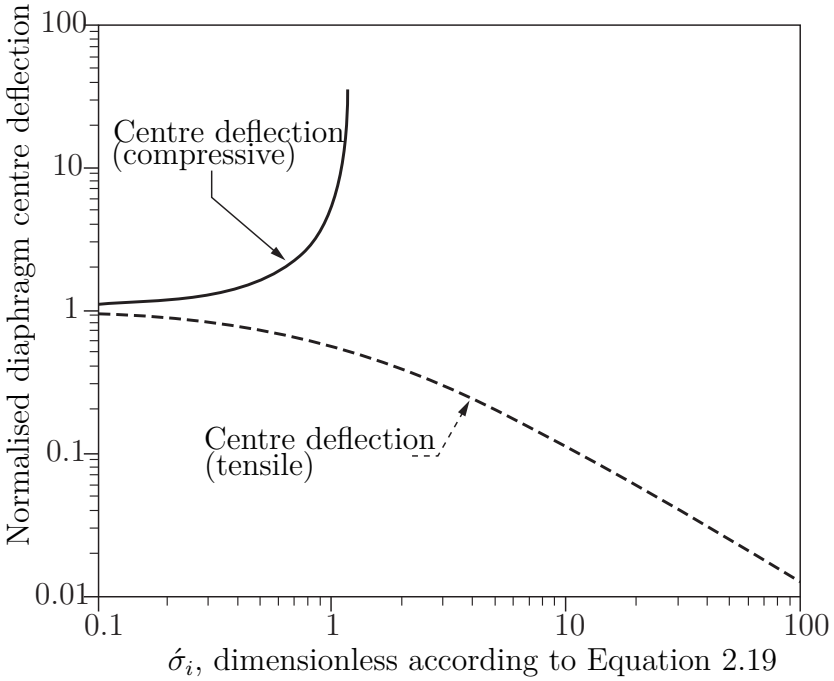


Figure 2.6: Normalised centre deflection of rigidly clamped, circular-shaped diaphragms as a function of the dimensionless intrinsic tensile (+) or compressive (−) stress, after [44]

Noise

There are three major sources of noise in diaphragm-based pressure sensors which need to be considered: mechanical vibration of the diaphragm, electrical noise and electrical noise due to the ROIC. The mechanical vibration can be divided into three different cases: Brownian motion in rarefied gases, in viscous damping media, and in thermally acoustic waves at higher pressures. In general, Brownian noise was found to be a negligible noise source at atmospheric pressure, since the

Brownian equivalent pressure noise is substantially less than 10×10^{-3} Pa [96]. Brownian motion of gas molecules in the close surrounding of a diaphragm delivers thermal energy, which can cause a change in diaphragm deflections. This can be considered as a noise equivalent mean square pressure. Equation 2.21 allows to estimate the impact of Brownian motion on a diaphragm for rarefied gas environments and for low frequencies [44]:

$$\overline{p_n^2} = \alpha \sqrt{\frac{32 k_b T}{\pi}} \frac{\left(\sqrt{m_1} P_1 + \sqrt{m_2} P_2\right) BW}{r_0^2}, \tag{2.21}$$

where k_b is the Boltzmann constant, T the absolute temperature, BW the bandwidth of the pressure sensor, m_1 and m_2 the masses of the gas molecules in both the pressures P_1 and P_2, which apply on both diaphragm sides. The coefficient α is set as 1.2 for capacitive diaphragms and 1.7 for piezoresistive diaphragms, each circular-shaped with a diameter of r_0. This expression was derived from ideal gas kinetics and is valid under very large mean free path lengths of the gas molecules, i.e. only at very low pressures. This means, the Brownian noise has a white noise spectrum. It is important to note that the magnitude only depends on the diaphragm area.
In higher gas or liquid pressure ranges, viscous damping dominates. Here, thermally generated acoustic waves become a factor to consider. Thus, the mean square noise pressure on the surface of the diaphragm is [97]:

$$\overline{p_n^2} = 4kTR_{r_0}, \tag{2.22}$$

where R_{r_0} represents the mechanical damping coefficient per unit area ($= R/\pi r_0^2$). Alternatively, R can be replaced by $m\omega_0/Q$, where m is the effective mass per unit area of a diaphragm, ω_0 is the resonant frequency and Q is the mechanical quality of the diaphragm resonance.

Noise in piezoresistive sensing The noise principles regarding the electrical noise from the piezoresistors and electrical noise due to the ROIC are shortly introduced. Piezoresistor thermal noise is written as [44]:

$$\overline{p_{n_{PZR}}^2} = \frac{4kTR_{PZR} \cdot BW}{\left(V_{supply} S_{pzr}\right)^2} \propto \frac{t^4}{r_0^4}, \tag{2.23}$$

with R_{PZR} as equivalent resistor of a resistor bridge. The ROIC noise gives a pressure resolution based on the resolvable change in voltage, ΔV_{min}:

$$Res_{PZR} = \frac{\Delta V_{min}}{V_{supply} S_{PZR}} \propto \frac{t^2}{r_0^2}. \tag{2.24}$$

Noise in capacitive sensing Comparable to the piezoresistor thermal noise is the kT/C noise for capacitors:

$$\overline{p_{n_{CAP}}^2} = \frac{4kT\left(C_0 + C_{parasitic}\right)}{\left(V_{supply} \cdot C_0 \cdot S_{CAP}\right)^2} \propto \frac{t^6 \cdot d^3}{r_0^{10}}, \tag{2.25}$$

where C_0 is the nominal capacitance and $C_{parasitic}$ represents parasitic stray capacitances in parallel to C_0. Due to ROIC filters a band-limitation of the quoted kT/C-noise in Equation 2.25 can be added.
In capacitive diaphragms, electrostatic pressure variations should further be considered. An applied voltage across the capacitor plates establishes an electrostatic driving force on the diaphragm, which should especially be considered for very large deflections or $w(0, r_0, P) \approx d$. Even though the influence is assumed to be in a magnitude of 1 hPa, this noise source is neglected. This is because the supply voltage is usually applied as oscillating voltage with a certain waveform and frequency, which is bound to the ROIC characteristics. Thus, it is inherently difficult to determine.
Another specific noise is the circuit noise of the used ROIC. This noise is usually much more limiting than the sensor noise itself. The pressure resolution based on the resolvable change in capacitance, ΔC_{min}, is:

$$Res_{CAP} = \frac{\Delta C_{min}}{C_0 S_{CAP}} \propto \frac{t^3 \cdot d^2}{r_0^6}. \tag{2.26}$$

Differences in Noise of Piezoresistive and Capacitive Pressure Sensors
Due to the higher contribution of thermal noise in piezoresistive sensing, the capacitive sensing approach shows an advantage, as it is inherently less noisy. With micromachined devices, however, the scaling limit of capacitive sensors is stricter than for piezoresistive. The values of capacitance are extremely small (in the range of femto to attofarads), and the additional noise from the interface electronic circuits often exceeds that of a resistance-based system [98].

Trapped Gas Effects

A further source for the temperature sensitivity of a pressure sensor diaphragm, in addition to different coefficients of thermal expansion of the diaphragm layers, for example, can be trapped gas, which was trapped in the closed cavity when the top layer was applied. A consequence can be errors in reading as well as loss of sensitivity [36]. For non-reactive trapped gases, the ideal gas law can be used to estimate the volume change ΔV after the sensor has returned to room temperature [99]:

$$P_1 = \frac{mRT_1}{V_0 - \Delta V} \approx \frac{mRT_1}{V_0 - \frac{a^6(P_a - P_1)\pi}{192D}} \tag{2.27}$$

where P_a is the applied pressure, V is the volume of the cavity, m is entrapped gas mass, R is the universal gas constant for air and T_1 is the temperature at the thermodynamic state in the closed cavity.
Another potential gas mechanism is outgasing of adjacent layers, which surround the cavity. Both trapped gas mechanisms should be prevented. Normally, annealing or deposition at high temperature are methods by which trapped gas mechanisms can be avoided. Since the temperature budget is limited to about 400 °C in post-CMOS processing, excessive annealing or high-temperature deposition processes are no options. However, prevention can be achieved by closing the cavity with thin film depositions at very low pressures [37]. Also, the use of highly reactive CVD processes could be considered to completely consume the process gases at the surfaces and inside the cavity [100].

Performance Criteria

Important characteristics of pressure sensors are full-scale output, sensitivity, dynamic range, and the temperature coefficients of sensitivity and offset. The sensitivity S is defined as the normalised output change per unit pressure change (δP) to the reference signal:

$$S = \frac{1}{\Theta}\frac{\delta\Theta}{\delta P} \tag{2.28}$$

The temperature sensitivity of a pressure sensor is an important performance metric. The definition of **T**emperature **C**oefficient of **S**ensitivity (TCS) is:

$$TCS = \frac{1}{S}\frac{\delta S}{\delta T} \tag{2.29}$$

The **T**emperature **C**oefficient of **O**ffset (TCO) of a pressure sensor is the value of the output signal at a reference pressure ($\delta P = 0$):

$$TCO = \frac{1}{\Theta_0}\frac{\delta\Theta_0}{\delta T} \tag{2.30}$$

The DR of pressure sensors is defined as the range over which the sensor can provide a usable output. This range can be limited due to the saturation of the transformed output signal, the yield or the failure of the diaphragm. The **F**ull **S**cale **O**utput (FSO) is the algebraic difference in the end point of the output. Further, the linearity is an important parameter as well. As most capacitive pressure sensors are operating in non-contact mode it is not playing a dominant role though.

2.1.4 Post-CMOS Integration of Pressure Sensor Elements

Some publications are identified, which describe developments regarding post-CMOS pressure sensor fabrication. However, some of them mix up intermediate CMOS integration, finalised by a few post-CMOS process steps, as for example [101, 102]. In this thesis, in contrast, an entire post-CMOS pressure sensor technology to be independently added above a CMOS substrate is developed. Only methods of surface micromachining are utilised. Thus, only those are considered, which describe a pure post-CMOS technology.

Under these conditions, the sealing of diaphragms is one of the most formidable challenges. The design of etch accesses may be horizontal, vertical, or through permeable materials. Trade-offs exist between release time and deposition on the structure [103]. On the one hand, the sealing issue of open diaphragms can be considerably simplified as etch accesses are placed on the cavity sides as horizontal etch-access channels. Here, a direct sealing by thin film **L**ow **P**ressure **C**hemical **V**apour **D**eposition (LPCVD) of poly-Si [31] or LPCVD Si_3N_4 [104] is established, which requires temperatures higher than 700 °C.

Low temperature sealing processes are required for post-CMOS technologies. Here, LPCVD **P**hosphorus **S**ilicate **G**las (PSG) and **P**lasma-**E**nhanced **C**hemical **V**apour **D**eposition (PECVD) Si_3N_4 are developed as sealing materials deposited at 450 °C and 300 °C, respectively [105]. As a drawback, the minimum required layer thicknesses are about 6 to 8 times higher compared to the LPCVD sealing at higher temperatures. Several micrometres of sealing are inappropriate layer

thicknesses for miniaturised diaphragm-based pressure sensors.
Some recent approaches at IMEC utilised alternative materials [43,106]. Amongst others, are **S**ub-**A**tmospheric **C**hemical **V**apour **D**eposition (SACVD) SiO_2 (Figure 2.7 a.) and sputter-deposited AlCu (Figure 2.7 b.), which is applied on an intermediate μc SiGe layer with a microhole in the centre (4) shown in Figure 2.7 c.. These two methods showed the most promising results regarding hermeticity, tensile layer stress and achieved cavity pressure. Unfortunately there are significant disadvantages with these materials, as for example CTE mismatches in the magnitude of 5 to 10. Further, metals usually suffer from creep [107]. SiO_2, however, is sensitive to humidity and would require an additional protection layer. Therefore, the sealing of pressure-sensitive diaphragms is not satisfactorily solved.

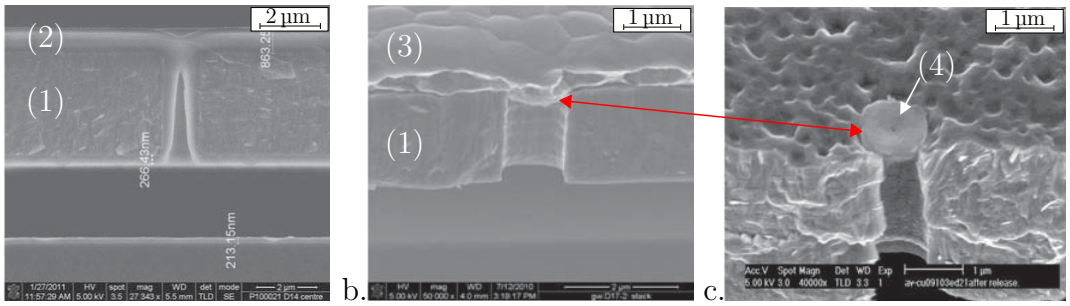


Figure 2.7: SEM cross sections of SiGe (1) diaphragms hermetically sealed by a. SACVD SiO_2 (2), or b. sputter deposited AlCu (3) applied on c. an intermediate cover layer with a microhole in the centre (4) [43].

In [43], piezoresistive as well as capacitive pressure sensor demonstrators are reported with different remaining challenges. The conclusion for piezoresistive post-CMOS pressure sensor is that higher annealing temperatures are required to yield acceptable resistor matching. This is in conflict with the temperature limitation of post-CMOS processes. Thus, the capacitive approach is reported to be more promising. Here, amongst others, an unfavourable design limited the sensor performance. For example, relatively thick SiGe diaphragms have to be established in the range of some µm. One of the reasons for this is due to the necessity of seed layers. Despite the relatively large area of the capacitive sensor elements, this leads to poor sensitivity.

2.1.5 Discussion on Principles Regarding post-CMOS Integration

Some aspects of capacitive and piezoresistive pressure sensors and their differences are made a subject of discussion in the previous chapters. These criteria regarding the potential of post-CMOS-integration are assessed in Table 2.2.
Summarising, the post-processing is assessed as more beneficial for capacitive than for piezoresistive pressure sensors. First, the advantage of saving area is more exploited in the case of capacitive applications which require relatively large MEMS area in comparison to piezoresistive pressure sensors. Second, the benefit of parasitic reduction on device performance is stronger for capacitive sensors than for piezoresistive pressure sensors. Third, the fabrication complexity is reduced for capacitive pressure sensors. Both principles require sealed diaphragms, with additional steps for piezoresistive structures, which moreover require critical annealing temperatures. Fourth, the lower power consumption [98, 108] make the capacitive principle more interesting for applications without random power supply, such as in biomedical implant devices.

Table 2.2: Assessment of PZR and CAP pressure sensor characteristics regarding post-CMOS integration. + = good; 0 = medium; − = moderate.

Criteria	PZR	CAP	References
Scaling limit	+	−	[44]
Noise limit	−	+	[96]
Fabrication complexity	0	+	[109]
Power consumption	0	+	[98, 108]
Potential for post -CMOS integration	0	+	

2.2 Post-CMOS MEMS Integration

2.2.1 Specifications of post-CMOS Integration

The development of an appropriate process scheme for a monolithic post-CMOS integration of MEMS is bound to some general requirements regarding processing

or substrate conditions. Amongst others, the most important are [106, 109–113]:

- A temperature budget limitation due to the CMOS technology chosen as substrate.
- A CMOS protection to apply MEMS processes.
- A planarised interface of the CMOS substrate as MEMS ground.
- A sufficient electrical connection of MEMS to CMOS substrate.
- Connectivity of CMOS interfaces.

The temperature budget limitations arise from the need to prevent degradations caused by thermally activated diffusion, agglomeration, spiking, or dopant deactivation in any CMOS IC. Exceeding the thermal budget limitations is firstly found to cause degradation of the metal interconnects [58] in standard CMOS circuits (i.e. 350 nm to 250 nm, aluminium-based metallisation). For example, an increase in the via resistance of >10 % is found after a temperature exposure at 450 °C for about 120 min [114]. In [58] it was found that a maximum temperature of 520 °C must not be exceeded for a duration of 90 min for standard 350 nm CMOS technologies. Respectively, investigations on standard 250 nm CMOS technologies show a maximum temperature budget of 360 min at 425 °C [114]. Thus the reduction of, for example, junction depths and interconnect dimensions in CMOS technologies may further decrease the temperature budget of post-CMOS processes. In [109, 110] it is mentioned that more advanced CMOS technologies comprising copper-based metallisation and low-permittivity dielectric layers are subjected to even more restrictive temperature limitations. According to a proposal for guidelines in post-CMOS processing [111], a general temperature limitation to 400 °C seems to be reasonable for aluminium-based CMOS substrates.
First, this limitation affects **C**hemical **V**apour **D**eposition (CVD) techniques, which require high deposition temperatures for usual. Second, methods for stress control such as temperature annealing, are only partially applicable due to the limited temperature budget. High temperature annealing is often applied, for example, to reduce intrinsic layer stresses.
Additionally, any contamination or damage to the already processed CMOS circuitry by chemicals for the surface micromachining and release etch have to be prevented [115]. The fabrication of MEMS in surface micromachining usually requires sacrificial layer technologies. Many MEMS processes utilise HF as a release

chemical to implement free-standing structures, for example. HF is reactive with most oxides and, with less reactivity, silicon rich nitrides and may therefore not be appropriate to be applied to a processed CMOS wafer.
With restriction to the specific temperature limitations of a certain CMOS technology, the application of a post-CMOS MEMS fabrication may become possible on any CMOS substrate. When it comes to the design of MEMS pressure sensors, which convert e.g. any physical displacement into an electrical signal, a downscaling of pressure sensors is inter alia limited with respect to a required sensitivity. Thus, it can be assumed that large shares of the available surface of any ROIC should ideally be exploited for sensor fabrication. To use any standard CMOS substrate as basis for MEMS requiring relatively large amounts of space, a planarised passivation and an additional via/metal layer has to be considered. For example, in [113] it is demonstrated that a CMOS substrate processing to generate a planarised post-CMOS MEMS interface can be realised with typical semiconductor equipment in a CMOS fab (here: 350 nm standard CMOS technology). In Figure 2.8 a result of a planarisation procedure is shown.

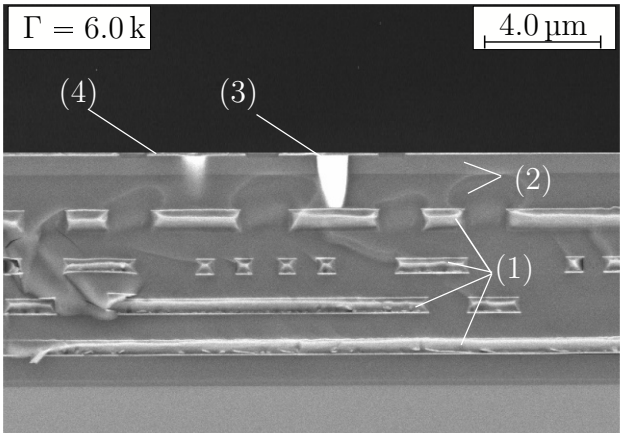


Figure 2.8: SEM cross-section of a planarised CMOS substrate after application of an W-CMP process. The substrate comprising four aluminium metal layers (1) and a planarised Si_XN_Y/SiO_2-passivation (2) filled with W-vias (3). The interconnection between the top thin TiN metallisation (4) and the 4^{th} Al metallisation is realised by W vias with a typical diameter of 1 µm. This interface is fabricated in a standard 350 nm technology at Fraunhofer IMS [113].

First, the intermediate dielectric layers as well as the top passivation layer are planarised by **C**hemical **M**echanical **P**olishing (CMP). Second, the interconnection through the planarised nitride/oxide-passivation is exemplarily filled

with tungsten plugs. These measures facilitate the post-processing due to a very smooth surface topology of the CMOS substrate. Depending on the post-CMOS MEMS process scheme, it can be useful to conclude these interface processing by a thin metal layer. This process step can be synonymous with the first process step in post-CMOS MEMS process chain.

2.2.2 Materials for post-CMOS Integration

An assortment of an initial literature search for compatible materials in order to design a capacitive pressure sensor in a post-CMOS compatible process scheme is presented in Table 2.3 [69, 116–120]. The presented characteristics are chosen with respect to the sacrificial layer technology utilising vapour-phase etching via HF or XeF_2 and the mechanical properties. A major concern in the material choice is the expansion mismatch between the substrate and diaphragm materials. The **C**oefficient of **T**hermal **E**xpansion (CTE) in capacitive pressure sensors can be minimised by the proper choice of materials and appropriate fabrication sequences.

Table 2.3: Materials for post-CMOS integration [69, 116–121]

Material	Etching vHF or XeF_2	El. Conductance	Young's Modulus ϵ in GPa	Poisson's Ratio ν	CTE α in 10^{-6}/K (at 25 °C)
Si	no / yes	Semiconductor	107	0.28	2.6
SiO_2	yes / no	no	70	0.17	0.5
Ti	yes / yes	yes	115	0.32	8.6
Al	yes / no	yes	70	0.35	23.1
Cu	yes / no	yes	124	0.34	16.5
Si_3N_4	yes / no	no	340	0.23	2.3
3C-SiC	no / no	Semiconductor	450	0.45	4.3
TiN	yes / yes	yes	50	0.32	22
Al_2O_3	no / no	no	400	0.25	6.5
Ta_2O_5	yes / -	no	145	0.25	-
SiGe	no / yes	Semiconductor	149	0.25	5.9
W	no / yes	yes	406	0.28	4.5
TiW	no / yes	yes	411	0.28	4.5
AlSi	no / no	yes	80	0.33	22

Etching barriers against vapour HF

In a MEMS releasing process, the sacrificial layer must have a high selectivity towards the layer underneath to avoid the formation of potential by-products. Therefore, this layer functions as an etching barrier. A frequently-used insulating material is for example Si_3N_4, which is reported to be an inappropriate etching barrier against vapour HF etchant in alcoholic vapour [122, 123], thus a proper material is desired. Silicon carbide (SiC) has attracted most attention in such situations due to its advancements in thermal stability, hardness, wear resistance and chemical stability [124, 125]. SiC also shows potential as electrical isolation material because of the wide band gap around 3 eV [124, 126]. Also, Al_2O_3 and AlF_3 are reported to remain unaffected after vapour HF exposure [116]. In the following, Al_2O_3 and Al, respectively, Si_3N_4 and SiC are discussed as potential materials for etching barriers against vapour HF in water vapour.

Al and Al_2O_3 Al is another common material exploited in the MEMS industry. If purely metallic Al is exposed to ambient, a thin film of aluminium oxide will form on the surface as shown in Equation 2.31. This film can be utilised as an etch barrier to stop further reaction from the surface to the bulk.

$$2Al + 3H_2O \leftrightarrow Al_2O_3 + 3H_2 \tag{2.31}$$

After an exposure of Al and Al_2O_3 to vapour HF, cracks can be formed on both the surfaces. In Figure 2.9 a. and b., the formation of aluminium fluoride with a thickness of 200 nm could be detected after etching on Al. In Figure 2.9 c., the adhesion between an 80 nm ALD-Al_2O_3 layer and the substrate is visibly reduced after an vapour HF exposure at 26.7 hPa [127]. On the evidence of the corresponding substance analysis on the layer surface, which demonstrates a low O concentration and a high F concentration, the etching reaction may occur between Al_2O_3 and HF. As shown by Equation 2.31, the existence of the thin water layer during the vapour HF etching can promote the formation of Al2O3 oxide and thus, further etching on Al_2O_3. Therefore, Al_2O_3 is not a suitable material as an etching barrier layer against vapour HF in vapour H_2O. Considering that Al can be effectively oxidised to Al_2O_3 and itself can react with HF, Al is also not a proper material for the desired function. There is the exceptional case for lower process pressure ranges, in which reduced amounts of

water condense on the surface. Under given process conditions of the experiments in [127], a reduction of the process pressures to less then 10.7 hPa rapidly inhibits the de-lamination and etching of Al_2O_3. It is assumed that either the reduced amount of H_2O due to reduced pressure, or a surface passivation of the Al_2O_3 due to F and Al bonding is responsible for the inhibited de-lamination and etching.

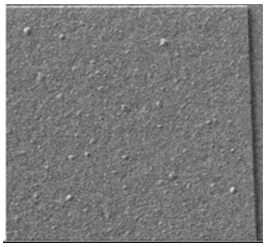
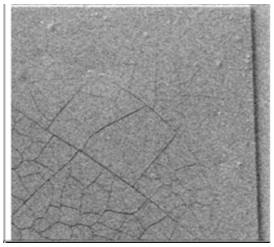
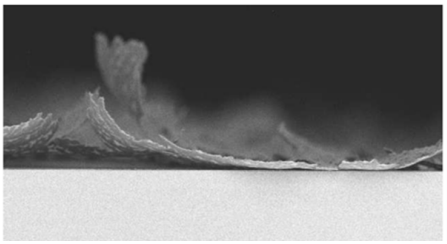
a.  b.  c. 

Figure 2.9: a. Al pre vapour HF exposure, b. Al post vapour HF exposure [69], c. 80 nm ALD-Al_2O_3 post vapour HF exposure.

Si_3N_4 Si_3N_4 is worth being discussed for two reasons. First, it is frequently used as an etch stop material in wet HF etching technologies for SiO_2 sacrificial layers, even in wet HF etching [37,128]. Second, in CMOS technologies, Si_3N_4 is a standard top surface layer, which provides protection and passivation functions. The second point is important for this thesis, because a post-CMOS MEMS fabrication is developed. It is reported that the selectivity with respect to Si_3N_4 is decreased by a factor of 4 compared to wet HF etching [123]. During the vapour HF exposure Si_3N_4, residues are formed according to Equation 2.32 [129]:

$$Si_3N_{4(g)} + 16HF \rightarrow (NH_4)2SiF_{6(s)} + SiF_{4(g)} \tag{2.32}$$

The solid residues can either be removed by wet cleaning processes or temperatures higher than 100 °C. The second is more appropriate since stiction of two surfaces can be avoided. Then, the decomposition is according to Equation 2.33:

$$(NH_4)_2SiF_{6(s)} \rightarrow NH_4HF_{2(s)} + SiF_{4(g)} + NH_{3(g)} \tag{2.33}$$

Good results are obtained with a short vacuum anneal at 10 Pa at 180 °C after vapour HF etching, by which the liquid phase of $NH_4HF_{2(s)}$ is avoided before evaporation [123].
In this thesis diaphragm structures which are designed to be released by wet HF etching via SiO_2 channels are experimentally investigated. In Figure 2.10 a., the

blue layer shows a part of the lateral etching channel layer before etching. The diaphragm structure is formed on a Si_3N_4 layer (1). Here, diaphragm structures have a diameter of 96 µm, a 670 nm thick sacrificial layer in TEOS SiO_2 and an extra 70 nm sacrificial layer spreading out of the sensor element as lateral etch-access channels (2). The functional layer on the sacrificial layer is 1 µm thick poly-Si (3). After the SiO_2 outside the sensor elements is etched, channel openings are released at the edge of the sensor elements. Then the etchant can push the etching reaction frontier into the sensor elements.

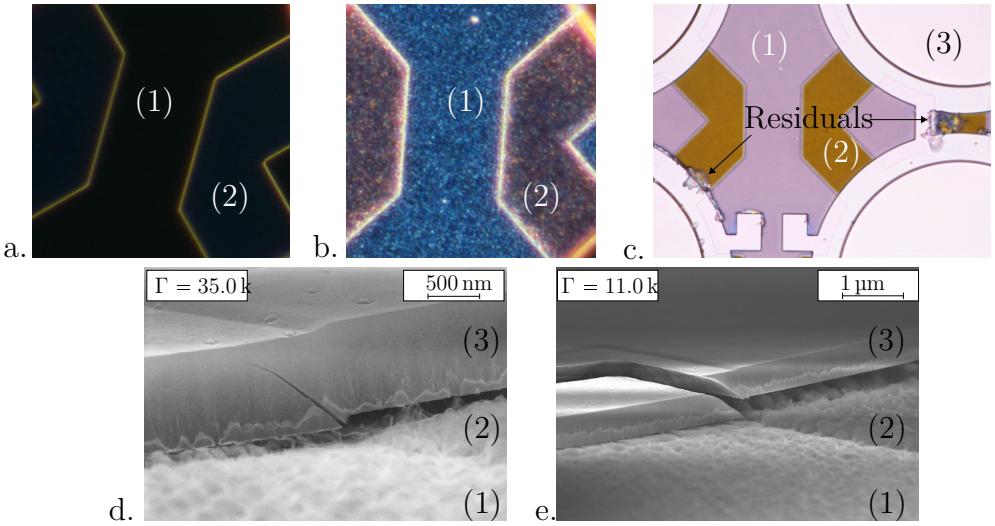


Figure 2.10: Microscope inspection results of a. a sample pre and b. post vapour HF exposure, both in dark field, c. a light field view showing residuals. SEM inspections in d. and e. show cracking of a structure due to residuals (primary $(NH_4)_2SiF_{6(s)}$). The materials exposed to vapour HF are Si_3N_4 (1), TEOS SiO_2 (2) and poly-Si (3).

Figure 2.10 b. shows that the surface of Si_3N_4 is visibly roughened (1) and is comparable to the SiO_2 surface (2). As an example, Figure 2.10 c. shows some residuals, which are here agglomerated at an etch-access channel. SEM inspections are shown in Figure 2.10 d. and e., respectively. The vapour HF etching produces residuals (primary $(NH_4)_2SiF_{6(s)}$), which irreversibly crack the structural layer. Thus, further measures, such as a decomposition according to Equation 2.33 under temperature and vacuum are no longer relevant. It is concluded that Si_3N_4 is not an appropriate material as an etching barrier in vapour-phase etching with HF and H_2O mixtures and a sufficient protection of the subjacent materials is not assured.

SiC, Silicon Carbide Applications, such as pressure sensors for use in harsh environments, at high pressure and high temperature in an automotive cylinder [89], electrostatic RF switch, accelerometers [130], or MEMS packaging encapsulations [131] are achieved with SiC. In these applications SiC is mainly used as structural layer material, while Si or SiO_2 are employed as sacrificial layers [132]. Investigations of the corresponding etchant (HF etchant to SiO_2, XeF_2 to Si) have proven the chemical inertness of SiC [133].
SiC is a polymorphic material, which owns more than 200 polytypes. The main technologically relevant and commercially available polytypes are $3C$-, $4H$- and $6H$-SiC [125,134,135]. The cubic structure $3C$-SiC is denoted as β-SiC and other polytypes, which are all uniaxial, are denoted as α-SiC [136]. According to different deposition parameters (primarily temperature and pressure) different polytypes are formed in single-crystal and polycrystalline [125, 132, 135]. Additionally, amorphous SiC, which can preserve good mechanical properties, is deposited when applied in temperature-limited situations [125, 130, 132]. [137] Considering the extremely high deposition temperature (above 1000 °C) of single-crystal and the feasibility of current micromachining technology, amorphous and polycrystalline SiC are commonly applied in MEMS applications.
With the help of PECVD, polycrystalline SiC deposition temperature can be reduced to a relatively low temperature range (400 °C to 700 °C). Amorphous SiC can be deposited at even lower temperatures (below 400 °C) [125, 132, 135].
Thin SiC films grown on Si substrates are also desirable candidates for the fabrication of pressure sensors that work in high temperature ranges. For these applications, the required SiC layer thickness ranges from a few nanometres to a few micrometres. [82]
SiC combines interesting properties, such as mechanical strength [132], high-wear resistivity [138], high thermal conductivity, an extreme chemical inertness in several liquid electrolytes [132], or an excellent etch resistivity against gaseous HF [69]. Additionally, SiC is increasingly being used for various functions in the fabrication of MEMS sensor devices, especially if a harsh environment is required. For this purpose, capacitive [82,89,137,139], as well as piezoresistive pressure sensors [140–142] made of SiC are reported.
In this work a SiC process is developed and tested as an etching barrier against vapour HF in vapour H_2O, as well as in the vapour XeF_2.

SiGe, Silicon Germanium as post-CMOS MEMS Material

In recent years, polycrystalline SiGe has become one of the most promising materials for post-CMOS MEMS developments. The main advantages of SiGe by methods of PECVD are high deposition rates at CMOS-compatible process temperatures of $\leqslant 450\,^{\circ}\mathrm{C}$, mechanical properties comparable to poly-Si and low resistivity [143, 144]. Two major approaches have been developed to deposit PECVD SiGe layers with these characteristics. First, hydrogen (H) dilution [145] and, second, with the aid of preliminary-deposited CVD SiGe seed layers [110].
With respect to a later integration in a post-CMOS pressure sensor technology in Fraunhofer IMS laboratories, different low-temperature processes for PECVD of in-situ boron-doped polycrystalline poly-SiGe layers have been developed as potential diaphragm materials [42,146]. A total increased gas flow causes enabled the PECVD of polycrystalline SiGe at very low process temperatures of less than $380\,^{\circ}\mathrm{C}$. The Ge-concentrations is about 70 % to 80 %. A minimal tensile stress in the magnitude of 10 MPa to 100 MPa and a very low electrical resistivity of less than $10\,\Omega\,\mathrm{mm}^2/\mathrm{m}$ are achieved. As a further benefit, no seed layers are required. The deposition rates of about $350\,\mathrm{nm/\,min}$ are relatively high. All these properties are highly desired for MEMS processing. This makes poly-SiGe an almost perfect candidate to replace poly-Si as the state-of-the-art MEMS diaphragm material. Poly-Si requires high temperatures in the range of $800\,^{\circ}\mathrm{C}$ to $1000\,^{\circ}\mathrm{C}$ to establish low tensile stress and for dopant activation [147]. This makes poly-Si an incompatible material for post-CMOS processing.
High Ge concentrations, however, can lead to drawbacks regarding reliability. For example, Ge is more affected by humidity compared to Si. Here, oxidation can become an issue because GeH species are more unsteady than SiH species [144, 148, 149]. Another side effect of high Ge concentration is an increased surface roughness, which is not expected to have a great significance for pressure sensor developments.
The patterning of SiGe alloys has been evaluated for a long time. Here, Cl [143, 150, 151], as well as F-based RIE [150, 152] processes are established. Further, some research regarding SiGe MEMS is performed at *IMEC*, Belgium [106, 109, 110, 145, 153]. There, post-CMOS technologies for various MEMS applications are under development.

2.2.3 Processes for post-CMOS Integration

Methods of surface micromachining are to be used for the fabrication of post-CMOS pressure sensors. Some important methods of layer deposition and etching (wet, anhydrous and dry) are introduced in this chapter.

Layer Deposition

In both electronic and mechanical aspects, the process chain for MEMS applications requires thin film deposition technologies. Combined with methods of photolithography, patterned multiple layer structures can be fabricated serving as electrodes, conductors for wiring, insulation, etching barriers, sacrificial layers and more. In surface micromachining, commonly used methods of layer deposition are CVD, ALD and PECVD. [154].

Vapour Deposition Vapour deposition, which transfers material from source to target through a vapour phase, is a common thin film deposition technology. The target, where the material solidifies to form thin film, can be a substrate or a previously deposited layer. This technology is mainly classified into two varieties: **P**hysical **V**apour **D**eposition (PVD) and CVD. PVD is mainly a transformation between phases and offers the advantage of material diversity. CVD benefits from film properties such as uniformity, purity and isotropy, since some kind of chemical reaction is involved during film deposition [155, 156]. The general process of CVD is as follows:

- Mass transport of convection introduces volatile precursor gases into the reactor chamber. Usually, the gases do not act as reactants directly. An additional activation process is required to excite and/or decompose the gases. This activation energy could be provided by e.g. heating, radiation or plasma.
- The gases or the gas constitutes, diffuse to the target substrate and adsorb on to the substrate surface.
- Surface chemical reaction occurs among adsorbed reactant molecules.
- The product of the reaction forms thin film through nucleation and island growth. The volatile by-products desorb into gaseous phase.

- The waste and by-product are exhausted by the convection.

Obviously, by-products have to be transformed into gaseous phase, to be exhausted. This is one prerequisite. With variations in process parameters, for instance, total pressure, gas flow, substrate temperature, and films with different properties can be obtained. The obtained thin film may show solid film as well as crystalline characteristics, such as mono-crystalline, polycrystalline and amorphous [132].
The reaction can be classified into homogeneous and heterogeneous, depending on the location, where the reaction occurs. The homogeneous reaction occurs not only on the surface of the substrate, but also in the space above it, even in the main gas flow. For this kind of reaction, a solid reaction product may be produced above and hit the substrate, resulting in flaky film surface with poor uniformity and numerous particles. Heterogeneous reaction only occurs on the surface of the substrate and the substrate functions as a catalyst [157]. This is desired for thin film deposition to provide good uniformity and flat surfaces.
High Density PECVD (**I**nductively **C**oupled **P**lasma (ICP) deposition) is a plasma deposition technique wherein inert gases are introduced above an inductive coil, which is placed around a ceramic tube. **R**adio **F**requency (RF) is applied to the coil to create a plasma. Volatile gas can be introduced near the substrate surface through a gas ring. If the inert gases combine with the volatile species, a chemical reaction occurs and layers are deposited on the substrate surface. This technique enables to apply more moderate temperatures than the typical PECVD ones to the substrate, and thus the process is well suited for depositing onto surfaces that have temperature limitations. By applying RF to the chuck, the film properties can be influenced. In this thesis, sacrificial layers made of SiO_2 and the developed SiC-layers are deposited via PECVD utilizing Inductive Coupled Plasma (ICP) in a *Plasmalab System 100* from *Oxford Instruments*. The utilized system uses an ICP source of *ICP-CVD 380* for introducing multiple gas lines with mass flow controllers to enable diverse materials deposition. Regarding the approaches to activate plasma, a unique magnetic ICP coupling at 2 MHz set up by the coil around the dielectric wall is designed to produce inductive coupled-plasma in the deposition chamber (besides the capacitive radio frequency coupling at 13.56 MHz in ISM band, which is commonly used in PECVD). This features higher density plasma resulting in good uniformity and outstanding reproducibility [158, 159].

Atomic Layer Deposition (ALD) ALD is a special type of CVD technology. Unlike other CVD types, ALD distinguishes itself by an alternating exposure of two precursors which leads to sequential reactions on the surface of the substrate. Thus, a self-limiting film growth of up to one atomic layer per deposition cycle can be achieved. This allows a highly isotropic, conformal and dense thin film coating, even on non-planar substrate surfaces with high aspect ratios.
Growth rates are determined by sufficiently long pulse times of single precursors which guarantee saturation of the surface to be coated. Also the process temperature influences growth rate by influencing reactivity of precursor gases. For improved reproducibility of film growths a temperature region needs to be identified, in which a self-limiting growth with a constant growth rate is established. This temperature region is called the *ALD-window*. [160]
At Fraunhofer IMS, a thermal ALD equipment of the type *R200* from *Picosun Oy*, which is a single-wafer reactor with vertical gas flow, is used. The ALD-windows of the available materials are in a range of 250 °C to 400 °C, as listed in Table 2.4.

Table 2.4: ALD process parameters for Al_2O_3, Ta_2O_5 and ZnO.

	Precursor A		Precursor B		Temperature
Material	pulse time	purge time	pulse time	purge time	Range
Al_2O_3	$AlME_3$ 0.1 s	6.0 s	H_2O 0.1 s	10.0 s	≈220 °C to 380 °C
Ta_2O_5	$Ta(EtO)_5$ 1.6 s	8.0 s	H_2O 0.1 s	8.0 s	≈270 °C to 300 °C
ZnO	DeZn 0.1 s	8.0 s	H_2O 0.2 s	8.0 s	≈200 °C to 300 °C

The basic ALD principle is explained with an ALD cycle of Al_2O_3 deposition process. Here, usual precursors are trimethylaluminum ($AlME_3$) and water (H_2O). Nitrogen (N_2) serves as an inert carrier and purging gas. First, the available surface sites (−OH groups) of the substrate are saturated by applying $AlME_3$. A purging step with N_2 removes by-products and the excess precursor. In the third step, the second precursor H_2O is applied so that $AlME_3$ and H_2O can react to Al_2O_3. The by-product in this chemical reaction is CH_4 which is removed by a second purging step within a deposition cycle. The discussed

chemical reaction is summarised in Equation 2.34:

$$2\,\mathrm{Al(CH_3)_3\,(g)} + 3\,\mathrm{H_2O\,(g)} \longrightarrow \mathrm{Al_2O_3\,(s)} + 6\,\mathrm{CH_4\,(g)} \tag{2.34}$$

Sacrificial Layer Etching

SiO_2 as Sacrificial Layer Mainly crystalline and amorphous types of SiO_2 are involved in the semiconductor industry. Commonly, an etchant containing hydrofluoric HF species is chosen to etch SiO_2, because the extremely high electronegativity of fluorine can break up the solid bond between Si and O in SiO_2 lattice [122, 161, 162].

Wet HF Etching A conventional approach to release free-standing structures that exploit SiO_2 as a sacrificial layer is to immerse them into an HF-containing solution. The etching reaction occurs when the etchant enters appropriate structures via the corresponding etching accesses. The general SiO_2 etching reaction by the etchant hydrofluoric water solution (HF) is shown in Equation 2.35 [163].

$$\mathrm{SiO_2} + 4\,\mathrm{HF} \longrightarrow \mathrm{SiF_4} + 2\,\mathrm{H_2O} \tag{2.35}$$

The bonds between Si atom and O atom in the lattice structure are terminated and this kind of Si-O bond is replaced by a Si-F bond. Unlike the O atoms, every F atom here can provide one bond to another Si atom, only. This means that the connection between Si atoms through bonds with Si atoms will terminate. If this consistent reaction occurs from the surface to bulk, Si atoms are released to the solution in the form of silicon tetrafluoride, SiF_4. The reaction acts as a repetitious dissolving process. The reaction product (SiF_4) can further react with HF to produce hexafluorosilicic acid (H_2SiF_6) (Equation 2.36). Equation 2.35 and Equation 2.36 can be combined together to induce a total reaction as Equation 2.37. This reaction produces H_2O during the reaction process.

$$\mathrm{SiF_4} + 2\,\mathrm{HF} \longleftrightarrow \mathrm{H_2SiF_6O} \tag{2.36}$$

$$\mathrm{SiO_2} + 6\,\mathrm{HF} \longrightarrow \mathrm{H_2SiF_6} + 2\,\mathrm{H_2O} \tag{2.37}$$

It was found that the existence of H_2SiF_6 shows a trend to further etching of SiO_2, as shown in Equation 2.38.

$$5\,\mathrm{H_2SiF_6} + \mathrm{SiO_2} \longrightarrow 3\,\mathrm{H_2(SiF_6SiF_4)} + 2\,\mathrm{H_2O} \tag{2.38}$$

Since HF is a weak acid with a logarithmic acid dissociation constant (pKa) value higher than 3 [164], most HF is not dissociated after the reversible dissociation process (Equation 2.39 [165]) has reached equilibrium state. Hence, there are large amounts of HF species in the solution upon the presence of fluoride F^-.

$$HF \longleftrightarrow F^- + H^+ \tag{2.39}$$

HF can react with F^- to produce bifluoride ion, $HF_2{}^-$, as shown in Equation 2.40. This process is called the ionisation of HF.

$$HF + F^- \longleftrightarrow HF_2{}^- \tag{2.40}$$

The entire HF ionisation process is obtained in Equation 2.41 after combining the two reactions in 2.39 and 2.40 with the help of hydronium, H_3O^+ [166].

$$H_2O + 2\,HF \longleftrightarrow HF_2{}^- + H_3O^+ \tag{2.41}$$

The effective etching of SiO_2 is supposed to be the reaction between SiO_2 and the product species after HF ionisation, i.e. $HF_2{}^-$ and H_3O^+. The following Equation 2.42 summarises the SiF_4 generation reaction. The production of these two reactants requires H_2O. Even more H_2O is produced by this reaction itself. This implies that the H_2O involved on the reactant side functions as a catalyst.

$$SiO_2 + 2\,H_3O^+ + 2\,HF_2{}^- \longleftrightarrow SiF_4 + 4\,H_2O \tag{2.42}$$

Balancing the stoichiometric number in products of Equation 2.41 by a factor of two and combining it to reactants of Equation 2.42, the reaction Equation 2.35 can be achieved after simplification. Although only the product H_2O is left after this simplification, H_2O is needed as catalyst.
HF and $HF_2{}^-$ are thought to react with SiO_2 simultaneously and $HF_2{}^-$ is found to be the predominant one. Therefore, in some applications [161], another sort of water solution, which comprises a relatively high contraction of ammonium fluoride NH_4F and low HF, is employed as the etchant in SiO_2 etching. This solution is called **B**uffered **H**ydro**F**luoric acid (BHF). This BHF provides better SiO_2 etching selectivity and it is used to slow down the etching rate to achieve a better control in the etching process.

Stiction In wet etching, the entire structure is rinsed after immersion in the etching solution. This means that the sacrificial layer has a sufficient reaction area to the etching agent, resulting in a rapid reaction. The space of the etched sacrificial layer, which forms a cavity structure, is then filled with the solution-comprising etchant, products and by-products. After wet etching, rinsing in streaming deionised water is typically applied to clean the entire structure. In order to dry the released structure, baking in nitrogen gas flow can be applied. Both heating or reducing the pressure leads to a phase transition from liquid phase to gas phase by means of evaporation, and is commonly used to eliminate the remaining liquid. However, these processes may cause stiction. It occurs at the drying step due to an attractive capillary force induced by the water bridging with a contact angle $< 90°$ (hydrophilic) [65, 167]. In Figure 2.11, stiction is shown for a circular-shaped poly-Si diaphragm structure, which sticks to a Si_3N_4 layer after a wet HF release step.

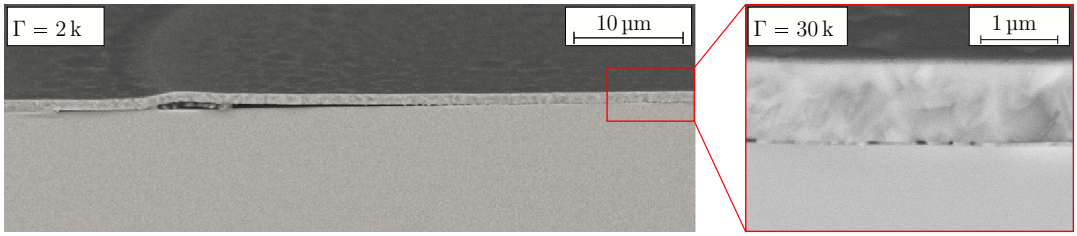


Figure 2.11: SEM cross sections of a circular-shaped poly-Si diaphragm structure sticking to a Si_3N_4 layer after wet HF release, after [168].

A number of methods have been described to counteract the stiction problem, which can generally be roughly divided into two principles [169]: First, methods to prevent physical contact between the structures and the substrate during fabrication by avoiding adhesive and capillary forces that bends the structures into contact with the substrate during the drying process. Second, methods to reduce the adhesive forces, e.g. by minimisation of contact surfaces. Some reported methods from both principles are listed.

- Freeze sublimation drying [170], supercritical drying [171, 172] or media exchange steps comprising substitution, polymerisation and plasma release [173] to avoid the liquid-phase.
- To reduce the wetted area of water bridges, mechanical surface modifica-

tion by stiction reducing bumps [174], surface roughening [175], or side-wall spacers grown partly underneath the structures [176] are utilised for example.

- Chemical surface modifications to create water contact angle $> 90°$(hydrophobic) by coating of self-assembled mono-layer [177] or fluorocarbon [178].
- Employing strongly hydrophilic materials such as Ti or Al_2O_3 [67]
- Elimination of H_2O from etching and cleaning procedures and use of alcohols such as vapour methanol (CH_3OH) instead [179].

All of the processes listed above entail considerable effort because additional process steps or special tools are required, which are rarely used in surface micromachining. Vapour-phase etching is a more elegant solution.

Vapour HF Etching In some articles [69, 71, 180], the vapour HF etching is called anhydrous to distinguish itself from the conventional aqueous immersion method. Actually, applying vapour HF only does not usually effect an etching process. In fact a liquid film needs to be condensed on the surface through adsorption to enable any etching process.
The requirement of this liquid layer is due to the catalytic effect of water in HF etching on silicon dioxide as described before. The ionisation of HF molecule triggers the etching reaction. When the etching reactants are taken to an environment lacking water, the etching rate on silicon dioxide dramatically increases if extra water is injected [181]. Water vapour is mixed with the HF vapour to start the etching reaction. In order to maintain an appropriately high etching rate for a high selectivity, this thin liquid layer must be maintained during this dry etching process. However, the amount of condensed liquid should be under control to avoid stiction caused by excess [69, 70].
The etching process combined with adsorption and desorption can be generalised as follows [163]:

- The surface is exposed to the mixture of H_2O and HF in the vapour phase.
- If the process parameters meet the threshold for condensation, a thin liquid layer forms through adsorption.

- The etching reaction on silicon dioxide begins to occur. By this continuous reaction, the reactants keep being adsorbed to the liquid layer on the surface and undesired products desorb.
- The silicon dioxide layer is etched off. The liquid layer containing reaction products is vaporised after setting proper process parameters.

In fact, the etching mechanism of SiO_2 proceeds in the liquid layer after initial condensation. Then, the mechanism is comparable to that in HF containing wet etching [163] and the etching rate in dependency of the HF concentration is comparable [68]. An increment in the amount of vapour water can shift the critical HF concentration, above which the etching reaction begins to occur, to a lower value [166]. High HF partial pressure is found to have the capability reducing the initial demand of water in the etching reaction [163].
Several kinds of SiO_2 have been investigated [166] for the variation in the aspect of the vapour HF etching performance. Different capabilities to adsorb vapour water onto the surface are assumed to be the key point. The adsorption processes strongly depend on the property of the adsorbent surface. Utilizing this, the critical process parameters are set up to realise selective vapour HF etching among different kinds of SiO_2. Exploiting this mechanism, a high selectivity vapour HF etching of **B**oro**p**hospho**s**ilicate **G**lass (BPSG) over thermal silicon dioxide can be achieved by increasing temperature and decreasing water vapour partial pressure. The adsorption of vapour water on thermal oxide is suppressed at an elevated temperature and reduced water vapour partial pressure. At the same time, BPSG is not significantly influenced by the variation of these two parameters because a $H_3PO_4(H_2O)$ layer forms on the surface, even at 65 °C. The subsequent HF etching reaction strongly relies on the water adsorbed on the surface. So the etching rate on a thermal oxide surface is relatively low compared with that on the BPSG surface at higher temperature and lower water vapour partial pressure. Therefore, a high etch selectivity vapour HF etching on different types of SiO_2 is obtained at this condition [182]. Regarding the etching products, continuous desorption of the major product SiF_4 is vital for the mitigation of residual particles or non-volatile liquids, which are formed by the combination of SiF_4 and H_2O during the period of H_2O residence time [180]. Another major etching product, H_2SiF_6 is only stable in the thin liquid layer. This non-volatile product has to be eliminated by the end of the etching sequence via Equation 2.43 to avoid any

potential residual problems, which might aggravate the undesired stiction effect by adhering the top surface to the lower. The desorption of SiF_4 could promote the decomposition of H_2SiF_6 [163]. However, if H_2SiF_6 remains in the liquid HF/H_2O solution layer, it can reduce the vapour pressure of HF and H_2O vapour above. This supports further condensation of the etching reactant from vapour to the liquid layer [163]. This fact indicates that H_2SiF_6 should be kept in the liquid layer to encourage the adsorption of reactants and should be removed at the terminal stage of the etching process.

$$H_2SiF_6 \longrightarrow SiF_4 + 2\,HF \tag{2.43}$$

An intention of developing a vapour HF etching process in this thesis is to avoid stiction problems. The only methods to eliminate reactants and products from the surface are desorption or evaporation [180]. Otherwise, the conventional methods become necessary, e.g. rinsing in DI water, which may cause stiction problems again. In summary, it is one of the major questions of this thesis, how stiction can be avoided despite the use of H_2O in a vapour-phase etching sequence.

Vapour Etching Tool In this thesis, the isotropic etching of sacrificial layers via vapour etching is performed in the *Sacrificial Layer Release System* from *memsstar*. This system comprises load lock, transfer module and process modules, which are capable of applying either HF, or XeF_2. In the process module chamber for HF, the pressure is controlled by the opening angle of the valve on the tube to the vacuum pump. The gases introduced into the chamber such as HF, H_2, N_2 are controlled by a mass flow controller and H_2O is controlled by a liquid flow meter. N_2 is the carrier gas of H_2O vapour after the water is vaporized. The applied parameters for isotropic SiO_2 etching are summarized in Table 2.5.

While the temperature and total gas flows were held constant, the applied pressure was varied. A higher pressure promotes the condensation of water vapour, as does a lower process temperature [66].

Table 2.5: Basic vapour HF parameters for isotropic SiO_2 etching process and verification of the SiC protection function.

Related gases	Pressure in hPa	Temperature in °C
N_2, HF, H_2O	variable, $\leqslant 26.7$	40

Methods of Dry Etching

Reactive Ion Etching RIE is applied by the use of a single-wafer, multi-chamber platform *MetEtch Precision* 5000 cold wall CVD-system by ***A**pplied **Mat**erials* (AMAT). Processes based on Cl or F are available depending on the target material.

Deep RIE, Bosch Process The Bosch process is a plasma technology which utilises alternating cycles of surface passivation using a C_4F_8 plasma, followed by an SF_6 plasma. This implies a directional ion bombardment to expose a structural layer at the base of the feature and a short (isotropic) etch which deepens the features, without etching the still protected side-walls of the hole. This process is appropriate to obtain vertical high aspect ratios in etching profiles. In each cycle, the isotropic nature of the SF_6 etch can lead to so called scallops. To minimise a parasitic side-effect of mask-undercutting, the etch cycles are limited to an appropriate time to minimise the size of a single scallop associated with each etch cycle. In this thesis, a Tegal 200 SE™ DRIE system equipped with the Tegal ProNova2™ reactor is used to apply DRIE processes for patterning etch-access channels.

2.2.4 Need for Process Development for post-CMOS Integration

Preliminary works at Fraunhofer IMS on post-CMOS fabrication of pressure sensors concentrated on the development of appropriate diaphragm materials made of SiGe and Ge. The mechanical and conductive properties of these materials have been evaluated after integration in an established intermediate CMOS sensor fabrication. In this process chain, wet HF etching was exploited to remove the sacrificial layer through small etch-access channels, which were laterally-arranged. In this intermediate CMOS fabrication, conductive layers were applied afterwards. By contrast, metallisations will be present in post-CMOS sensor fabrication. Therefore, the development of an appropriate post-CMOS fabrication scheme has to pay particular attention to the temperature limitations on the one side, and to the sacrificial layer release processes on the other.
In this thesis, vapour-phase etching was identified as the method of choice, in

order to avoid stiction issues. Unfortunately, the etching rates are relatively low compared to wet etching. This requires design considerations to enable an efficient and quick release process. The requirements are even higher, since high aspect ratios of diaphragm diameter compared to the structure height are required in order to address low pressure ranges.
Further, one has to consider materials for protection of any CMOS substrates from the gaseous release etching. Moreover, covering the open diaphragms after the release etch has successfully been applied, is a challenge. Processes need to be identified, which first enable a sufficient closure of the diaphragm cavity at a minimal process pressure. Second, the deposition within the cavity through the etch access tunnels must be minimised. Third, the cover layer must be chosen compatible to the major diaphragm material. Here, many material characteristics need to match in order to achieve controllable diaphragm characteristics. Amongst others, some of the potential risks are buckling due to compressive stress, gas diffusion or an inappropriate CTE mismatch.

3 Post-CMOS Pressure Sensor Design Considerations

In this chapter, essential design considerations for the sensor elements to be developed are presented with regard to the subsequent integration into a capacitive sensor system. This requires for example specifications regarding the pressure ranges, the wiring of discrete capacitive sensor elements and the interconnection to an array of discrete sensor elements. Such an array defines the nominal capacitances to be connected to a ROIC. Emerging questions regarding the effects of the diaphragm suspension and etch access designs are discussed.

3.1 Specifications and Design

The design of the capacitive sensor elements is based on the presented diaphragm theories in Chapter 2.1.3, which concern the deflection in non-contact and contact mode, as well as the calculation of capacitances in both modes. In Chapter 1.1 the motivation states that the miniaturisation of pressure sensor systems is highly interesting for medical applications such as implants. Pressure ranges around the barometric pressure are of interest, which is for example a range from 800 hPa to 1200 hPa. In addition, other interesting ranges can be found in the ultra-low pressure regime (vacuum). A pressure range from 0.1 hPa to 10 hPa may be attractive for low-cost miniaturised pressure sensor transponder applications. These pressure ranges are primarily, but not exclusively, taken into account in the design of the capacitive pressure sensor elements.

3.1.1 Capacitive Pressure Sensor Elements

As introduced in Chapter 1.1, Figure 1.2, the miniaturisation of MEMS diaphragms for pressure sensor applications approached a ratio of the diaphragm length or diameter over its thickness of 80 : 1. This ratio is regarded as a starting point for design considerations. In this chapter, the following values are used unless otherwise stated: A Young's modulus for SiGe of $E = 149\,\text{GPa}$ [42], a Poisson ratio of $\nu = 0.25$, diameters $2r_0$ of 100 µm, 200 µm and 300 µm, a nominal thickness $t = 1.0\,\mu\text{m} \pm 0.5\,\mu\text{m}$, a cavity height d=1 µm, a thickness of an isolation layer t_{iso}=100 nm $\epsilon_0 = 8.85 \times 10^{-12}\,\text{F/m}$, $\epsilon_{r,iso} \approx 10$, $\epsilon_{r,vac} = 1$.
Equation 2.6 is used to calculate the centre deflection $w_{c,0}$ under the assumption of rigidly-clamped, circular-shaped SiGe diaphragms which are free of intrinsic stress. The results are drawn in Figure 3.1.

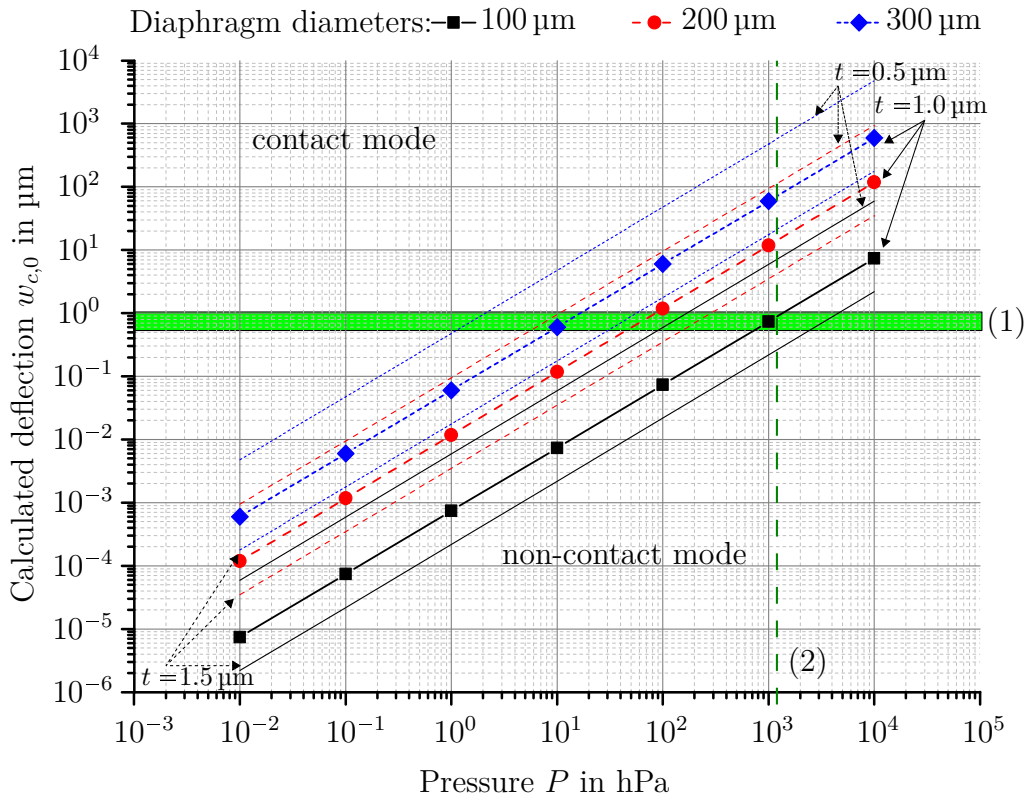


Figure 3.1: Pressure dependent centre deflections $w_{c,0}$ of SiGe diaphragms of different diameters (100 µm, 200 µm and 300 µm) calculated with $E = 149\,\text{GPa}$, $\nu = 0.25$, thickness $t = 1.0\,\mu\text{m} \pm 0.5\,\mu\text{m}$. An appropriate range for the cavity height d (1) and the barometric pressure (2) are highlighted.

Here, (1) highlights an appropriate range for cavity heights. It defines the CPP, at which the centre of a diaphragm touches the bottom of the cavity. The highlighted area also sets the transition from non-contact ($w_{c,0} \leqslant \approx 0.5\,\mu m$ to $1.0\,\mu m$) to contact mode ($w_{c,0} \geqslant \approx 0.5\,\mu m$ to $1.0\,\mu m$). The drawn centre deflections in contact mode are only virtual, because the centre deflection cannot become larger than the cavity height. As described in Chapter 2.1.3, operations in contact mode are interesting due to more linear changes of the sensor capacitance and an increased dynamic range.

It is apparent that diaphragm designs in the drawn range of $100\,\mu m$ to $300\,\mu m$ for the given thicknesses can ideally cover a wide range of absolute pressure. Further, the sensitivities S in terms of deflection per applied pressure can be derived from Figure 3.1. The dynamic ranges for contact mode can for example be evaluated graphically due to the curves shown in Figure 3.2.

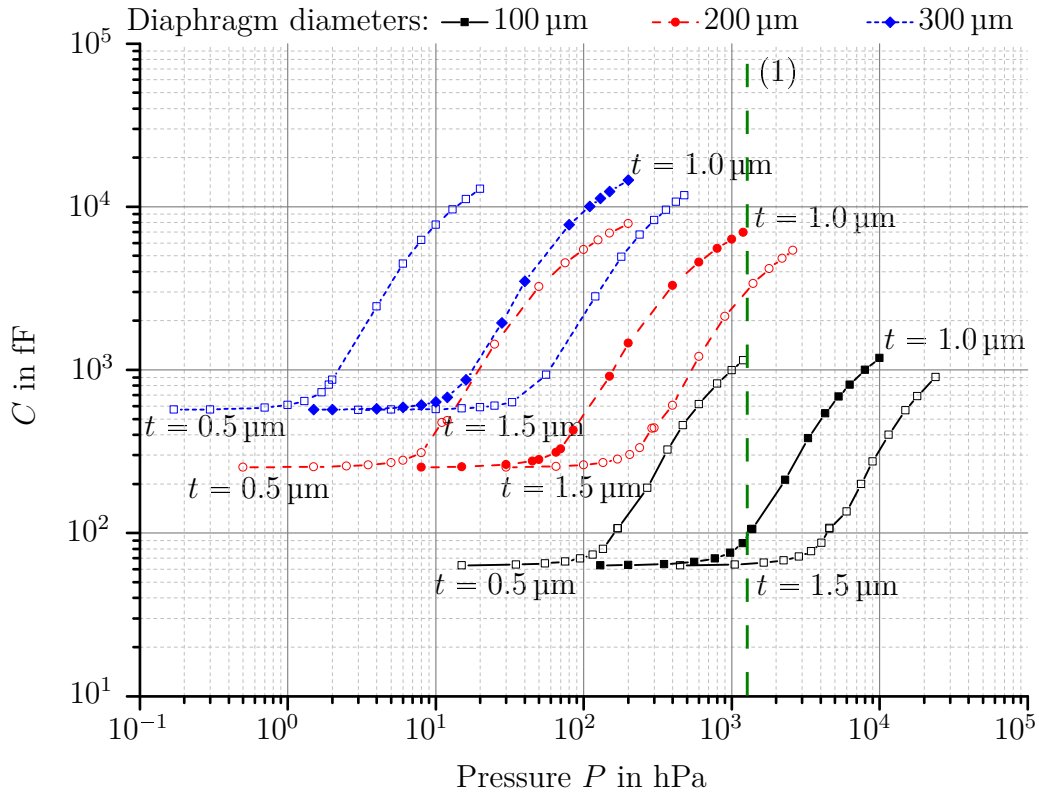


Figure 3.2: Capacitance-to-Pressure characteristics of pure SiGe diaphragms of different diameters ($100\,\mu m$, $200\,\mu m$ and $300\,\mu m$) calculated with $E = 149\,GPa$, $\nu = 0.25$, thickness $t = 1.0\,\mu m \pm 0.5\,\mu m$, cavity height d=$1\,\mu m$, thickness of SiC isolation t_{iso}=$100\,nm$ $\epsilon_0 = 8.85 \times 10^{-12}\,F/m$, $\epsilon_{r,SiC} = 10$, $\epsilon_{r,vac} = 1$. The barometric pressure (1) is highlighted.

Here, the calculated capacitances are calculated for both non-contact (according to Equation 2.8) and contact mode (according to Equation 2.11) considering ideal, stress-free SiGe diaphragms. This Equation additionally requires an indication of the CPPs. The CPPs are set equal to the pressure at a deflection $w_{c,0} = 1\,\mu m$. These are calculated for the example of 1 µm cavity height d according to Equation 2.10. The CPPs can also be read at the top edge of the highlighted area (1) in Figure 3.1, which are in agreement with the calculations. In Figure 3.2, both the operation modes become visible and are separated by the CPP. The linear behaviour of the C-P characteristics in contact-mode decreases for increasing pressure load. The diaphragm displacement is saturated for increasing pressures. To exclude the saturation region from the DR in contact mode, it is defined here as the range in which the coefficient of determination, R^2, for a linear regression is $\geqslant 99\,\%$. The minimum pressure loads in non-contact mode, however, are estimated by a decade shift with respect to the CPP, which is usually an appropriate measurement range for capacitive pressure sensors in non-contact mode (see for example [183]). Finally, the dynamic range in non-contact mode will be limited by the maximum resolution and accuracy of the further signal processing by a ROIC. The dynamic ranges are visualised in Figure 3.3, divided by diameter $2r_0$ and diaphragm thickness t.

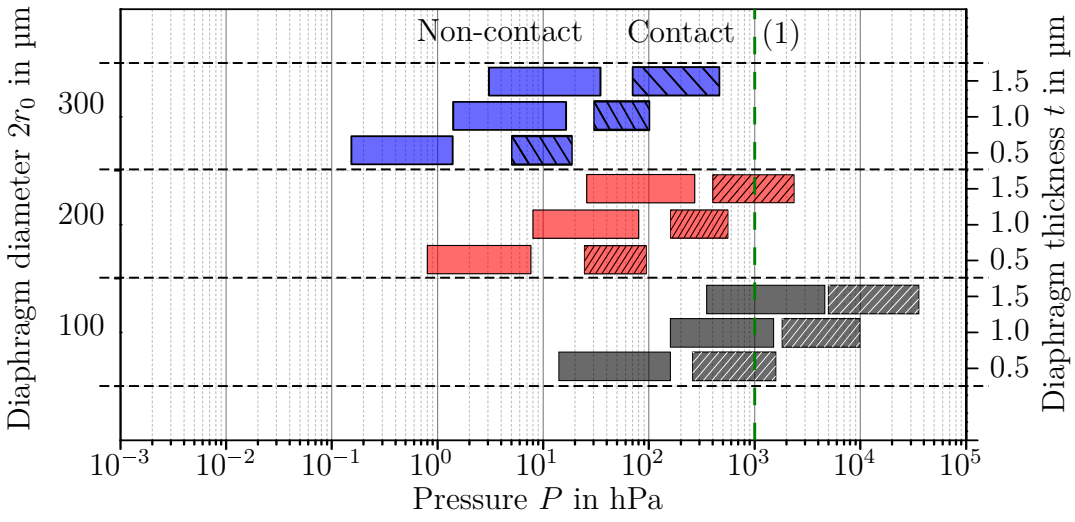


Figure 3.3: Visualisation of dynamic ranges for different diaphragm designs comprising diameters of 100 µm, 200 µm and 300 µm and layer thicknesses t of 0.5 µm, 1.0 µm and 1.5 µm for an assumed cavity height d of 1 µm. The barometric pressure is highlighted (1). Filled bars stand for the DR in non-contact mode and hatched bars for the DR in contact mode.

In Table 3.1 the information provided by Figure 3.3 is listed and supplemented by the sensitivities S and S_C. Again, the information is shown for both operation modes and divided by the intended diameters $2r_0$ and the diaphragm layer thicknesses t.

Table 3.1: Summarised mechanical (S) and capacitive (S_C) sensitivities, CPP at a deflection $w_{c,0} = 1\,\mu m$ and calculated DR of SiGe diaphragms with diameters $2r_0$ of 100 µm, 200 µm and 300 µm and thicknesses t of 0.5 µm, 1.0 µm and 1.5 µm for both non-contact and contact mode.

Diaphragm thickness t in µm				0.5	1.0	1.5
Diaphragm diameter $2r_0$	100 µm	Non-contact	S in nm/hPa	5.9	0.7	0.2
			DR in hPa	15 to 150	130 to 1300	450 to 4500
			S_C in fF/hPa	0.24	0.03	0.01
		Contact	CPP in hPa	170	1356	4577
			DR in hPa	250 to 1200	1400 to 8000	5000 to 25 000
			S_C in fF/hPa	1.0	0.13	0.04
	200 µm	Non-contact	S in nm/hPa	94.4	11.8	3.5
			DR in hPa	0.5 to 10	8 to 80	30 to 260
			S_C in fF/hPa	18.32	1.86	0.61
		Contact	CPP in hPa	11	85	286
			DR in hPa	15 to 100	100 to 830	300 to 2600
			S_C in fF/hPa	57.3	7.3	2.2
	300 µm	Non-contact	S in nm/hPa	477.8	59.7	17.7
			DR in hPa	0.15 to 1.5	1.5 to 15	3 to 50
			S_C in fF/hPa	150.9	17.8	6.4
		Contact	CPP in hPa	2	17	57
			DR in hPa	3 to 17	20 to 150	60 to 470
			S_C in fF/hPa	717.0	88.3	26.0

According to the modelled performance, for example a pressure sensor comprising diaphragms of 300 µm in diameter and a diaphragm thickness of 1.0 µm can be utilised in non-contact mode to measure the pressure in a range from about 1.5 hPa to 15 hPa, or from 20 hPa to 150 hPa in contact mode. Alternatively, a sensor comprising diaphragms of 100 µm in diameter and a layer thickness of 1.5 µm can ideally be used from 450 hPa to 4500 hPa as a barometric sensor,

which operates in non-contact mode. As mentioned before, the contact mode range is defined as the range with a linear coefficient of determination, R^2, of 99 %. This means that the calculated dynamic ranges for the contact mode are not necessarily limited to the listed pressures. It is evident that many pressure ranges can be set by the diaphragm diameters of 100 µm, 150 µm, 200 µm and 300 µm.

It is also clear that the modelling presented here is based on idealised assumptions. The course of process development will show how well these assumptions reflect the real diaphragm characteristics. Significant influences can be expected from the layout of the sensor elements. This layout is presumably influenced by a significant design parameter, the design of the etch access channels.

3.1.2 Design of Etch Access Channels

With respect to the characteristics of vapour-phase release etch technologies, different etch access designs are considered. As described in Chapter 2.2.3, the stiction effect can be avoided by controlling the amount of water in a vapour-phase HF release etch. This is accompanied by a reduction in etching rates. Reported etch rates of vapour HF/H_2O mixtures are for example about 100 nm/ min to 300 nm/ min [184]. This shows that diameters varying from 100 µm to 300 µm could require high durations for complete releases in the range of about 160 min to 1500 min per wafer, if etch accesses are designed as laterally-arranged channels. Because process times of more than 1 h per wafer are rather ineffective, alternative designs of enabling etch access are discussed.

Two basic principles to access the sacrificial layer are to exploit either vertically or laterally-arranged channels. Laterally-arranged channels would require an additional layer spreading to the edge of the electrode. The extra part outside the sacrificial layer bulk is the etching channel opening. In the field of monolithic SoC integration of absolute capacitive pressure sensors, state-of-the-art sealing is established by using such sacrificial etch channels. Here, an advantage regarding the sealing is that isotropic as well as anisotropic layer deposition can be applied without affecting the cavity height at the diaphragm centre point (e.g. [37]). While laterally-arranged channels can be fabricated with relatively low complexity, vertically-arranged etch channels require methods to precisely control the patterning process. Additionally, very small structure widths are required, which

can become challenging because there are limits due to the available lithography. In Figure 3.4 two different etch access designs are shown.

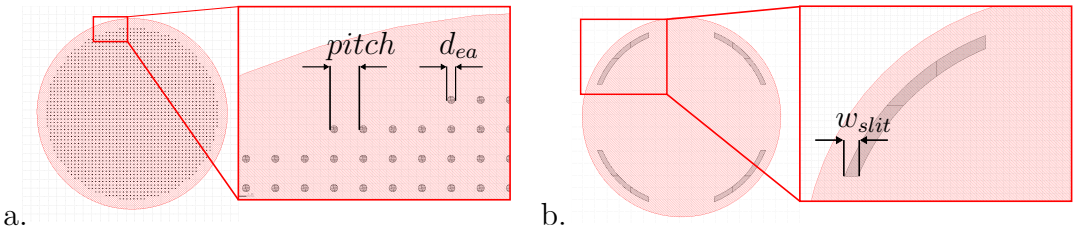


Figure 3.4: Etch access designs of circular-shaped diaphragms with a. surface perforation (via dark-field mask) with a pitch of 2 µm and variable etch access diameters d_{ea} and b. 1/8 circular segments with a radial width w_{slit}.

The design shown in Figure 3.4 a. has circular-shaped etch access channels, which are arranged in a pitch of 2 µm. The etch access channel diameters d_{ea} are scaled to 500 nm ($V2$) and to 700 nm ($V3$), respectively. A darkfield mask layer is required to transfer these structures in a resist. This design is also referred to as surface perforation.

In Figure 3.4 b., circular segments (slits) placed close to the edge of the diaphragm are shown. This option is related to laterally-arranged etch access channels, because a similar distance of undercutting is required. Slits require no additional lithography step, if the width of it, w_{slit} is designed in the µm range. This step is included in a brightfield mask layer for the patterning of the diaphragm layer. These etch accesses may not only be covered, but even be completely filled by anisotropic layer deposition. On the one hand, a filling decreases the effective diaphragm diameters and thus the sensitivity. On the other hand, the process may become simple compared to a surface perforation. Unlike the perforation, a limitation occurs here because the minimum required thickness of the cover layer must be higher than the cavity height. In this case, asymmetry would also arise and the flexible diaphragm area would no longer be circular.

Another design could be an uninterrupted edge perforation, which is a mixture of slits and the surface perforation. On the one hand, this eliminates the advantage of the complexity of the slit design, since an additional lithography step is necessary. On the other hand, there would be no asymmetry if the diaphragms were covered.

In general, the covering of a cavity in absolute pressure sensing should enclose

a very low pressure to provide a reference for pressure measurements. For this purpose etch access channel diameters as small as possible are assumed to be beneficial. However, the smaller the dimensions of these channels, the more complex the processing. Some major advantages of relatively small dimensions of these channels are assumed to be:

- The required thickness of the cover layer is minimised. This is beneficial for the design of a pressure sensor to achieve high sensitivity.
- The deposition of the cover material into the cavity is minimised, so that the maximum diaphragm deflection is not further limited subsequently. Thus the maximum sensor signal is ideally not deteriorated compared to the original design.
- Bi-material effects can be minimised by which a high sensitivity can be ensured.
- A minimised area of etch accesses maximises the area of the sensitive capacitor electrode. For example, vertical etch access channels arranged in a pitch of 2 µm generate more than 11 000 channels on a diaphragm with a diameter of 300 µm. An etch access channel diameter d_{ea} of 500 nm reduces the capacitor area by about 5 %. [185].

In Table 3.2 some characteristics of the discussed etch access designs are assessed. Even though the design of laterally-arranged etch access channel combines several advantages, the surface perforation is most probably to prefer. By this, high etchant media consumption can be avoided to completely release the diaphragms with diameters greater than, for example, 100 µm. An array of vertically-arranged etching channels with a high density is assumed to effectively accelerate the release process from hours to a few minutes per wafer. Nevertheless, all these design variations are considered for the layout of the maskset presented in Chapter 3.1.3 for experimental verification.

3.1.3 Maskset and Sensor Layout

The considered range of diaphragm diameters from 100 µm to 300 µm is implemented as a mask set. A die area of 2 mm x 2 mm and the amount of discrete

Table 3.2: Evaluation matrix of different etch access options.
++ = very good; + = good; 0 = medium; − = moderate; −− = bad.

Evaluation Criteria	Etch access channels			
	Lateral:	Vertical:		
	Channels	Slits	Surface Perforation	Edge Perforation
Process complexity	+	++	0/+	+
Production complexity	+	+	+	+
Diaphragm coverage	++	−	+	++
Impact on mechanical stress	+	+	−	0
Impact on sensor signal	++	−	0	+
Release etch	−−	−	++	−

diaphragms per array are chosen to match the area and possible input capacitances of a ROIC labelled as *IMS-CAP51*, which has been developed by Fraunhofer IMS [183] in parallel to this thesis. This is a readout circuit for capacitive MEMS sensors such as accelerometers, gyroscopes or pressure sensors. A flexible interface makes it possible to connect a wide range of types of capacitive sensing elements. The ROIC was designed with focus on ultra-low noise operation and high analog measurement performance. Thus it enables full-scale measurement ranges from ±750 fF to ±3 pF, depending on the gain. Excluding the pad frame, a reduced area of about 3.1 mm x 3.1 mm can potentially be utilised by post-CMOS sensor fabrication. Unfortunately, no discrete capacitive sensor elements are evaluated with this ROIC yet. The reader is referred to Appendix A for more information about the ROIC.

The layout of arrays to be connected to the ROIC is based on the modelled capacitive characteristics of the capacitive sensor elements with diaphragm diameters $2r_0$ of 100 µm, 200 µm and 300 µm and thicknesses t of 0.5 µm, 1.0 µm and 1.5 µm for both non-contact and contact mode. The results for the dynamic ranges and the sensitivities presented in Table 3.1 are used to calculate the full-scale signal of a single sensor element in pF. Dividing the full-scale measurement range of ±3 pF by the obtained value, the amount of maximum sensor elements to connect to the ROIC can be calculated. For each diameter, the minimum number for the maxi-

mum sensor elements should be considered to deal with the potential variations in diaphragm thickness, t. Thus, in non-contact mode, one obtains 150, 27 and 16 sensor elements per array for the corresponding diameters of 100 µm, 200 µm and 300 µm. In contact mode, however, one obtains 5, 1 and 0 sensor elements

Table 3.3: Calculation of array sizes comprising capacitive sensor elements with diaphragm diameters $2r_0$ of 100 µm, 200 µm and 300 µm and thicknesses t of 0.5 µm, 1.0 µm and 1.5 µm for both non-contact (N.-C.) and contact (C.) mode. The arrays should be able to be accommodated on an area of about 2 mm x 2 mm.

Diaphragm thickness t in µm				0.5	1.0	1.5
Diaphragm diameter $2r_0$	100 µm	N.-C.	Full Scale in pF	0.04	0.04	0.04
			# of max. Sensor Elements	150	150	150
		C.	Full Scale in pF	1.04	0.89	0.80
			# of max. Sensor Elements	5	6	7
	200 µm	N.-C.	Full Scale in pF	0.22	0.17	0.19
			# of max. Sensor Elements	27	35	31
		C.	Full Scale in pF	5.0	5.2	5.0
			# of max. Sensor Elements	1	1	1
	300 µm	N.-C.	Full Scale in pF	0.30	0.30	0.36
			# of max. Sensor Elements	20	20	16
		C.	Full Scale in pF	10.3	13.7	10.8
			# of max. Sensor Elements	0	0	0

per array for the corresponding diameters of 100 µm, 200 µm and 300 µm. This means that the capacitive change for the calculated dynamic range is too high to be completely covered. Nevertheless, either by measuring over smaller pressure ranges, or because of an reduced sensor signal due to parasitic effects, the sensor elements will be possible to use. There are many potential parasitic effects to be considered, which are for example:

- The intrinsic layer stress, which can inhibit sensitivity and deflection range according to the Equations 2.15 to 2.19.
- The variation of the isolation layer thickness, t_{iso}, scales linearly with $1/t_{iso}$ in contact mode according to Equation 2.11. This layer could for example be affected by the diaphragm cover, which can potentially show depositions inside the cavity.

- The loss of capacitor area depending on the etch access design.

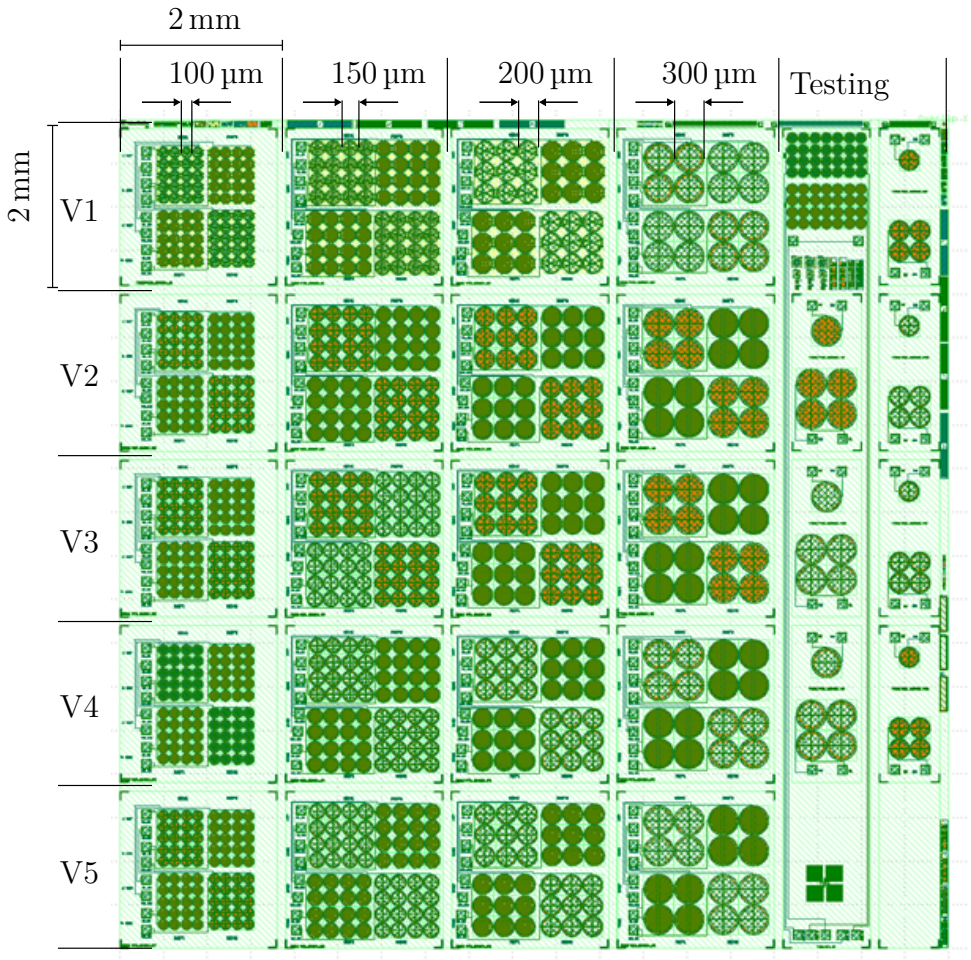


Figure 3.5: The developed maskset contains 8 layers to realise capacitive pressure sensor elements, which vary in terms of the diaphragm diameters (100 µm, 150 µm, 200 µm and 300 µm) and in the etch access designs ($V1$ to $V5$).

Therefore, in the layout shown in Figure 3.5 a slightly increased number of sensor elements per diameter has been taken into account. For sensor elements with diameters of 100 µm, 200 µm and 300 µm the corresponding numbers of sensor elements are 25, 9 and 4. In addition, 150 µm diameters are included with 20 sensor elements according to similar calculations. The arrays are duplicated in order to comprise 2 of them per die. These can be connected optionally, depending on the realised capacitances and the interconnection scheme. Moreover, arrays of the same amount comprising insensitive sensor elements are implemented. These elements can potentially be used for half-bridge circuits to compensate temperature effects, which also cause a change in the diaphragm deflection.

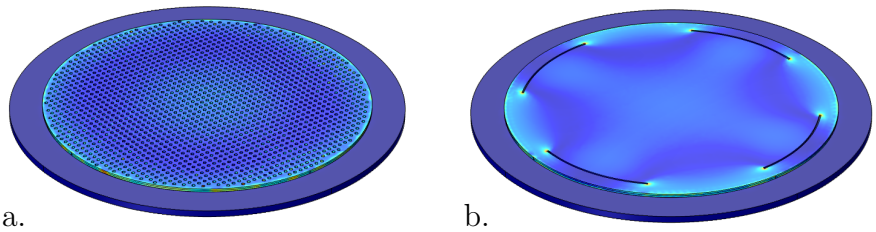
The versions $V1$ to $V5$ refer to different designs regarding the etch access channels. Laterally-arranged channels ($V1$), surface perforations ($V2$, $V3$), edge perforation ($V4$) and slits ($V5$) are implemented. For the further evaluation in this thesis, $V2$ to $V3$ are most relevant. These comprise vertically-arranged etch access channels with both a pitch of 2 µm and etch access channel diameters d_{ea} of 500 nm and 700 nm, respectively. These diameters are chosen due to the limitation in lithography, even though, smaller diameters are highly desired.
The wiring is optimised to realise different interconnection options for different types of sensing elements, as for example a single ended sensing element (after [183], shown in the Appendix in Figure A.2).

3.2 Simulation

In this section the issues of etch access designs and the diaphragm suspension are evaluated in the COMSOL Multiphysics® software V4.4.

3.2.1 Simulation of Etch Access Designs

Simulations of single circular-shaped diaphragms, both with a diameter of $2r_0$ 100 µm, a thickness t of 500 nm, built on crystalline silicon, are evaluated. Figure 3.6 shows two different designs. In Figure 3.6 a. a pitch of 2 µm between the vertically-arranged etch access holes is designed and the effective diameter of the circular-shaped etch access channels d_{ea} is varied. In Figure 3.6 b. a design comprising four 1/8 circular segments as etch accesses is sketched.



a. b.

Figure 3.6: A virtual load of 1500 hPa is applied to diaphragms of both 100 µm in diameter, 500 nm in thickness, 500 nm cavity height, placed on a substrate of crystalline silicon. a. obtains vertical arranged etch access channels with variable diameters and a constant pitch of 2 µm, b. shows a design with four 1/8 circular segments as etch access.

In order to determine the impacts of different etch accesses, these designs are

evaluated regarding stress. For this purpose, the diaphragms are rigidly clamped into place and subjected to pressure. A distributed load of 1500 hPa is applied virtually. For the design of any low pressure sensor it is reasonable to define a maximum load of slightly higher than 1 atmospheric pressure (about 1015 hPa), which corresponds to the storage conditions of these sensors. Figure 3.7 illustrates the maximum von Mises stresses of the diaphragm area.

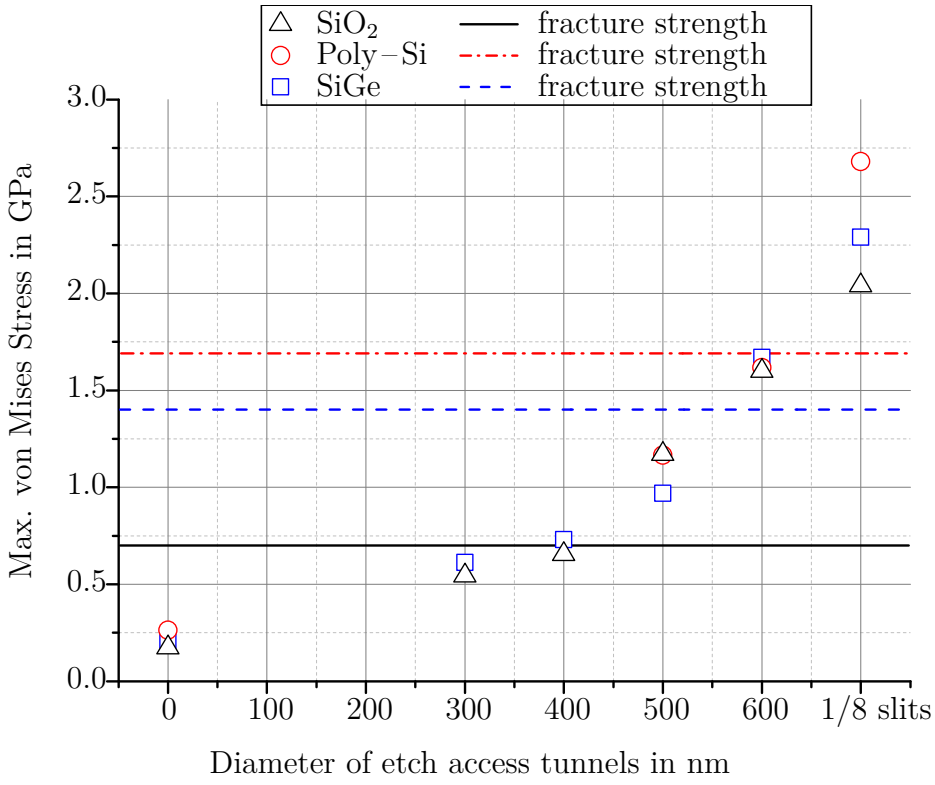


Figure 3.7: Design of etch access is plotted versus the maximum von Mises stress for a virtual load of 1500 hPa and compared to the fracture strengths of SiO_2, poly-Si and SiGe with high Ge proportion. The diameters of the diaphragms, $2r_0$, are 100 µm, the thickness t is always designed as 500 nm.

Different diameters of the etch access channels are evaluated (0 nm, 300 nm, 400 nm, 500 nm and 600 nm). As Diaphragm materials, SiO_2 and SiGe with high Ge proportion ($\geqslant$90 %) [146] are considered. The SiO_2 is considered in order to investigate whether a SiO_2 diaphragm supported by a very thin subjacent metal layer is an alternative. Thin subjacent metals could be TiW or TiN to form an electrode in the capacitive pressure sensor.
The stress values are compared to the corresponding fracture strengths, which are

commonly about 1 % of the Young's modulus (i.e. 0.7 GPa for SiO_2 and 1.4 GPa for SiGe [146], respectively). The simulations of the maximum von Mises stresses of different membrane designs show that a reduced size of etch access channels is very beneficial to increase the fracture strength. Diameters of 0.4 µm (pitch: 2 µm) or less limit the maximum stress in a diaphragm to approximately half the fracture strength of SiGe. Due to the lower fracture strength of SiO_2, here, a much thicker sealing layer would be required even for etch access channel diameters of 0.4 µm and lower. The resulting maximum stress values are too close to the fracture limit. For this reason, the idea of an SiO_2 diaphragm supported by a thin metal layer is no longer being pursued.
The design of 1/8 circular segments (slits) is different. Due to the placement at the areas of maximum stress, these etch accesses should not only be sealed, but be completely filled by methods of anisotropic layer deposition. On the one hand, this decreases the effective membrane diameters and thus sensitivity; on the other hand, the maximum stress would be far below the fracture strength, because there is no more deflection at this area of the diaphragm. Consequently, the etch access area would rather strengthen the diaphragm suspension.
In fact, the simulation concerned open diaphragms. This represents the case of a cover layer with a minimal thickness. The thicker the final cover layer, the more dominant its influence will become. For an ideal filling of the etch access channels, the mechanics of the design will probably be similar to a closed surface. This case is represented by a diameter of the etch access channels equal to zero and should always be pursued.

3.2.2 Diaphragm Suspension

So far, ideal rigid clamping is assumed for the diaphragm suspension. However, if a sacrificial layer is patterned by methods of surface micromachining before the diaphragm layer is deposited, the suspension can differ from ideal clamping. For this reason, the stress distribution at the edge of a diaphragm is evaluated for different side wall angles. The impact of the side wall angle regarding the maximum von Mises stress at the edge of circular-shaped diaphragms is evaluated by simulation.
A diaphragm is designed with an outer diameter of 100 µm, and both a diaphragm layer thickness and a cavity height of 1 µm. Selected materials are SiGe for the

diaphragm structure and Si for the substrate. In Figure 3.8 a. the results of a variation of the side wall angle α is shown. The absolute values for the maximum von Mises stress should be considered in relation to the step coverage at the edge of a diaphragm, which depends on deposition parameters. Nevertheless, an optimum can be found for a side wall angle of about 50° with a von Mises stress of about 0.21 GPa [185]. In Figure 3.8 b. the stress distribution is shown for a side wall angle of 45° and a conformity 9/10 of width/height under an applied load of 1000 hPa.

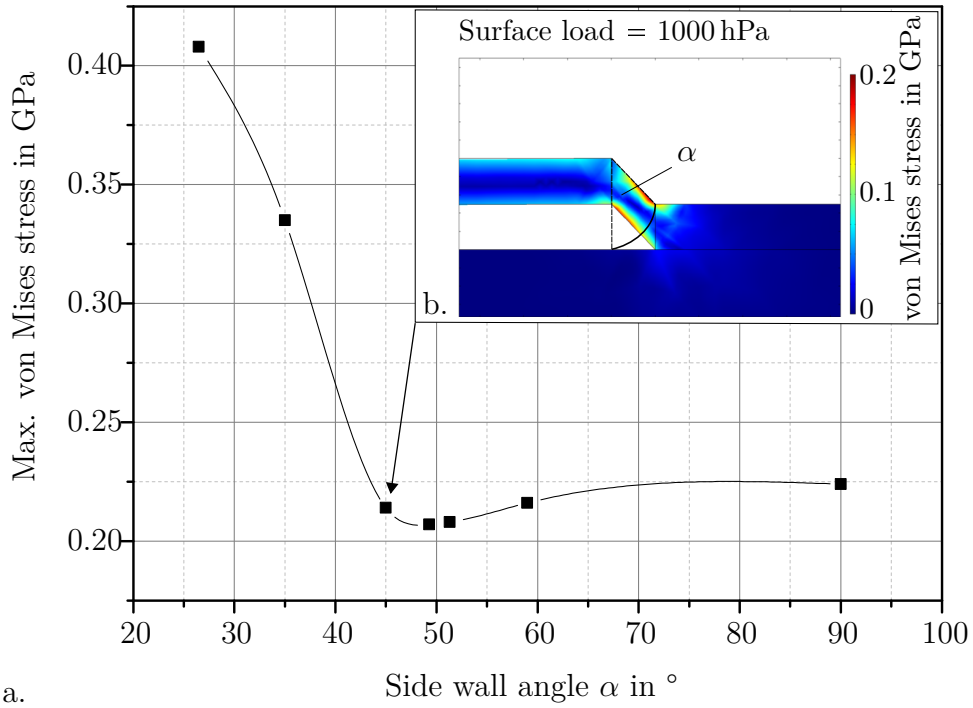


Figure 3.8: a. Results of a variation of the side wall angle α from 26° to 90° for diaphragms with a diameter of 100 µm, and a diaphragm layer thickness and a cavity height of both 1 µm. The here applied load is 1000 hPa. b. Von Mises stress distribution at the edges of a single diaphragm with an assumed 9/10 conformity of the step coverage, after [185].

3.2.3 Diaphragm Deflection due to Residual Stress

Residual stress is the stress that occurs in a material due to the fabrication process. It is primarily promoted by the intrinsic stress and thermal stress. Other sources include impurities introduced during the deposition process, process variations, and interstitial atoms or vacancies in the crystal lattice. Even if measured values for an arbitrary layer are moderate (e.g. some 100 MPa), thin films can

nevertheless suffer from excessive stress gradients. These can cause harmful effects of bending on comb-drive actuators etc. that require coplanar structures. The theoretical basis regarding the effects of residual stress is described in Chapter 2.1.3. There it is shown that especially compressive stress should be avoided to prevent buckling of the diaphragms. As for example demonstrated in [42], the suspension of diaphragms should also be considered regarding the deflection due to intrinsic layer stress. Before, a side wall angle of about 50° was determined to be appropriate. Diaphragms with properties of SiGe, diameters $2r_0$ of 100 µm and 200 µm, a thickness t of 1 µm and a suspension with an optimum side wall angle are simulated, whereby the intrinsic stress is varied. The results are shown in Figure 3.9.

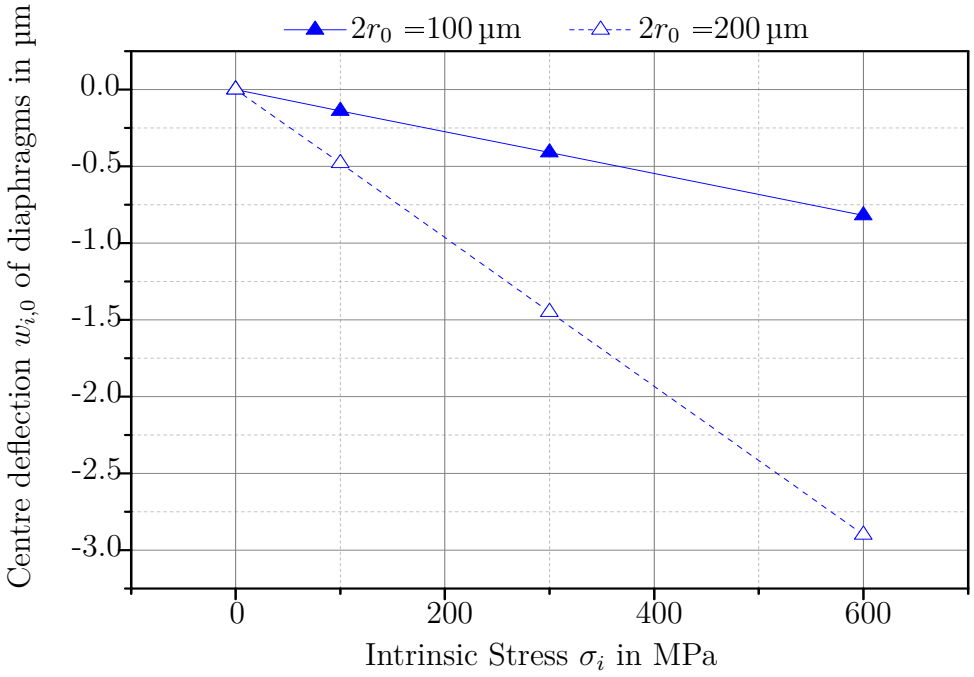


Figure 3.9: Centre deflection $w_{i,0}$ due to intrinsic tensile stress of a SiGe diaphragm diameters $2r_0$ of 100 µm and 200 µm, a thickness t of 1 µm and a side wall angle of about 50°.

It becomes clear that the residual stress should be well controlled. Otherwise, excessive, stress-induced diaphragm deflection can easily occur, reducing the dynamic range. The used PECVD in-situ boron-doped SiGe is expected to show a light tensile intrinsic stress of less than 100 MPa [42]. For example, for a diaphragm with a diameter of 200 µm, the dynamic range in deflection is reduced by about 50 % for a cavity height of 1 µm, if the intrinsic stress is about 100 MPa.

4 Development of a post-CMOS Pressure Sensor Technology

In this thesis a process scheme is developed to fabricate capacitive pressure sensor elements by methods of post-CMOS surface micro machining process techniques. The primary objective in the post-CMOS processing of the MEMS is to avoid inhibiting the properties of the CMOS substrate. As described in Chapter 3.1 on Page 51, the limitations in the applicable temperature budget and the required protection from etch and deposition steps to fabricate a sensor on top of the CMOS substrate have to be considered in particular.

The processes used for the developed process chain will not exceed a maximum temperature of about 380 °C. The cumulated duration of substrate exposure to 380 °C is considerably less than 15 min. Integrated on a CMOS substrate, the technology comprises 6 photolithographic masks. Regarding the connection to a post-CMOS MEMS system, either bond-wires or **T**hrough-**S**ilicon **V**ias (TSV) can be utilised. If a CMOS substrate provides TSV for 3D integration a priori, the number of required masks for MEMS fabrication will be 5 only.

In Chapter 3.1.3 a maskset is introduced for the fabrication of capacitive pressure sensor elements comprising diaphragms with diameters of 100 µm, 150 µm, 200 µm and 300 µm. Further, lateral (channels, extra mask-layer) vertical (slits, channels of 500 nm and 700 nm in diameter and a pitch of 2 µm) designs regarding the etch-access are implemented. Next to sensitive diaphragms, significantly less sensitive diaphragms are also implemented. Pillars below the diaphragm reduce its sensitivity without having to adjust the layer thickness.

4.1 Conceptual Developments

In this chapter, first, a concept for post-CMOS integrated, absolute capacitive pressure sensor is presented. Second, a concept for the fabrication of stand-alone absolute capacitive pressure sensor elements to be connected via wire-bonds is developed. The process flow of this concept and the identified major issues are discussed. Finally, an optimised process flow is presented. The major developments and challenges of this thesis are further summarised. These are primarily the 1st MEMS wiring level, an isolation and protection layer, the sacrificial layer technology and etch-access options, the development of a sub-process chain for a MEMS-specific side-wall spacer, the closure of open diaphragms and a bond pad metal stack.

4.1.1 Post-CMOS integrated Capacitive Pressure Sensor

The superior objective of the technology development to fabricate a capacitive pressure sensor adapted for post-CMOS integration is to equip most of the area of an appropriate CMOS IC. Ideally, the post-CMOS technology will be compatible with any CMOS technology and only design adaptions will be necessary to combine MEMS and CMOS in this way.
In Figure 4.1 a schematic cross-section of an integrated post-CMOS pressure sensor is shown. A CMOS substrate with for example 3 metal layers (1) fabricated in any standard CMOS technology is drawn. An ideal starting point for post-CMOS MEMS processing would be a flat surface. CMOS IC surfaces, however, do not show flat surfaces. Instead, the different overlaying metal layers cause unevenness of the surface in the range of some hundreds of nm to some µm. Therefore, the CMOS substrate should be supplemented by an adapted interface layer (2) comprising a maximum degree of filling with the 3rd metal layer, a dielectric layer, which is planarised via CMP, and a 4th metal layer. The 3rd and 4th metal layers are electrically connected via metal interconnections, subsequently referred to as plugs, and thus, connected to the subjacent CMOS IC. As described in Chapter 2.2 on Page 31 et seq., the interface can be entirely implemented with standard CMOS processes without limitations to the IC fabrication [113].

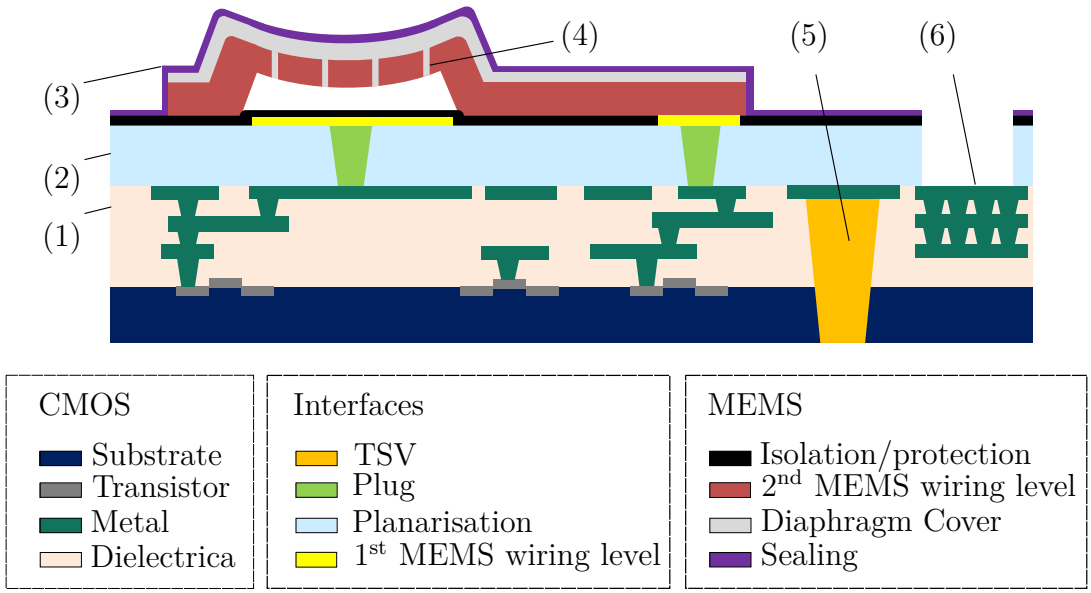


Figure 4.1: Schematic cross-section of an integrated post-CMOS pressure sensor (not to scale): (1) CMOS substrate with 3 metal layers, (2) interface layer comprising a planarisation with plugs and a 4th metal layer as 1st post-CMOS wiring level, (3) sealed diaphragm with indicated etch-access channels (4); potential electrical interfaces of the system be TSV for a back-side contacts (5), or open pads for wire bonds (6).

This is where the post-CMOS processes fabrication of the MEMS (3) begins. The 4th metal layer can for example be utilised as 1st post-CMOS wiring level to form the 1st MEMS electrodes and the wiring. Then, a dielectric and protective layer is deposited. The function of this layer is not only electrical isolation of two MEMS electrodes, but also provides media resistivity for the later application of a sacrificial layer release.

This is followed by the deposition and the patterning of a sacrificial layer. By this means, the distance of the capacitor electrodes of the pressure sensor element is defined. Furthermore, the side angle of the patterned sacrificial layer needs to be considered since the further layers form the diaphragms. The side angle affects the diaphragm suspension and thus the boundary conditions of the diaphragms. Here, mechanical and intrinsic stress, fracture strength and the shape are major issues. Smooth side wall angles smaller than 90° are desirable to minimise parasitic mechanical effects.

Further, a 2nd MEMS wiring level is formed and connected to the CMOS IC at appropriate positions. Particularly at this level, there is the need for a material with appropriate electrical and mechanical characteristics since the major layer

of the pressure sensitive diaphragm is formed as well.
First, this formed diaphragm structure has to be released. There are different ways to design etch accesses. In Figure 4.1, vertically-arranged etch-access channels are indicated (4) to remove the sacrificial layer and release the major diaphragm layer. Second, the now released diaphragm is an open, residual-free, and free-standing structure. By a subsequent layer deposition at a pressure some magnitudes smaller than the intended working pressure of the sensor, the etch-access channels have to be filled and covered. While the layer deposition process covers the etch-access channels at a certain pressure, the process gas becomes trapped in the cavity, which is the volume between the capacitor electrodes of the pressure sensor. Finally, the diaphragm is flexible according to applied pressure changes by the environment.
The top layer drawn Figure 4.1 represents sealing and optional surface functionalisation. A required characteristic is a minimal gas permeability of the diaphragm structure to assure a minimal drift behaviour, for example. Other desired functions of a top layer could be light shielding, improved bio-stability and -compatibility or controlled adhesion characteristics for further encapsulations.
As electrical connections, TSV for back side contacts (5), or surface openings to access pads (6) for wire bonds are possible to connect the post-CMOS MEMS.

4.1.2 Post-CMOS compatible Capacitive Pressure Sensor Elements

As described in more detail in Chapter 2, a temperature budget of 455 °C for ⩽5 h for a post-CMOS SiGe pressure sensor fabrication is reported to be tolerable in a 0.13 µm Cu-based CMOS technology [43,72]. The maximum applied temperature in this thesis is 380 °C for far less than 15 min. For this reason, the major focus is on the process development for the MEMS process itself with respect to the temperature budget and the pressure sensor design for improved sensor performance compared to [43, 72]. In this thesis, capacitive pressure sensors elements are therefore fabricated as stand-alone MEMS adapted for the post-CMOS integration. The CMOS integration of these sensor elements goes beyond this thesis. Unlike what is shown in Figure 4.1, the discrete MEMS additionally requires a

bond pad to enable electrical connectivity for evaluation purposes. In Figure 4.2, a schematic cross-section of the designed outcome of this thesis is shown not to scale. The developed process scheme enables the fabrication of absolute capacitive pressure sensitive elements, which are scalable for different pressure ranges by design and layer properties.

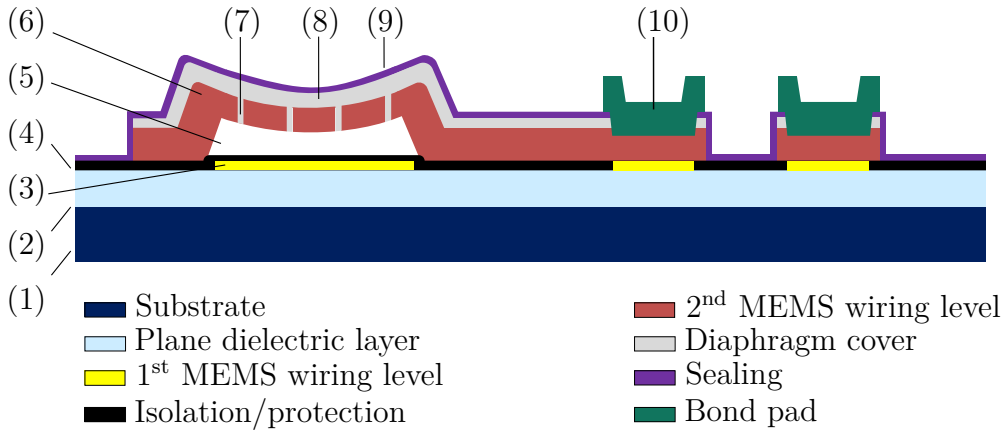


Figure 4.2: Schematic cross-section of capacitive pressure sensor structures (not to scale) adapted for the post-CMOS integration.

To enable diaphragm structures with significantly lower pressure sensitivity but comparable values of the nominal capacitance for compensation measures in the sensor system circuitry, only slight variations in design are suggested. Analogous to Figure 4.2, a schematic cross section is drawn in Figure 4.3.

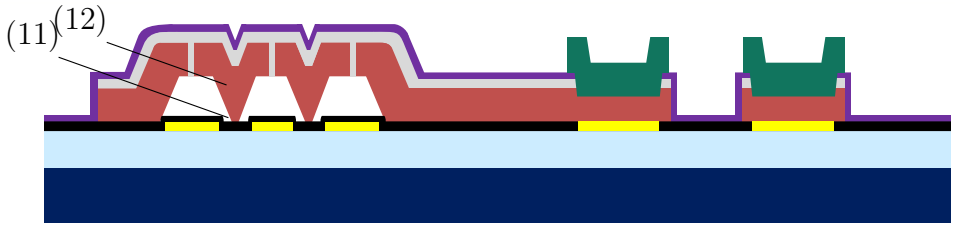


Figure 4.3: Schematic cross-section of a diaphragm structure with inhibited pressure sensitivity (not to scale): the 1st MEMS wiring level is equipped with recesses (11) where the pillars (12) are drawn.

For example, pillars could be placed within the diaphragm area due to recesses in the mask layer of the sacrificial layer. Further, to avoid large parasitic capacitances, the 1st MEMS wiring level should be supplemented by recesses (11),

where the pillars (12) are placed within the diaphragm area. These measures will inhibit the diaphragm to deflect and it can thus serve as a reference element.
In Figure 4.2 different layers and structures are drawn and labelled with numbers, which correspond to the following listing. The layers are explained in more detail, and the results of the corresponding developments of this thesis are summarised.

(1) Substrate: The processes are developed with 200 mm reclaimed p-doped bulk-Si substrates with a thickness range of 685 µm to 725 µm.

(2) Plane dielectric layer: Unless specified differently, the substrate is equipped with an **U**ndoped **S**ilicate **G**lass (USG) layer (2), which is usually used as **I**nter-**M**etal **D**ielectric (IMD) and deposited via PECVD. This ensures sufficient isolation from substrate and appropriate surface characteristics to evaluate important parameters such as adhesion and protection functions of the following layers.

(3) 1st post-CMOS wiring level: The choice of the 1st post-CMOS wiring level is developed with respect to a high conductivity and an appropriate contactability to SiGe, which is the material of the 2nd MEMS wiring level.

(4) Isolation/ protection: A protection of the 1st post-CMOS wiring level and all subjacent layers (including the CMOS circuitry) becomes necessary since a highly reactive sacrificial layer-releasing process by the use of **V**apour **H**ydro **F**luoric acid (vHF) is applied two steps later. Because the sacrificial layer must have a high selectivity towards the layer underneath to avoid the formation of potential by-products, the protection layer must show characteristics of an etching barrier. Some frequently used insulating materials, for example nitrides, have been proven inappropriate [122]. However, silicon carbide (SiC) has attracted attention due to its advantages in thermal stability, hardness, wear resistance and chemical stability [124, 125]. SiC also shows potential as electrical isolation material because of the wide band gap around 3 eV [124, 126]. In this thesis, a low temperature SiC process is developed as a protection layer. A SiC layer thickness of about 100 nm is proven to be sufficient to protect for example SiO_2 from a vapour HF attack in a wide process range from 6.7 hPa to 26.7 hPa. A minimal protection layer thickness is desired to enable short distances between the capacitor electrodes of the pressure sensor structures. Thus, a high net change

in capacitance is possible. Furthermore, SiC can also be used in vapour XeF_2 etching processes, if amorphous Si is utilised as sacrificial layer. The developed SiC protection layer, comprised of Si, α–SiC ($4H$, $6H$, $8H$) and amorphous SiC, is formed with a deposition rate of about 3.3 nm/ min. The development is described in more detail in Chapter 4.2.1.

(5) Cavity: The cavity is the free space between the capacitor electrodes formed by the 1st and 2nd MEMS wiring levels where a lithographically patterned sacrificial layer was present before. The characteristics of the cavity are mainly determined by the sacrificial layer. Height, diameter, material, etch access, the release etch and the way of covering influence the cavity characteristics. The cavity height is varied in a range of 500 nm to 1000 nm according to the design considerations in Chapter 3 and with respect to the varied cover process. Another important characteristic of the sacrificial layer is the side-wall angle, which affects the stress distribution in the diaphragm. In order to adjust the side wall angle, a variation of the focus for resist exposure is performed.

(6) 2nd MEMS wiring level: SiGe is the preferred material to form the 2nd MEMS wiring level. In preliminary works at Fraunhofer IMS, low temperature PECVD of in-situ boron-doped SiGe and Ge layers in a range of 340 °C to 375 °C have been developed as a process module to be utilised in a post-CMOS pressure sensor fabrication [42, 146]. The SiGe layer can be deposited as amorphous or polycrystalline material depending on the quantity of the total gas flow. The increased total gas flow favours the crystallisation of the deposited SiGe or Ge layers. This effect is attributed to the reduced gas residence time. The reduced residence time improves the crystallisation of the deposited layers by increasing the Ge content in the layers (in the case of SiGe layers) and probably additionally through increasing the GeH_3 and SiH_3 radicals in the plasma [146]. With the deposition method with increased total gas flow, poly-SiGe and poly-Ge layers with very low resistivity (about $10\,\Omega\,mm^2/m$) can be deposited at very low substrate temperatures (poly-SiGe: 375 °C; poly-Ge: 340 °C). These layers have small tensile stresses, which is highly desirable for the initial deflection of pressure sensor diaphragms.

(7) Etch-access channels: Two basic principles to access the sacrificial layer are vertically and laterally-arranged etch-access channels. The issue of etch accesses and release processes is a major development task in the present work. The design of the etch-access channels has to be considered thoroughly with respect to the diaphragm characteristics such as the mechanical sensitivity, the resulting electrode area, or the fracture strength. Moreover, influences on processes are identified, such as effects on the overall etch rate of the sacrificial layer and the occurrence of stiction. As described in the Chapter Sacrificial Layer Etching on Page 43 et seq., in vapour-phase etching with HF, the etch rate correlates with the amount of condensed water at the surface which is directly linked to the process pressure. However, more water is in turn found inconvenient as it promotes the stiction effect [65, 69, 70]. Especially capacitive sensing structures show a potential risk because the capacitor areas are large while the distance between the electrodes should be small, ideally. Consequently, vertically-arranged etch-access channels seem to be the best trade-off regarding stiction-free vapour-phase release processes with sufficient overall etch rates. The choice of etch-access channels further affects the capping of release diaphragms. Vertically-arranged etch-access channels are, unlike laterally-arranged ones, a greater challenge to the capping for at least two reasons: First, the required thickness of the diaphragm cover correlates with the cross-sectional geometry of the etch-access channels. It shall apply regardless of the capping process: The larger a channel geometry, the higher the required cover layer. Second, the cavity can be filled at the same time. A filling would inhibit the displacement of the flexible capacitor electrode and, thus, reduce the dynamic range. The cavity height is designed in the magnitude of 1 µm and less for a higher dynamic range. As a first approach to counteract the problem of filling the cavity while capping the diaphragm, the vertical etch-access channels should be designed much smaller in diameter than the cavity height. This example illustrates the benefits of the smallest possible etch-access channels. Therefore, a side-wall-spacer process to minimise the diameter of vertical etch-access channels is developed after [186]. By using two temporarily applied SiO_2 hardmasks, the diameter of lithographically structured channels is effectively reduced [187]. These hardmasks are removed in-situ with the sacrificial layer by vapour HF and do not require any additional etching step. The development of this sub-process chain will be described in Chapter 4.2.3.

A third, different principle is to exploit porous layers through which the vaporous etch media as well as the etching products can diffuse [188]. The idea is that a porous etch-access layer is an advantage in layer deposition to close the diaphragm. The porous etch-access layer should prevent a deposition inside the cavity and, thus, promote the capping. A post-CMOS compatible, nanoporous ALD composite layer consisting of Al_2O_3 and ZnO is developed, which is selectively etched by vapour HF, which can be implemented in an in-situ sacrificial layer release process [189]. This method is described in Chapter 4.2.5.

(8) Diaphragm Cover: The etch-access channels of the diaphragms have to be covered to enable pressure-dependent deflections of the diaphragms. The major challenges are identified as intrinsic stress control to maintain the desired shape of the open diaphragm, and cavity filling. Adding a cover layer to the diaphragm creates a multilayer diaphragm. The cover layer becomes a 2nd diaphragm layer with a significant layer thickness and, therefore, delivers a considerable contribution regarding the intrinsic stress. The required layer thickness is dependent on the applied design of the etch-access channels. For example, vertically-arranged, circular-shaped-etch-access channels obtain diameters d_{ea} of 200 nm to 500 nm, which are dependent on the quality of the lithography on patterned surfaces or the quality of the side-wall spacer. In order to close these channels, at least a thickness of the capping layer t_{cap} of half a diameter is necessary. This means that thicknesses of at least 100 nm to 250 nm are required. Here, two principle methods are evaluated: PECVD and CVD deposition. Figure 4.4 shows schematic drawings of single diaphragms covered by a. PECVD and b. by CVD processes. The differences are the filling of the etch-access channels (compare (1) and (3)), the deposition inside the cavity (4), and the form of deposition at the bottom of the cavity (compare (2) vs. (5)). While the PECVD causes bumps due to the pattern of the etch-access channels with $t_{bottom} \leqslant d_{ea}/2$, the CVD process can show the result of island growth $t_{bottom} \gg d_{ea}/2$ if a material-dependent incubation time is longer than the incubation time plus required deposition time to fill the etch-access channels. A SiGe CVD process shows desired characteristics. Whereas a PECVD shows no further deposition inside the cavity, the CVD causes a homogeneous layer deposition on the backside of the diaphragm with $t_{cavity} \leqslant d_{ea}/2$.

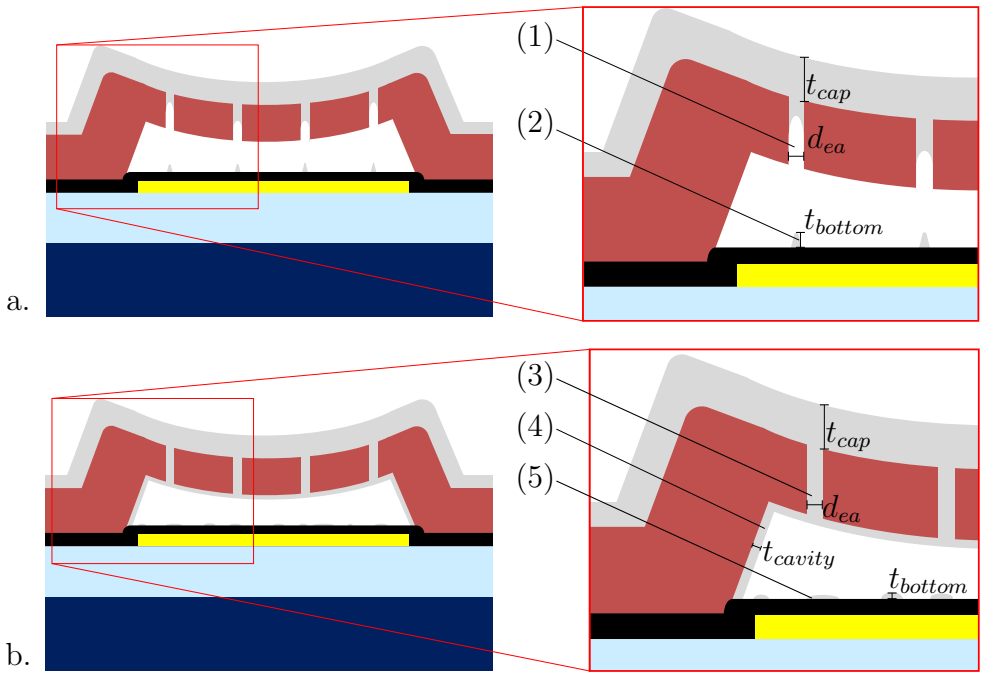


Figure 4.4: Schematic cross section of single diaphragm, which are covered via a. PECVD and b. via CVD

First, SiO_2 via ICPECVD is evaluated. An advantage of this method is the relatively little deposition inside the cavity due to an anisotropic characteristic. Unfortunately, plasma-induced heating turned out to be the major disadvantage of PECVD. A significant heat transfer limitation from the centre of the diaphragms to the substrate arises. Since the extra heat generated due to the impact of accelerated particles is not efficiently dissipated to the substrate, a locally increased material expansion occurs. This can lead to a curvature in the opposite direction of the intended deflection. A consequence is buckling, which significantly reduces the capacitive sensor signal and can even lead to destruction of the diaphragms.

Therefore, the use of a CVD process to form an undoped SiGe layer at the same substrate-temperature as the PECVD of the SiGe diaphragm at 375 °C is identified as the more appropriate method. Here, different incubation times depending on the exposed material are observed [153]. These features can be used to an advantage. The deposition of undoped CVD SiGe on a boron-doped PECVD SiGe diaphragm show the high grow rates in a range of 30 nm/min to 70 nm/min with hardly any incubation times until laminar layer growth starts. Thus, the

PECVD SiGe acts as seed layer. The reason for different incubation times for CVD SiGe deposition on materials different from SiGe, such as SiO_2 or SiC, is due to different crystal grains. This effect may be exploited in a cover deposition on the open diaphragms in order to achieve a minimal cavity filling. A further major advantage compared to a PECVD cover layer is the fact that a later reduction of t_{cap} is possible due to the complete filling of the etch-access channels. Creating a closed, pure SiGe diaphragm is expected to show advantages compared to state-of-the-art sealings, because an almost identical CTE for diaphragm and cover layer can be assumed, ideally.

(9) Sealing: Here, for example, Si_3N_4 is an approved material [37, 190, 191]. At this position of the process chain, ALD-materials can be utilised instead to achieve application-specific properties, which are mentioned before. In this case, the ALD windows must be considered regarding the temperature budget and the potential CTE mismatch compared to the diaphragm - stack materials. Further, a 100 °C ICPECVD at 0.27 Pa process pressure is available for the Si_3N_4 sealing layer. Thus, a standard surface passivation can be established. A need for additional sealing can arise due to the high Ge concentrations in the 2nd MEMS wiring level. This can lead to drawbacks regarding reliability due to the fact that Ge is more affected by humidity compared to Si. Here, oxidation can become an issue because GeH species are more unsteady than SiH species. [144, 148, 149].

(10) Bond Pad: A stack of Ti, TiN and AlSi is sputtered with thicknesses of 40 nm, 80 nm and 900 nm to form an electrode for wire-bonding purposes. This electrode stack is applied onto the PECVD SiGe, which is opened with the aid of a lithographic mask and a Cl-based RIE-process. Here, Ti acts as an adhesive layer to prevent delamination off the subjacent layer. TiN is applied as a diffusion-barrier layer to prevent metallurgical reactions as well as diffusion between the silicon and the contact metal [155, 192], which can already occur at relatively low temperatures of 250 °C. Although the risk of the so-called Al-spiking into SiGe or even deeper is classified as low, since no further temperature steps are applied in the MEMS processing, there might be risks for example due to the thermal activation during bond-processes. Further, the presence of Ge increases the solubility of Si in Al, which can lead to excessive spiking at relatively low

temperatures. These risks are successfully prevented by the chosen metal stack, as shown in Chapter 4.2.6 on Page 122.

4.1.3 Schematic Process Flow

In Figure 4.5 the process flow for the fabrication of absolute capacitive pressure sensor diaphragms is sketched and divided into 9 steps. Note that developed resist structures are not drawn, but the use of photoresists is indicated by the labels on the right side.
First, a. indicates the sputter deposition and patterning of the 1st MEMS wiring level via patterned thin film resists and RIE. In Chapter 4.2.2, TiW is evaluated as the most promising material. Then, b., shows a SiC layer with a dual function as electrical isolation and etch barrier to protect the 1st MEMS wiring level and the subjacent layers/substrate against subsequent etching processes. The deposition and patterning of the sacrificial layer for MEMS diaphragm follows to form the diaphragm (c.). Here, the 2nd photoresist patterning concerns optimised exposure settings to realise chamfered edges of the sacrificial layer. The patterning is, again, performed via RIE. As a further measure for additional chamfering and side-wall smoothing, a vHF flash can be applied followed by an immediate photoresist removal. The next step, d., shows the opening of the SiC protection layer to release the 1st MEMS wiring level. This requires a patterning via RIE with the aid of a 3rd photolithographic mask. The PECVD of SiGe as 2nd MEMS wiring level establishes the major diaphragm layer and is connected to the 1st MEMS wiring level. No extra via filling is required, because the SiC protection layer is relatively thin ($\approx$ 100 nm) and the contact areas are relatively large (100 µm at bondpads, 1 µm in vias) due to the mask design. In e., the patterning of etch-access channels via hardmask processes is applied. Here, two hardmasks are added in order to use a side-wall spacing effect. This sub-process is described in more detail in Chapter 4.2.3. By this purpose, etch-access-channel diameters smaller than the lithographically achievable resolution are realised. Here, the 1st hardmask is patterned by the use of the 4th photolithographic mask. Finally, the SiGe diaphragm is patterned via the applied hardmasks in order to enable an etch-access to the buried sacrificial layer. The next step, f., includes the hardmask removal and sacrificial layer release etch simultaneously in a single vHF etch process.

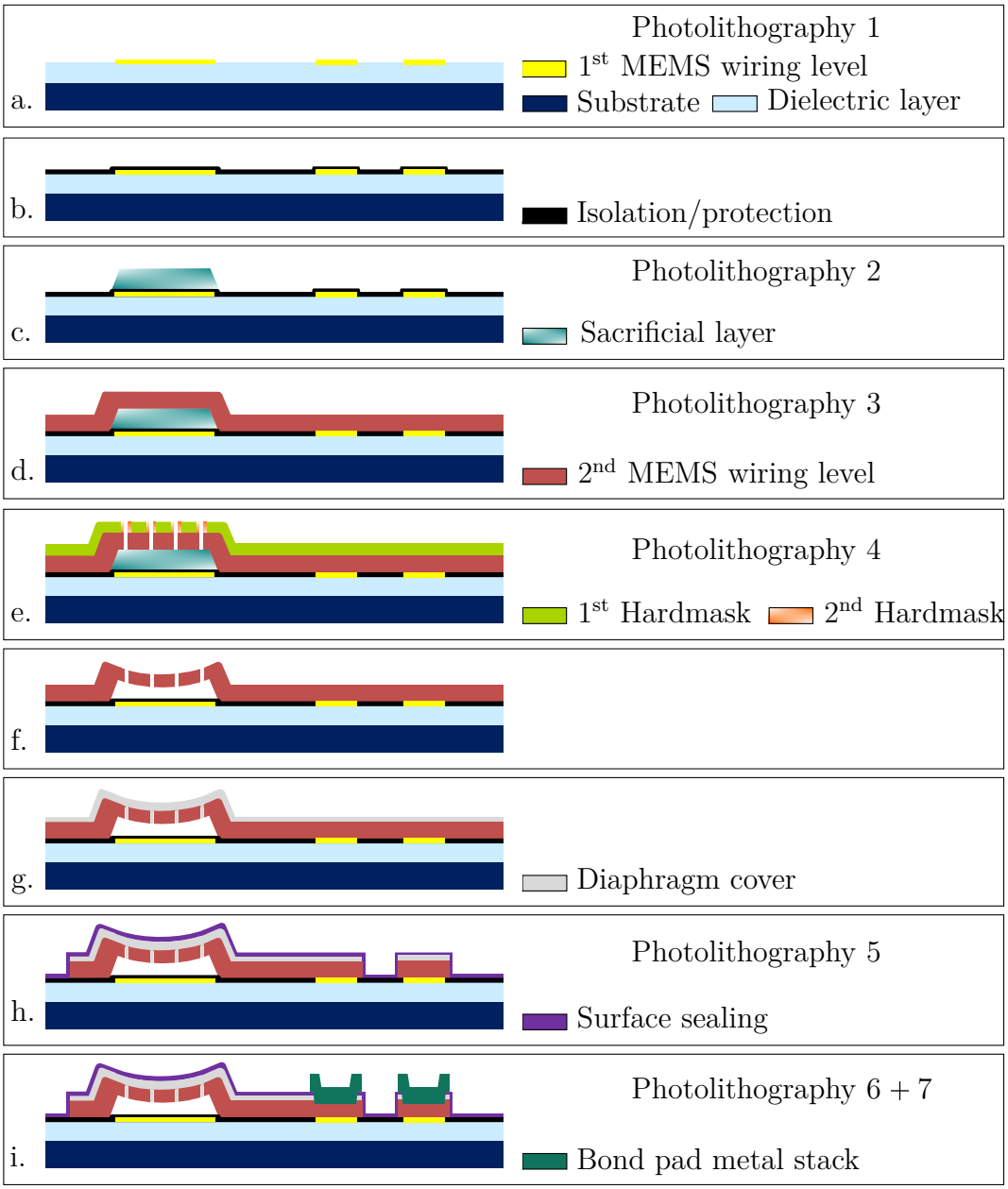


Figure 4.5: Schematic fabrication flow: a. 1st MEMS wiring level, b. isolation/protection of 1st MEMS wiring level, c. sacrificial layer to define the cavity, d. 2nd MEMS wiring level and diaphragm, e. patterning of etch-access channels through side-wall spacer processes (hard-masks), f. in-situ removal of hardmasks and sacrificial layer release, g. deposition of cover layer, h. patterning of 2nd MEMS wiring level, then surface sealing, i. bond pad metal stack.

The following step, which is sketched in g., is to close the etch-access channels of open diaphragms. Otherwise, stiction is inevitable because several subsequent processes require the use of water or fluid media. Amongst others, photoresist

spin coating, resist development, resist stripping or cleaning after resist stripping are processes which must not be applied to the open diaphragms designed. After the diaphragms are covered, further patterning processes are applicable again. Thus, in h., the patterning of both the 2nd MEMS wiring level and the cover layer is applied. For this purpose a 5th photolithographic mask is required. This step is completed with the deposition of surface sealing with Si_3N_4. In order to finalise the stand-alone pressure sensor elements without a subjacent CMOS substrate, an opening of both the sealing and the cover layers to release the 2nd MEMS wiring level is required. For this purpose, a 6th photolithographic mask layer is applied. Then, deposition and patterning of an bond pad metal stack comprising Ti, TiN and AlSi is chosen due to proven suitability for wire-bonding. The patterning of the bond pad metal stack requires a last 7th photolithographic mask layer (i.).

4.2 Process Developments and Challenges

For development of a post-CMOS technology to fabricate diaphragm-based MEMS pressure sensors in surface micromachining, some challenges have been previously identified and described. Some of the most important developments of individual layers or process sequences are described as follows: an appropriate material for the 1st MEMS wiring level. Further, the development of a SiC protection for the CMOS substrate and the 1st MEMS wiring level from aggressive media is described. Another major focus is to utilise vapour-phase etching as the method to release the sacrificial layer. Here, a mixture of vHF and water vapour is utilised. This means, contrary to established processes utilising vHF with vapour ethanol, stiction becomes a risk, thus the prevention of stiction is another major focus. Additionally, vapour-phase etching requires an appropriate design of etch-access channels of pressure sensitive diaphragms. In this thesis, a process sequence is developed to enable etch-access channel diameters to be much smaller than the available lithographic resolution. The fabrication of diaphragms, which utilise capacitive sensing principle due to the improved suitability for highly sensitive applications has to fulfil the temperature limitations in post-CMOS processing. Therefore, SiGe is utilised as the material of choice. Here, developments for the different stages of patterning the SiGe are evaluated. Further, the diaphragms

require completely closed surfaces for the exposure in environments that differ from ideal gases. This requires a cavity cover layer. In this context, PECVD and CVD cover layer processes are evaluated. At the aspired level of development an assistant electrode becomes necessary for electrical characterisation of the sensor elements. The electrical characteristics of this assistant electrode comprising SiGe, Ti, TiN, and AlSi are evaluated.

4.2.1 Isolation and Protection Layer

In a MEMS releasing process, the sacrificial layer must have a high selectivity towards the layer underneath to avoid the formation of potential by-products. Therefore, a protection layer must show characteristics of an etching barrier. Some frequently used insulating materials, for example nitrides, have been proven inappropriate, as discussed in Chapter 2.2.2. Thus, a material is desired with some primary characteristics:

- Outstanding resistivity against the applied vaporous etch media.
- Available at appropriate temperatures, i.e. lower than 400 °C.
- Appropriate von-Mises stress to ensure an acceptable wafer bow.
- Insulating characteristics to prevent shorts in the sensor wirings, especially in the case of capacitive sensors.

Silicon carbide (SiC) seems to be a suitable material due to its advancements in thermal stability, hardness, wear resistance and chemical stability [124, 125]. SiC also shows potential as dielectric isolation material because of the wide band gap around 3 eV [124, 126].

SiC Design of Experiments

SiC-layers are developed with PECVD utilising Inductive Coupled Plasma (ICP) in a *Plasmalab System*100, which is introduced in Chapter 2.2.3. Due to the limited temperature budget in post-CMOS processing, the deposition temperature is set at 300 °C. Further, the power of ICP, is set to 2000 W. The parameters are summarised in Table 4.1. The precursor gas SiH_4 is introduced as Si source and CH_4 is used as C source, while Ar or H_2 activate and discharge the plasma.

The deposition process pressure is suggested to be kept under 2.7 Pa for security reasons for the protection of the etching chamber which is made of Al.

Table 4.1: Basic SiC ICPECVD deposition parameters.

Related gases	Pressure in Pa	ICP power in W	Temperature in °C
H_2, Ar, SiH_4, CH_4	$\leqslant 2.7$	2000	300

Characterisation The developed SiC layers are characterised by the use of energy-dispersive X-ray spectroscopy (EDX), X-ray diffraction (XRD), scanning electron microscopy (SEM), and Raman spectroscopy. The cross-sections of the samples are checked by SEM *S*-4700 from *Hitachi* with a working voltage of 7 kV. The surface topography is inspected and measured by *Leica DCM* 3*D system*, which integrates confocal and interferometer technology and can handle 3D optical surface metrology scanning. XRD is used to investigate the crystal structures in deposited layers. XRD is performed in *D*8 *Advanced X-ray Spectrometer* from *Bruker* with a Cu X-ray tube with a wavelength of 1.5418 Å. Raman spectroscopy, which can distinguish different crystal polytypes, is performed in the tool *inVia confocal Raman spectrometer* from *RENISHAW* with a green laser of 532 nm wavelength. The power of the laser is fixed at 1 % and the exposure time for analysis is 10 s. Further, to detect deviations ("defects") from a "clean" reference wafer surface after deposition and etching, the multifunctional equipment *Linewidth and Overlay Measurement System MT*3000 from *MueTec* is used. Layer thicknesses of deposited materials are measured by the ellipsometer *UV*1280 from *KLA-Tencor*. The Dual Beam Spectrometer (DBS) mode is used and every thickness is obtained by a setting of 49 point measurements.

Variation of deposition parameters From literature it is known that amongst others, appropriate precursor gas flow rate ratios, applied process pressures and PECVD power are proven to promote the crystallisation of SiC layer regarding the layer properties, deposition rate, deposition uniformity, stress and Si to C composition ratio [133]. The combined usage of both a magnetic ICP and a capacitive RF source has ensured a successful deposition of SiC layers on Si, amorphous Si and SiO_2 substrates with good adhesion performance. Increasing

the power of the RF source and the deposition pressure has been proven to be capable to elevate the deposition rate linearly, with, at the same time, increasing bias voltage. An appropriate optimum is found by applying 100 W RF power, whereas the resulting bias voltage does not exceed 300 V.
Further, the deposition pressure is known to elevate the deposition rate linearly according to its correlation to the number of molecules. Consequently, to obtain a high deposition rate, the highest available pressure (2.7 Pa) is utilised in the following experiments. In an applied pressure range from 0.5 Pa to 2.7 Pa, there was no significant difference detected in layer uniformity, which varied in a range of 6 % to 10 %.
The precursor gases (CH_4 and SiH_4) ratio and carrier gas (Ar or H_2) of the deposition process are investigated experimentally. Here, a dense SiC protection layer is intended that obtains high selectivity against the applied etchant. The effectiveness of the desired protection function is evaluated with the aid of defect scan results. This method counts the deviations from a preselected reference area, which is assumed to be free from any visible defects. It was applied before and after an exposure of the samples to vapour HF etchant. The thicknesses of the investigated SiC layers are about 200 nm when Ar is used as carrier gas and about 70 nm for H_2. With respect to SiC layer deposition rates, about 66 nm thick layers were obtained after 20 min deposition, thus the calculated deposition rate is about 3.3 nm/ min. The thickness is around 1/3 to those deposited in Ar with the same deposition parameters.
In the experiments regarding both carrier gases, CH_4 over SiH_4 ratios of 2, 1 and 0.5 were implemented, respectively. Moreover, for experiments with H_2 as carrier gas, a dilution ratio (defined as $H_2/(CH_4 + SiH_4)$) of 2 was chosen to obtain the best crystallisation result [193]. In addition, a variation of the applied etching pressure in vapour HF exposure was implemented to detect any impacts on the SiC layer by this process step. The observed results are shown in Figure 4.6 and listed in Table 4.2. Here, the numbers of defects allocated on a 200 mm wafer with a size of 10 µm and greater are presented, measured after applying vapour HF exposure. In order to show a reference value, wafer 1 in the first line of Table 4.2 represents the number of defects before applying any etchant exposure. However, compared with the deposition process utilizing Ar, the SiC deposition with H_2 obtains a lower deposition rate, reduced by about a factor of 3.

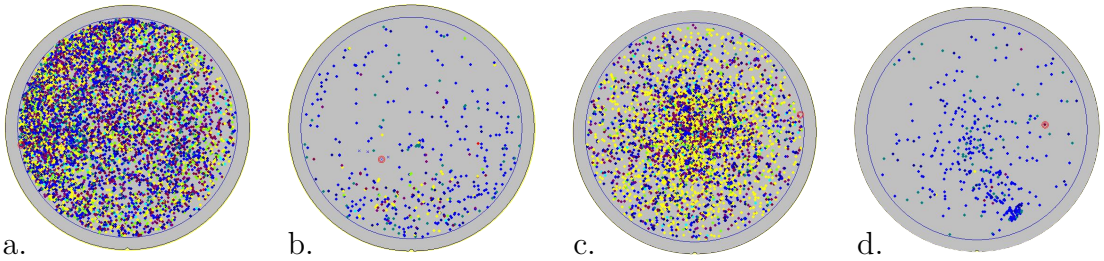


Figure 4.6: The defect distributions on 200 mm wafers after vapour HF etching under variation of gas flow ratios and etching parameters:
a. Ar:CH_4:SiH_4 = 3 : 2 : 1, etching 26.7 hPa for 15 min
b. Ar:CH_4:SiH_4 = 3 : 0.5 : 1, etching 6.7 hPa for 25 min
c. H_2:CH_4:SiH_4 = 6 : 2 : 1, etching 26.7 hPa for 15 min
d. H_2:CH_4:SiH_4 = 3 : 0.5 : 1, etching 6.7 hPa for 25 min

Table 4.2: Deposition and etching process parameter variation, as well as defect scan results on samples with layer stacks comprising a Si substrate with 200 nm SiO_2 and SiC layers. In SiC deposition with either H_2 or Ar used as carrier gas, the gas flow ratios are varied. Additionally, in vapour HF etching a variation of the process pressure is applied.

	Deposition	Vapour HF exposure		Result
Wafer #	Gas flow ratios H_2/Ar:CH_4:SiH_4	Pressure in hPa	Time in min	# of defects $\geqslant 10\,\mu m$
1	3(Ar) : 2 : 1	not applied	not applied	51
1	3(Ar) : 2 : 1	26.7	15	7400
2	3(Ar) : 1 : 1	26.7	15	237
3	3(Ar) : 0.5 : 1	6.7	25	131
4	6(H_2) : 2 : 1	26.7	15	4770
5	6(H_2) : 2 : 1	13.3	15	3824
6	4(H_2) : 1 : 1	13.3	15	809
7	3(H_2) : 0.5 : 1	6.7	25	29

First, it can be observed that an increasing dilution by the carrier gas decreases the number of defects due to a reduction of CH_4. Second, the defect scanning results show that applying lower etching pressure reduces the number of defects, but less effectively than the benefits brought by the decrement of the precursor gas ratio. Third, a dilution ratio of 2 was found to obtain the best crystallisation result.

Finally, SiC layers employing H_2 show an outstanding result after etching, comparing the results obtained by gas flow rate ratios of 3 : 0.5 : 1 in Ar (#3) and H_2 (#7), respectively. This improvement proved that H_2 functions as a crystallisation agent to facilitate forming a dense SiC layer comprised of more crystalline SiC morphology. This result confirmed that the crystallisation is promoted with the presence of H_2 instead of Ar [193].
Furthermore, differences of less than $\pm$ 1 nm in thickness between pre and post vapour HF exposure are detected. Thus, no reduction of the thickness of the SiC protection layer is assumed. This indicates that this SiC layer is not etched and it kept stable in the vapour HF etching.

Characteristics of SiC etching barriers

In Table 4.3 the main parameters of the wafers are listed, which were characterised by XRD, EDX and Raman spectroscopy.

Table 4.3: Layer samples for XRD (# 8, 9) and Raman (# 3, 7) spectroscopy.

Wafer #	Carrier gas	Gas flow ratios Ar/H_2:CH_4:SiH_4	SiC thickness in nm
8	H_2	3 : 0.5 : 1	2000
9	Ar	3 : 2 : 1	4400
3	Ar	3 : 0.5 : 1	200
7	H_2	3 : 0.5 : 1	70

XRD For the XRD analysis, both gracing incidence (glancing angle, detector scanning) mode for relatively thin layers (up to several hundred nanometres) and $\theta - 2\theta$ mode for relatively thick layers (up to several millimetres) were used. In the gracing incidence mode, the sample is fixed at a small incidence angle and the detector can rotate. In the $\theta - 2\theta$ mode, the sample can rotate at a constant angular velocity and the detector rotates at double angular velocity. The scattering angle (2θ) is twice the incidence angle (θ). Because the penetration depth of incidence X-ray is related to the incidence angle, the difference in incidence angle of these two modes leads to the different available measurement ranges.

The results of the gracing incidence mode showed primarily very weak peaks located at about 29°, which are attributed to the noise introduced by the basic Si substrate. In Figure 4.7 the results of a $\theta - 2\theta$ measurement are shown. Peaks can be clearly observed at about 33° in the spectra of both samples. The peaks around 33° are attributed to 4*H*-SiC. None of the wafers showed 3C-SiC characteristics.

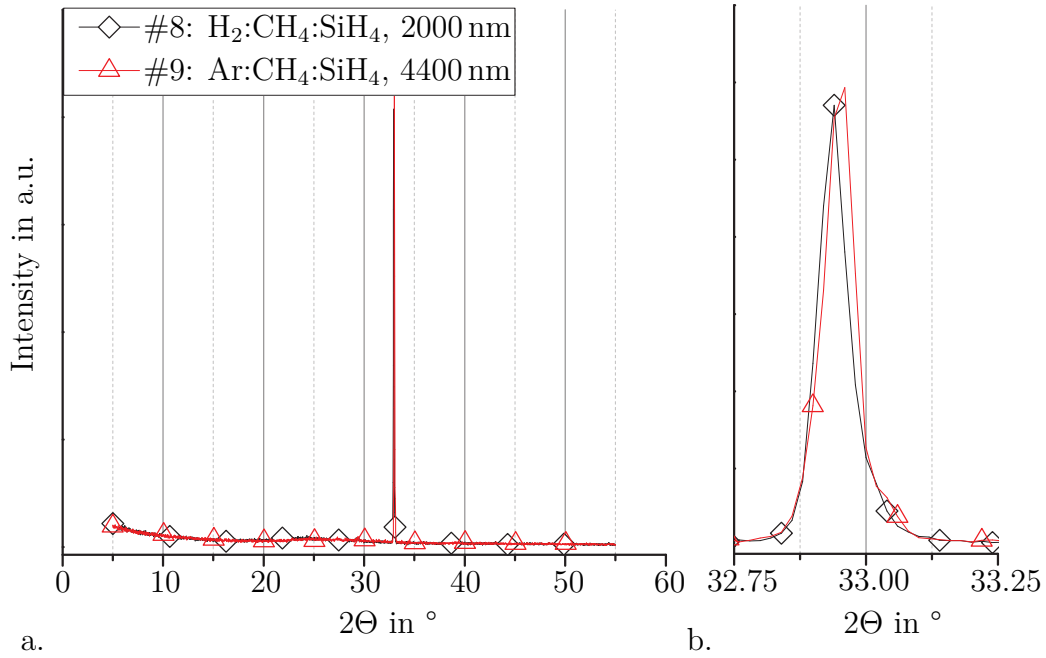


Figure 4.7: XRD analysis spectra of #8 and #9 obtained via $\theta - 2\theta$ mode, a. spectrum range 20° to 80°, b. magnification for peak at about 33°.

EDX To support the results achieved by XRD, an EDX analysis is applied to further investigate the chemical composition. The results are displayed in atom%. For wafer #8, 15 % C with 85 % Si and for wafer #9, 20 % C with 80 % Si are obtained.

Raman spectroscopy Raman spectroscopy has the capability of distinguishing different polytypes in detail. This method was applied to investigate two sample layers, whose only different deposition parameter is the carrier gas (Ar and H_2), while the total gas flow rates are hold constant and the ratio of Ar or H_2:CH_4:SiH_4 of 3 : 0.5 : 1 is applied. The SiC layers are deposited on SiO_2 layers to have a contrast in the Raman spectra. The variation of the carrier gas

resulted in different thicknesses of 200 nm for Ar and 70 nm for H_2, respectively. The corresponding spectra are shown in Figure 4.8.

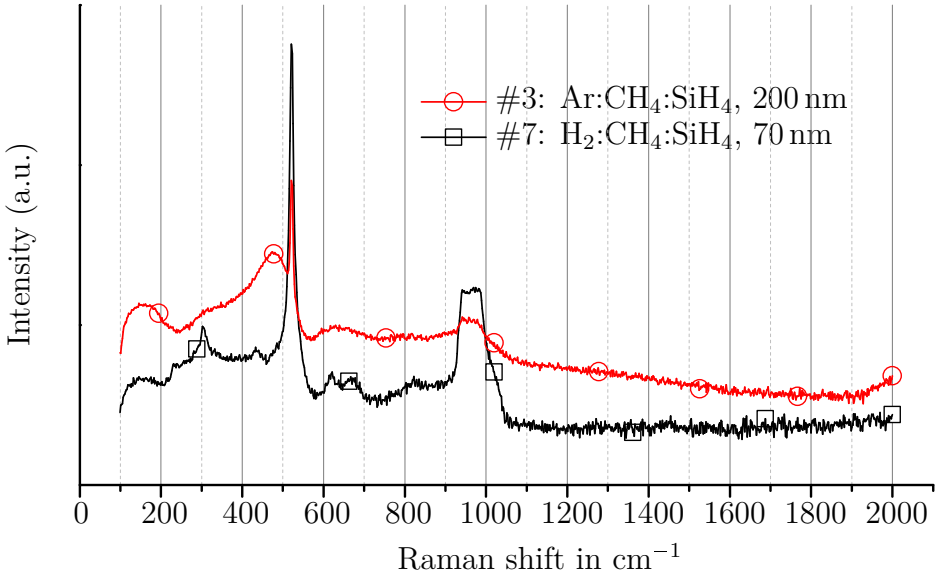


Figure 4.8: Raman analysis spectra. These plotted spectra are very typical patterns and each analysed sample has either similar pattern.

The peak at 500 cm^{-1} is the major peak of crystalline Si and that at around 300 cm^{-1} is related to Si as well [140, 194]. The spectrum pattern of wafer #4 from 100 cm^{-1} to 500 cm^{-1} is the typical pattern of SiO_2. Rises of the intensities at about 950 cm^{-1} were observed for both samples. The wide peaks around 950 cm^{-1} might correspond to an overlapping of Si peak and SiC peaks of diverse polytypes, including 3C-SiC, 4H-SiC and 6H-SiC. The swelling and shoulders between 600 cm^{-1} to 900 cm^{-1} might be attributed to the peaks of 4H-SiC and 6H-SiC. The major peak of SiC at around 800 cm^{-1} is not observed in the spectra. This is maybe due to the weak performance in this range of Raman spectroscopy or due to the limitation of the applied laser. The trend of rising spectrum over 1800 cm^{-1} could be due to the amorphous SiC. As a conclusion, the peak of SiO_2 might be the noise introduced be the substrate SiO_2 layer underneath due to the relatively thin sample layer and the deposited layer could be synthesised with Si, α-SiC (4H, 6H, 8H) and amorphous SiC.

Summary of material characterisation The individual characterisation results are inconclusive. For example, an increase of the gas flow ratio of CH_4/SiH_4 lowers the intensities of the diffraction peaks of (111), (220), and (311) crystal planes gradually [195], at the same time the carbon content increases. However, the higher the C concentration, the worse the resolution of crystalline diffraction peaks to be observed, implying that the layer characteristics become more amorphous. In grazing incidence XRD, the elevated signal on the range of 5° to 15° is related to amorphous SiC [195]. In $\theta - 2\theta$ mode XRD, the observed peaks at about 33° are attributed to the diffraction peak of (100) crystal plane of $4H$-SiC [196, 197]. Regarding the EDX measurement results, significant C concentrations are detected, even inhibition by the Si content from the substrate, for example by a still too low layer thickness, is possible. The detected concentrations are not stoichiometric, thus an amorphous characteristic SiC is probable. Moreover, the trend of the results is meaningful, as increasing the CH_4 over SiH_4 ratio elevated the C content. Then, in Raman spectroscopy, rising intensities at about $950\,cm^{-1}$ were observed for both samples. These are due to SiC characteristics of diverse polytypes, most probably $4H$-SiC and $6H$-SiC. Further, an observed trend of a rising spectrum over $1800\,cm^{-1}$ points to the amorphous SiC characteristic. In summary, all the results showed that the deposited layers are comprised of $4H$-SiC, amorphous SiC and Si.

SiC exposure to vapour HF The developed SiC layer synthesised with the optimised parameter setting is deposited on a patterned SiO_2 sacrificial layer. For proof of principle, free-standing SiC-structures with a layer thickness of about 180 nm and of 80 µm in diameter are successfully released in a vapour HF etch process with the aid of lithographically perforated etch-access channels with 630 nm in diameter. A cross section of an edge of a single SiC-structure is shown in Figure 4.9 a., the holes for the access of the etchant are shown in Figure 4.9 b.. The cavity height of 500 nm was given by a patterned SiO_2 layer. This result shows that the deposited SiC preserves the chemical inertness in the vapour HF etching process with the presence of the SiO_2 etching reaction. Further, as shown in Figure 4.9 a., the vertical part at the edge of the test structure shows a thickness of about 40 nm, which is smaller than 180 nm of the lateral part of the SiC layer. This means a very low side wall step coverage with a conformity

of 0.22. Thus, the deposition of SiC is anisotropic. However, even these thin vertical structures remained stable and supported the lateral, free-standing part of the layer. No cracks were observed.

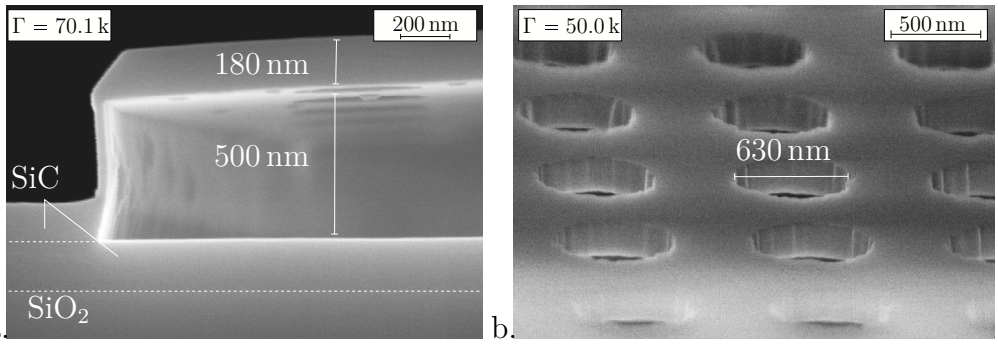


Figure 4.9: Free-standing, circular-shaped SiC structures with a diameter of 80 µm, a cavity height of 500 nm and etching access channels with a diameter of about 630 nm after vapour HF etching of TEOS SiO_2 sacrificial layer. a. SEM cross section of the edge of the structure, b. SEM aerial perspective of etch-access channels.

In Figure 4.10 the topography scanning result of one 80 µm structure via $3D$ interferometer is shown. The pitch of every two adjacent structures is 20 µm. Figure 4.10 a. indicates that the surface of this structure before the vapour HF etching is flat and Figure 4.10 b. demonstrates that a bow shape deformation is formed after the vapour HF etching.

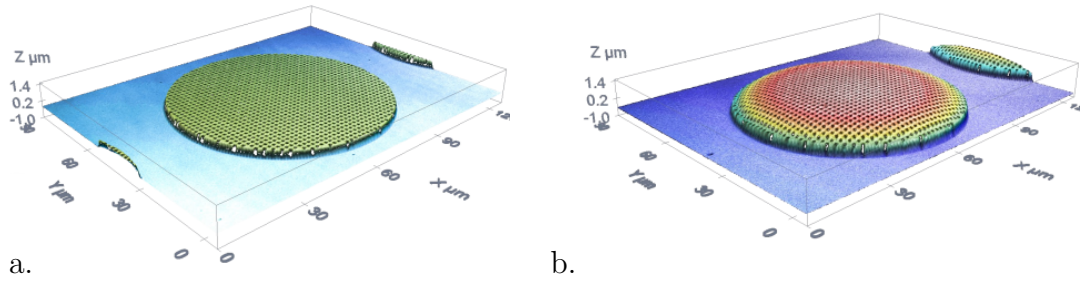


Figure 4.10: 3D interferometer topography of a single structure a. before and b. after release etch.

Figure 4.10 demonstrates a bow shape deformation of the SiC structure after the vapour HF release etching. The height of the structure centre after etching is around 1.7 µm. In conclusion, considering that the height of the cavity had been 500 nm and the structural SiC layer obtained a thickness of about 180 nm, a significant deformation of about 1 µm is observed. The non-uniformity was less

than 4 % among 5 structures at evenly distributed positions on the whole wafer. This indicates that this deformation was due to the intrinsic mechanical stress within the SiC structural layer. This topography result does not show stiction and further, a thin vertical wall can effectively support the entire structural layer. Thus it is proven that SiC is highly appropriate to act as protection layer in vapour-phase etching for sacrificial layer release processes.

SiC exposure to vapour XeF_2 Experiments are performed to demonstrate the robustness of a SiC protection layer against XeF_2. Test structures have been fabricated analogous to the previous ones with the exception of the sacrificial layer. Here, aSi is deposited instead of SiO_2. The results show a destruction within the areas of patterned sacrificial layer but not in the adjacent area around the patterned sacrificial layer [185]. It is assumed that the perforated test structures are blown away as a result of a highly exothermic reaction between XeF_2 and Si [198]. Even though the SiC seems to show protection characteristics against XeF_2, this sacrificial layer technology is no longer pursued because of the disruptive effect on the test structures.

4.2.2 1st MEMS wiring level

A first material selection is based on the results of Chapter 2.2.2. Investigated materials are TiN, TiW, Cu, or AlSi, which are sputtered by the use of an *Endura PVD* 200 mm by *AMAT*. Further, TiN layers via an ALD-CVD process at 350 °C with different thicknesses are evaluated. Unless specified differently, the following results describe sputtered metals on 200 nm USG layers on a bare reclaimed Si substrate. Regarding the 1st MEMS wiring level, some primary characteristics required are summarised:

- Matching of individual CTE
- Etch resistivity
- Electrical conductance
- Residual stress
- Adhesion of SiC
- Connectivity to boron-doped SiGe (PECVD)

For example, the CTE mismatch is evaluated based on literature values [199]. The CTE matches regarding adjacent layers of SiC, SiO_2, Si_3N_4 and SiGe are listed in Table 4.4. The adjacent layers are those, which have direct contact to the 1st MEMS wiring level. These are, primarily, SiC, which is deposited at 300 °C as a protection layer on patterned metal, and SiO_2 or Si_3N_4 as subjacent materials on CMOS substrates. Finally, SiGe as a 2nd MEMS wiring level is considered since contact areas (vias) have to be established. The CTE matches of the investigated metals to each adjacent layer are expressed in percent. Here, 100 % would represent a perfect match. In the last row of Table 4.4 the average match is calculated as an arithmetic mean. TiW shows the highest match (72.2 %) followed by Cu, TiN and AlSi with all less than 20 % match.

Table 4.4: CTE matches of evaluated metals (TiN, TiW, Cu and AlSi) regarding adjacent layers SiC, SiO_2, Si_3N_4 and SiGe.

Material		TiN	TiW	Cu	AlSi
	CTE in 10^{-6}/K	≈22	≈4.5	≈16.4	≈22
SiC	≈4.3	19.6 %	95.6 %	26.2 %	19.6 %
SiO_2	≈0.6	2.7 %	13.3 %	3.7 %	2.7 %
SiGe	≈5.4	26.4 %	128.9 %	35.4 %	26.4 %
Si_3N_4	≈2.3	10.5 %	51.1 %	14.0 %	10.5 %
Average CTE match		14.8 %	72.2 %	19.8 %	14.8 %

Etch Resistivity of Metals against Vapour-Phase Etching

While the previously discussed characteristics are known from literature, the effects of vapour phase etchant exposure of the named metals and the adhesion of SiC on those are evaluated. The etch resistivity against vapour HF utilised as etch media for the sacrificial layer is not a primary issue, because the 1st MEMS-wiring-level layer is protected by an etch barrier layer. Nevertheless, the etch resistivity is investigated for two reasons: First, to identify the risk of potential failures or etching reactions in case of local, unexpected etch accesses via the protection layer. Second, the higher the reactivity of the 1st MEMS circuit layer, the thicker the protection layer should be designed in order to minimise the risks due to inhomogeneities, pinholes or random, locally contained defects in the

protection layer. Here, it is important to keep in mind that no H_2O-containing processes should be applied after exposure to vapour HF in order to avoid any risks regarding stiction effects. This means that cleaning steps are not an option to remove any etching products of HF against the 1st MEMS-circuit-level material.

In Figure 4.11 the effects of 10 min vapour HF/H_2O exposures with a constant process pressure of 13.3 hPa at 40 °C are shown by microscope inspections. Even though only planar layers are investigated in the present chapter, 13.3 hPa is chosen as it is the threshold region of a maximum process pressure at which a stiction-free release of the free-standing structures designed in this thesis is possible.

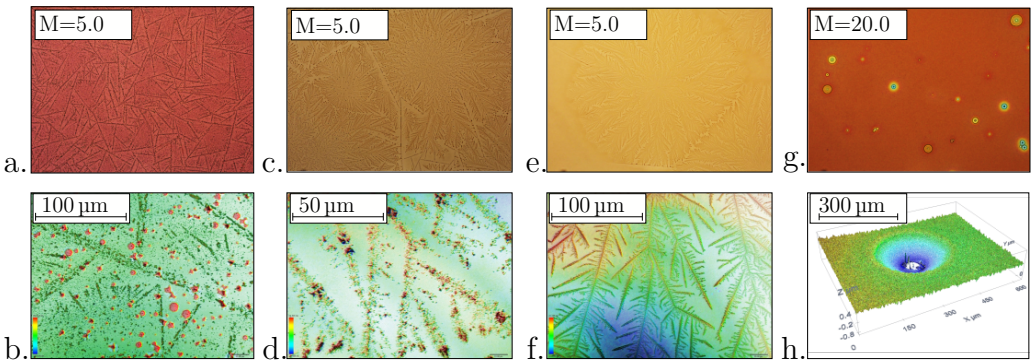


Figure 4.11: Microscope inspection of a. and b. 50 nm TiN via sputter deposition, c. and d. 20nm TiN via ALD-CVD, e. and f. 40nm TiN via ALD-CVD, g. and h. 300 nm Cu.

The different TiN layers and the Cu layer are visibly attacked after the vapour phase etchant exposure. The sputter-deposited TiN layer in Figure 4.11 a. and b. shows two major error patterns, which are crystalline forms at the layer surface and circular-shaped, red-coloured irregularities (see b.). There, under-etching effects are visible and indicate pinholes, which enable etch-access to the underlying SiO_2. However, the ALD-TiN layers in Figure 4.11 c. to f. show primary crystalline forms at the surface, but the appearance of pinholes is significantly minimised with increasing layer thickness (compare d. and f with ≈20 nm and ≈40 nm, respectively). These crystalline forms are not completely understood. Perhaps these are a result of oxidation at crystal boundaries, where Ti has a lower content of N. In [122] it is reported by using Auger depth profiles that Ti is converted to Ti-oxide during wet HF/H_2O etching processes. Converted

to Ti-oxide, the etch resistivity and thus, the sheet resistance are significantly increased. This further supports the observation that hardly any change in layer thickness is detected.
In 4.11 g. to h., the surface of Cu after vapour HF exposure is shown. Here, many defects in the magnitude of at least 10 µm to 100 µm are detected. In h., a spalling released a hole in Cu with a diameter of about 250 µm to 300 µm and a depth of at least 500 nm. This indicates that pinholes in Cu granted etch accesses to the USG and the formation of by-products could have caused spallings.
The surfaces of TiW and AlSi remain visually unaffected and are therefore not shown. In Table 4.5 the changes of the individual sheet resistances $R_{\square}$ detected at 49 points per wafer with a *Resmap 168* by *CDE* based on the four-point method are listed. The results support the visual inspection before. The sheet resistances of TiW and AlSi are hardly affected and show a variation of 1.9 % and −5.4 %, respectively. The absolute reduction in sheet resistivity of AlSi is negligibly small. However, sputtered TiN and Cu show significant changes of 16 % and 33 %, respectively. All the results support the microscope inspections.

Table 4.5: Evaluation of sheet resistances due to vapour HF exposure

Metal	ρ in $\Omega\,\mathrm{mm}^2/\mathrm{m}$	$R_{\square}$ pre vHF exposure in $\Omega/\square$	$R_{\square}$ post vHF exposure in $\Omega/\square$	$\Delta R_{\square}$ in %
50 nm TiN	2.8	56.8 ± 3.4 %	65.9 ± 7.4 %	16.0
20 nm ALD-TiN	2.2	107.6 ± 8.6 %	119.7 ± 17.5 %	11.2
40 nm ALD-TiN	2.8	69.1 ± 8.2 %	72.8 ± 8.5 %	5.4
100 nm TiW	0.8	7.8 ± 1.5 %	8.0 ± 2.1 %	1.9
300 nm Cu	0.03	0.08 ± 2.1 %	0.11 ± 18.3 %	33.0
400 nm AlSi	0.04	0.092 ± 1.6 %	0.087 ± 1.4 %	−5.4

Effects of SiC Deposition on Evaluated Metals

Since the 1st MEMS wiring layer partly acts as 1st capacitor electrode in a capacitive pressure sensor, an insulation is necessary to avoid short circuits while the diaphragms are highly deflected under applied pressure. As evaluated, TiN or Cu layers need further protection from vapour HF because of the shown etch reactivity. Because SiC is developed as material to fulfil both isolation and protection

function, the effects of SiC depositions on the individual metals are evaluated. The deposition of about 150 nm to 200 nm SiC via ICPECVD showed conformal layers on TiW, TiN (sputter-deposited and ALD) and AlSi. On the contrary, the deposition on 300 nm sputter-deposited Cu showed large-scaled delamination, cracks and spalling effects. This indicates most probably the presence of inhibition effects while applying the SiC process on Cu. The large CTE mismatch is assumed less likely to be responsible, since the mismatch of AlSi to SiC is even larger (compare Table 4.4). In Figure 4.12 the results of scotch-tape tests on conformal SiC layers applied on TiW and TiN are shown for example. The layers have been manually prepared with a cross by the use of a micro-diamond-scriber tool in order to create weaknesses in the tested layers. Delamination or other undesired effects are not observed on 4 equally distributed points on the tested wafer areas.

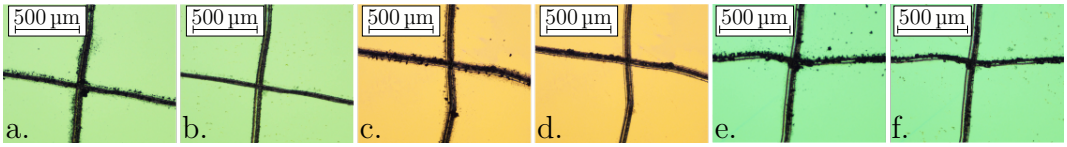


Figure 4.12: Results of scotch-tape test on 50 nm sputter-deposited TiW (a. pre, b. post), 50 nm sputter-deposited TiN (c. pre, d. post) and 40 nm ALD TiN (e. pre, f. post)

Summary 1st MEMS wiring level

In Table 4.6 the evaluated results are summarised in an evaluation matrix regarding the specified requirements. Sputter-deposited TiW shows the highest degree of fulfilment regarding the requirements. Especially the good average CTE match, an outstanding resistivity against vapour-phase etching in HF/H_2O mixtures and the compatibility to SiC (deposition process and layer adhesion) make TiW the most promising material as 1st MEMS wiring level amongst the evaluated metals. Further, TiN can be used as second choice, since the disadvantage in etch resistivity is compensated by the protection layer, to which a sufficient adhesion is detected despite the large mismatch in the thermal expansions. The electrical quality of the contacts at the 1st and 2nd MEMS wiring level junctions is further evaluated in Chapter 4.2.6.

Table 4.6: Evaluation matrix of different 1st MEMS-circuit-level materials.
++ = very good; + = good; 0 = medium; − = moderate; −− = bad.

	TiN	ALD-TiN	TiW	Cu	AlSi
Average CTE match	−−	−−	+	−−	−−
Vapour HF resistivity	−	0	++	−−	++
Conductivity (ρ)	0	0	+	++	++
Minimal layer thickness	+	++	++	−	−
Compatibility to SiC	++	++	+	–	−−
Contribution to thermal budget	++	−	++	+	+

4.2.3 PECVD SiGe as 2nd MEMS wiring level

SiGe is the material of choice as 2nd MEMS wiring level and diaphragm. This thesis refers to the developments of PECVD SiGe at Fraunhofer IMS [146]. In this chapter, the deposition processes of SiGe are evaluated in the context of the newly developed process chain. Amongst others, the compatibility regarding the adjacent materials and applied processes is evaluated. Further, as described by the process flow in Figure 4.5, different stages of SiGe patterning are required:

1. etch-access channels in order to remove the sacrificial layer in step e.

2. release of conductive lines and separation of diaphragms in step h.

Deposition of SiGe

A Precision 5000 cold wall CVD-system by AMAT is used for the depositions SiGe are performed with. The RF-frequency for the PECVD is 13.56 MHz. The applied process pressure in the deposition chamber is 2.67 hPa. Pure monosilane (SiH_4) and pure monogermane (GeH_4) are used respectively as the silicon and the germanium source. For the in-situ boron-doping, 5 % diborane (B_2H_6) in Ar is used. These process gases are diluted with argon during deposition. The ratio of the gas flow rates for the gases GeH_4, SiH_4, Ar and B_2H_6 is 208 : 150 : 2365 : 5 for the deposition of the SiGe layers. Here, a **N**ormalised **T**otal **G**as **F**low (NTGF) is introduced and refers to a gasflow of 1364 sccm. Further, R_{GeH_4} is defined as the ratio of the flowrate of GeH_4 over the sum of the GeH_4 and SiH_4 flowrates. Based on the results of a previously completed research at Fraunhofer IMS [42,

146], three different promising parameter setting are evaluated for the deposition on fully coated, unpatterned SiO_2 and SiC substrates, respectively. As presented before in Chapter 4.1.3 and in Figure 4.5 d., the deposition of SiGe as 2nd MEMS wiring level are applied to a substrate, which is primarily covered by the SiC protection layer with a minimal area opened to the 1st MEMS wiring level. Additionally, the patterned sacrificial layer partly covers the SiC. Thus, three different surfaces are exposed to SiGe. The combination of SiGe with the 1st MEMS wiring level is primarily important for the formation of an electric contact and therefore evaluated separately in Chapter 4.2.6 in combination with the bond pad metal stacks placed on top. However, SiO_2 and SiC are very important regarding the layer growth characteristics and, thus, influence the intrinsic layer stress. As outlined in Chapter 2.1.3 with Equation 2.19, it is absolutely essential to establish a minimal tensile built-in stress in the diaphragm layer.

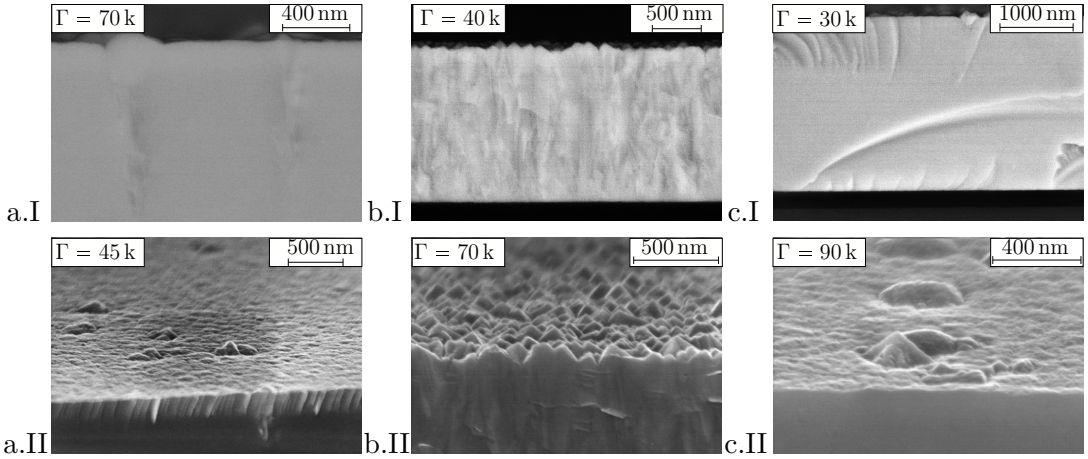


Figure 4.13: SEM cross sections and aerial views of three parameter settings for the PECVD of microcrystalline SiGe developed in [42,146] (all PECVD parameters listed in Table 4.7): a. SiGe - I (NTGF= 1.5, R_{GeH_4} =58 %, 125 W power) is primarily amorphous with µcrystals, b. SiGe - II (NTGF= 0.5, R_{GeH_4} =75 %, 66 W power) is polycrystalline and c. SiGe - III (NTGF= 1.9, R_{GeH_4} =58 %, 125 W power) is amorphous.

Figure 4.13 SEM cross sections and aerial views of three different parameter settings for the PECVD of microcrystalline SiGe developed in [42,146] are shown. Here, the results of SiGe depositions on a SiO_2 layer are shown. The corresponding PECVD process parameters are listed in Table 4.7. It can be observed, that the material shown in Figure 4.13 b.I and b.II has the highest degree of crystallisation, while the other layers are mainly amorphous with some embedded

microcrystals.

The results regarding the specific resistivity, ρ, are obtained by 49 measurement points equally distributed over the wafers. While the layers of the materials SiGe-I and -II show higher resistances than the detection limit of the tool, the material SiGe-II shows the expected resistivity compared to the results obtained in [42]. The intrinsic layer stress is slightly higher than the expected value of about 100 MPa. Because also the visual inspection did not show any defects such as delamination or pinholes in the millimetre range, the material SiGe-II is chosen to develop the post-CMOS compatible pressure sensor elements. The parameters are a NTGF= 0.5, $R_{\mathrm{GeH_4}}$ =75 %, a power of 66 W, a substrate temperature of 375 °C and a process pressure of 2.67 hPa.

Table 4.7: Summary of all evaluated characteristics of three different SiGe deposition parameters and deposition on SiO_2 and SiC substrate layers, respectively.

	Characteristics	SiGe - I	SiGe - II	SiGe - III
PECVD parameter	NTGF	1.5	0.5	1.9
	$R_{\mathrm{GeH_4}}$ in %	58	75	58
	Power in W	125	66	125
	Electrode distance in mm	9.37	9.37	9.37
	Substrate Temperature in °C	375	375	375
	Process pressure in hPa	2.67	2.67	2.67
SiGe on SiC	Ge-content in at $-$ %	88 ± 1.8	85 ± 2.0	85 ± 1.9
	Specific resistivity ρ in $\Omega\,\mathrm{mm^2/m}$	n.d.	12.6	n.d.
	Morphology	a/µc	poly-c	a
	Deposition rate in nm/min	484 ± 10	303 ± 6	463 ± 9
	Intrinsic layer stress in MPa	344 ± 14	180 ± 21	370 ± 24
	Visual appearance	Bubbles	Ok	Defects
$SiGe$ on SiO_2	Ge-content in at $-$ %	87 ± 1.7	92 ± 1.7	89 ± 1.7
	Specific resistivity ρ in $\Omega\,\mathrm{mm^2/m}$	n.d.	8.5 ± 3	n.d.
	Morphology	a/µc	poly-c	a
	Deposition rate in nm/min	480 ± 29	305 ± 40	470 ± 35
	Intrinsic layer stress in MPa	246 ± 10	124 ± 8	241 ± 11
	Visual appearance	Spallings	Ok	Ok
	Summary	$-$	$+$	$-$

Patterning of SiGe

In this thesis, the etching of in-situ boron-doped SiGe is investigated for the purposes of patterning the layer in a large magnitude as well as for a minimal open area in the case of enabling etch-access channels for the sacrificial layer release processes. For patterning large amounts of the wafer area, an Cl-based RIE process is found as the best option. As shown in Figure 4.14, patterning of 900 nm SiGe layer on a ≈ 100 nm SiC protection layer on a 200 nm USG layer is achieved with a very acceptable over-etching (≈ 50 nm) into the SiC protection layer with a relatively high etch rate of ≈ 10 nm/s. Some of the main advantages are a sufficient endpoint detection by monitoring the Ge concentration in the process plasma due to the significantly higher selectivity of Cl to SiC compared to SiGe, or the high on wafer uniformity. However, an edge rounding is observed at the bottom of the SiGe layer, even though the wafer is not released to atmospheric pressure, but directly transferred to a strip chamber under vacuum conditions. This edge rounding is tolerable for the patterning of conductive lines or the outer diaphragm shapes of the 2nd MEMS wiring level because the minimal structure length/width are designed relatively large (7.2 µm).

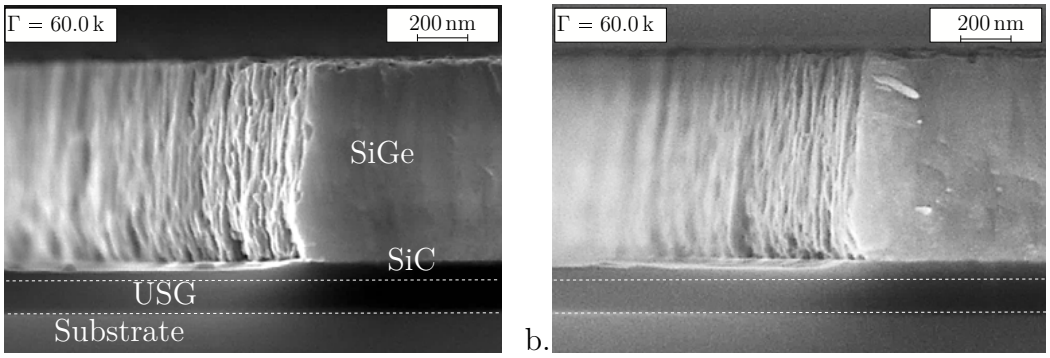


Figure 4.14: SEM cross-section at a structure edge of a SiGe layer of ≈ 900 nm on a ≈ 100 nm SiC protection layer on a 200 nm USG layer at different positions on a 200 mm wafer: a. Centre b. Edge (Notch).

Connectivity of SiGe to 1st MEMS wiring level

SiGe is utilised as the 2nd MEMS-circuit-level material and, thus, formed as the diaphragm electrode of the capacitor structures. A through-hole plating, also referred to as a *via*, between SiGe and the material of 1st MEMS wiring level has to be established. First, the metal, which forms the bottom electrode of the

capacitor, should have only minimal effects on the shape of the surface profile of the diaphragm. An effect on the shape of the sensitive diaphragm area is possible due to a design rule. In designing the maskset it was defined, that the diameter of the 1st capacitor electrode must be smaller than the diameter of the cavity for the purpose that parasitic capacitances are avoided at the surrounding of diaphragms. Therefore, either a relatively thin layer is required, or, alternatively, CMP processes would become necessary. In this thesis, the approach of a thin layer as the 1st MEMS wiring level is used. This, in turn, implies for example etching processes to partly remove the overlaying layers with high selectivity against the metal of choice. Otherwise, the risk of over-etching thin metal layers inhibits the connectivity.

Here, the selectivity of the SiC etch process with respect to the etching of TiW is significant. An F-based RIE is developed to pattern SiC with end-point detection included. In case of TiW utilised as the 1st wiring level, an appropriate end-point detection is achieved. In order to evaluate the quality of electrical contacts between TiW and SiGe, test structures with meander-shaped conductive lines with lengths l_{M-test} of about 6.8 mm and widths of about 6 µm (Figure 4.15 a.) are used to evaluate the individual resistivity of the 1st and 2nd wiring level. Another test structure with a length of $l_{Via-test}$ of about 2.8 mm and a width of about 6 µm combines both wiring levels by 154 vias in total (Figure 4.15 b.). Here, TiW and SiGe as the 1st and 2nd wiring level respectively, are deposited with similar layer heights between 90 nm to 100 nm, isolated by a 100 nm SiC layer. To create such vias, the isolating protection layer made of SiC is patterned with the aid of F-based RIE. In (Figure 4.15 c.) a SEM cross-section shows the conjunction of SiGe and TiW in a single via. It can be seen that only a very thin TiW film of approximately less than 20 nm is left after SiC patterning, which means an over-etch of approximately 80 %. This indicates that the end-point detection is sufficient. However, it becomes obvious that this process is critical due to the risk of over-etching. Thus the process parameter and end-point detection should be improved in order to increase the selectivity and prevent potential yield losses.

Nevertheless, sufficient resistances are detected at 5 equally distributed positions on a wafer. In Figure 4.15 the results of IV measurements performed with an *Agilent 4155C Semiconductor Parameter Analyser* are shown as an example for the centre position of a wafer. Since the applied voltage generates a current which

is linearly dependent on the resistance of the test structure according to Ohm's law, ohmic behaviour can be assumed.

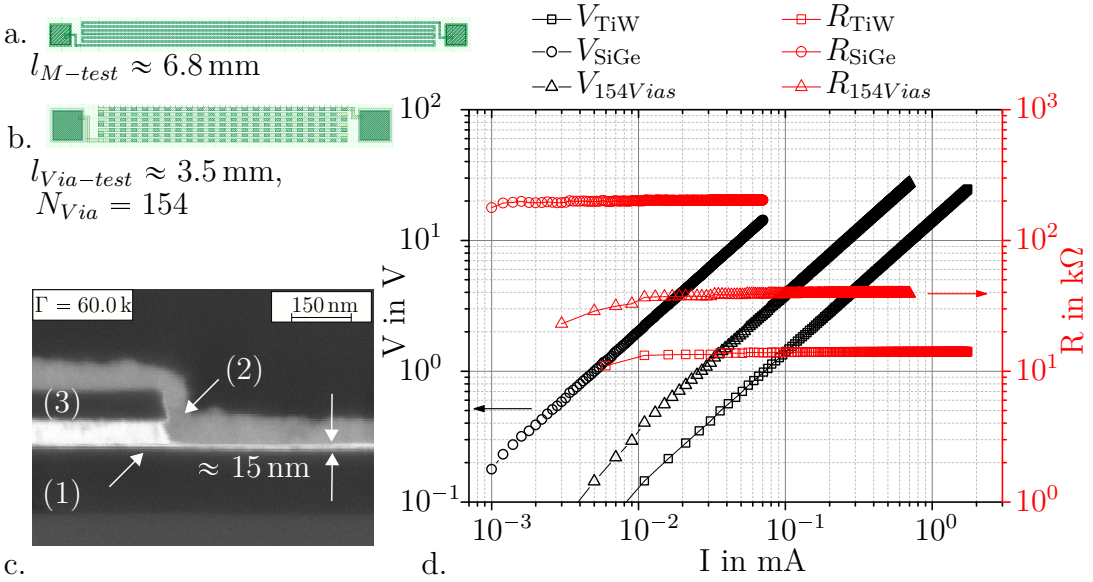


Figure 4.15: a. Design of meander test structure for 1st and 2nd wiring level, respectively, b. design of test structure for a via chain comprising 154 vias, c. SEM cross section of via made of TiW (1) and SiGe (2) isolated by SiC (3), and d. results of resistance measurements.

The resistances R measured here for the TiW and SiGe meander test structures shown in Figure 4.15 are 14 kΩ and 203 kΩ, respectively. Hereby, the material specific electrical resistance ρ is calculated with:

$$\rho = R \cdot \frac{h \cdot w}{l} \tag{4.1}$$

where h is the height of the wiring layers, w is the width of the wiring, and l is the length of the test-structure. The resistance of the test structure comprising 154 vias yields 39 kΩ. Finally, the mean resistance of a single via can be calculated by using the individual specific resistances of TiW and SiGe obtained by Equation 4.1, and their different geometric contributions to the via structure. Thus, single vias show a mean resistance of 52 Ω with a 1σ deviation of about 68 %. In Table 4.8, the results of the measurements are summarised. On the one hand, a relatively high 1σ deviation of about 68 % can be observed. This is primarily due to results obtained from a certain area of the examined wafer which demonstrates the sensitivity of the RIE process applied for the via opening. On the other

Table 4.8: Summary of resistance measurements of TiW and SiGe wiring levels for 5 equally distributed structures on a 200 mm wafer.

Structure	h in nm	w in µm	l in mm	Mean R in Ω	1σ dev. in %	ρ in $\Omega\,\mathrm{mm}^2/\mathrm{m}$
TiW meander	≈ 90	6	6.8	17.3×10^3	26.5	1.4
SiGe meander	≈ 100	6	6.8	197.1×10^3	3.9	17.3
Via structure	≈ 90 to 115	6	3.5	4.0×10^4	14.8	-
154 Vias only	≈ 115	4	1.2	8.0×10^3	68	-
1 Via only	≈ 115	4	8×10^{-3}	52.1	68	-

hand, the results regarding the vias show low ohmic resistances which indicate an appropriate contact forming.
The determined specific resistances for both TiW and SiGe are about 25 % to 45 % higher than determined before. In the case of SiGe, $12.6\,\Omega\,\mathrm{mm}^2/\mathrm{m}$ have been presented in Table 4.7. Here, the layer thickness was much higher (≈1.6 µm, see Figure 4.13). This indicates that the 100 nm SiGe layer used here for test purposes can have an inhibited conductivity, possibly due to the layer growth mechanisms. Therefore, an improved electric conductivity can be expected for the targeted layer thickness (about 1 µm) of the PECVD SiGe 2nd wiring level.
For TiW, the specific resistance evaluated before is about $0.8\,\Omega\,\mathrm{mm}^2/\mathrm{m}$ (see Table 4.5) and was measured with a comparable layer thickness. This could indicate contact issues at the contact pad which is made of sputter-deposited AlSi. As the primary purpose of this AlSi is to establish a bond pad, this is further evaluated in Chapter 4.2.6 on Page 122.

Etch-access Patterning of 2nd MEMS wiring level

As motivated in Chapter 3.1.2 (Design of Etch Access Channels), a diaphragm perforation by laterally-arranged vertical etch-access channels is the very best solution regarding the release etch. This applies all the more since only low process pressures in vapour phase HF/H_2O etching should be applied in order to avoid stiction, as evaluated in Chapter 4.2.4. The consequence is that only low lateral etching rates are applicable. This further depreciates the alternative etch-access methods, because they require long lateral etching paths. However, primarily three disadvantages regarding the diaphragm cover, the impact on mechanical

stress and the absolute sensor signal are identified. All these disadvantages are significantly minimised or even eliminated if the areas of the etch-access channels are minimised. Therefore, a size reduction of circular shaped etch-access channels in released MEMS-structures is developed in this thesis [187,200] after [186], which is presented in Figure 4.16 as a schematic not to scale.

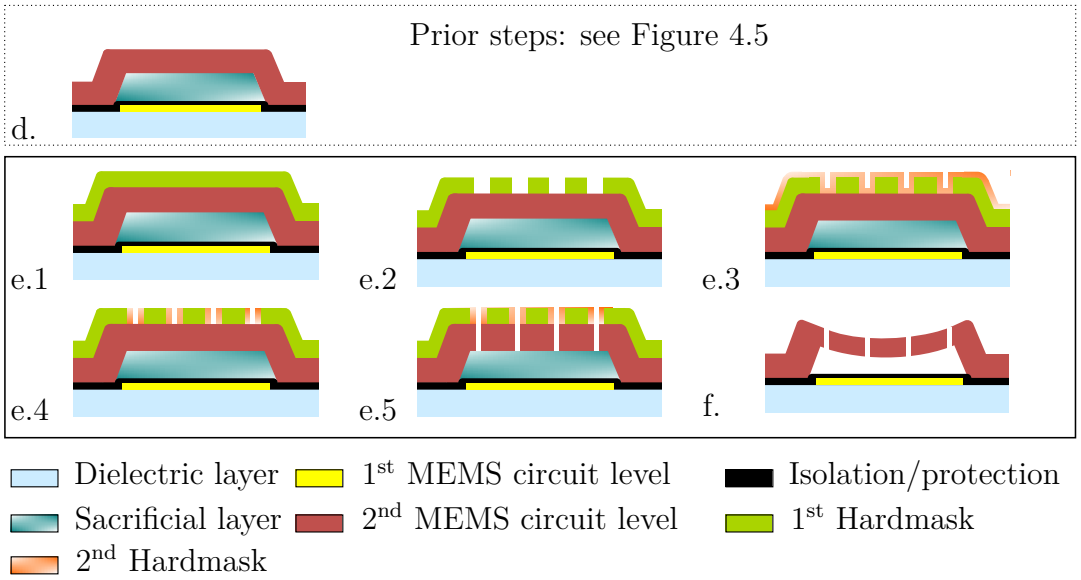


Figure 4.16: Schematic fabrication sub-flow of the side-wall spacer process: d. 2nd MEMS wiring level is the top layer to be patterned represents the starting point, e.1 deposition of 1st hardmask, e.2 patterning of 1st hardmask with the aid of photolithographically patterned resist and RIE, e.3 deposition of 2nd hardmask as side-wall-spacer layer, e.4 RIE of 2nd hardmask until 2nd MEMS wiring level is opened, e.5 etching of 2nd MEMS wiring level creates etch-access channels to sacrificial layer, f. in-situ hardmask removal and sacrificial layer release etch.

Process Flow Side-Wall Spacer The presented sub-process sequences are applied to a wafer with a closed SiGe layer with a patterned sacrificial layer and 1st MEMS wiring level layer protected by SiC underneath (d.). At first, a 1st hardmask layer (e.1) is deposited. After a photoresist has been patterned, the 1st hardmask is etched anisotropically with the aid of an F-based RIE until the structural layer (SiGe) has been reached (e.2). Further, the resist is removed via plasma stripping, then a 2nd hardmask is deposited (e.3). Here, two different options are developed: first, if the structural layer is much thinner than the diameter of the etch-access channels, an appropriate ratio of edge overgrowth

to channel filling grade is established which is not drawn in the schematic flow. Second, if the thickness of the structural layer is equal or thicker than the 1st hardmask, a conformal deposition of the 2nd hardmask is applied, as drawn in Figure 4.16 e.3. The next step (e.4) implies an RIE process, which again removes the 2nd hardmask anisotropically, in order to reveal the surface of the SiGe layer. Finally, the remaining openings are narrowed due to the now visible side-wall spacers. Due to further applied RIE processes, this patterning is transferred into the structural layer. It is important to distinguish between the above mentioned cases: a 2nd MEMS structural layer much thinner than the 1st hardmask can effectively be patterned by an RIE process and a side-wall spacer, which comprises the effect of edge overgrowth. Otherwise, given an equal or higher layer thickness of the structural layer, a highly anisotropic etching sequence is required. Finally, the remaining openings were transferred into the structural layer by applying an anisotropic RIE process (e.5). Here, anisotropic RIE is only appropriate if the structural layer thickness is smaller than the thickness of the 2nd hardmask. If the structural layer thicknesses become larger than the thicknesses of the 2nd hardmask, which is limited due to the lithographically established radius of the first pattern, a time-multiplexed etching (Bosch-process) with C_4F_8 cycles for passivation can be applied. Here, much higher aspect ratios due to a sharply increased selectivity are obtained.

After releasing the patterned structural layer by vapour-phase etching, the hardmasks have to be removed (f.). In order to remove both the sacrificial layer and the hardmasks in a single etching step, only SiO_2-based materials are chosen.

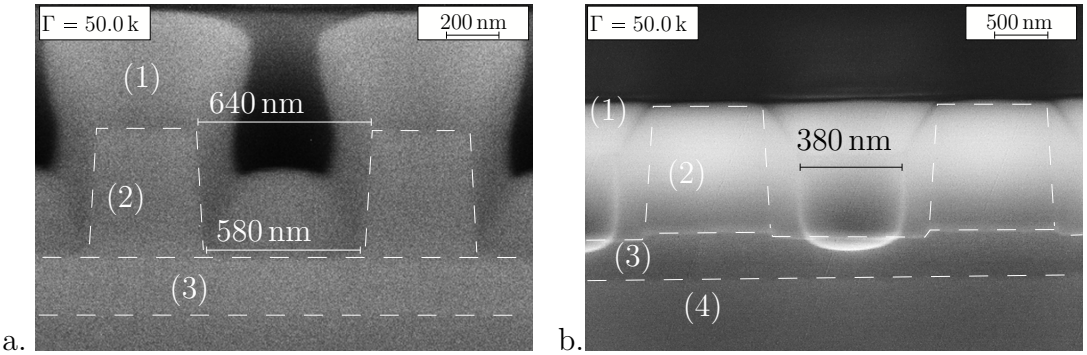


Figure 4.17: SEM cross sections of a. applied hardmasks (1) and (2) on a structural layer (3) on a sacrificial layer (4) and b. after opening the 2nd hardmask to the structural layer via RIE.

In Figure 4.17, first a USG-hardmask with a layer height of 500 nm is deposited and then lithographically patterned. The structure width was designed as 500 nm. After lithographical patterning, the structure width is about 640 nm. A 2nd hardmask made of TEOS SiO_2 is deposited via ICPECVD, afterwards. The original layer thickness of the 1st hardmask of about 500 nm is reduced to about 380 nm after applying a 2nd hardmask and RIE to open the masks to the structural layer.

SiGe-Etch-Access-channel Etching via SiO_2 hardmasks Different processes are tested to transfer the structures of the hardmasks into the SiGe diaphragm. Ideally, an etching stop is achieved on the sacrificial layer material. This requires a high selectivity of the etch process between SiGe and SiO_2. A potentially suitable process is the chlorine-based RIE process from Chapter 4.2.3, which showed a desired selectivity.
In Figure 4.18 the results of applying a chlorine-based RIE to pattern are shown for the centre (a.) and the edge (b.) of a wafer. The hardmasks (1) are slightly etched and the etch-access channels are widened (2) by approximately 60 nm to 80 nm compared to Figure 4.17. Below the hardmasks, a clear over-etching of the SiGe (3) is visible. It is interesting to note that increased etching occurs especially at the bottom of the cavity. This gives the cavity the shape of a truncated cone. It may be assumed that the ions have experienced a strong acceleration through the plasma, so that the ions get deep into the cavity before a chemical reaction takes place.

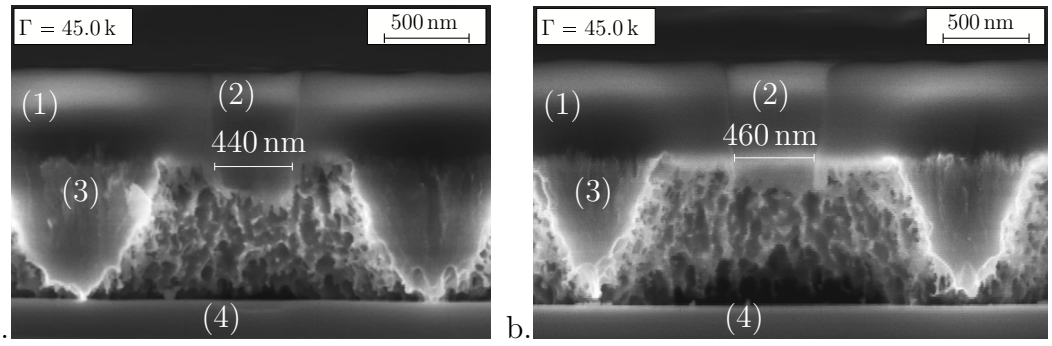


Figure 4.18: SEM cross-section of an already patterned SiO_2 hardmask (1) (finally ≈530 nm) on a SiGe (≈900 nm) on USG (≈200 nm) (4), after a Cl-based RIE (BCl_3, Cl_2, N_2) is applied to create etch-access channels (2) the SiGe at: a. centre and b. edge of a wafer.

The patterning of etch-access channels is obviously different compared to the patterning of large areas, because only a very small area of the SiGe layer is exposed to the etchant. In this case, the edge rounding becomes intolerable in case of an excessive etching reaction and a proportionately poor endpoint signal. Therefore, an alternative etching process for the patterning of etch-access channel into a SiGe layer is tested. In Figure 4.19 a. and b., a fluorine-based RIE process is applied to pattern the etch-access channels via a SiO_2 hardmask (1). Again, the centre (a.) and the edge (b.) of a wafer are shown. This process shows a very poor selectivity between SiGe (2) and SiO_2 (1, 4). Additionally, etch rates vary greatly between the centre and the edge. Thus, such a process is also unfavourable.

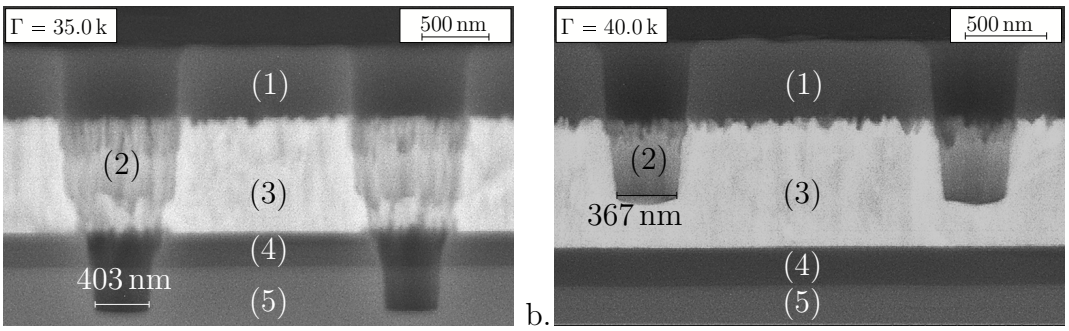
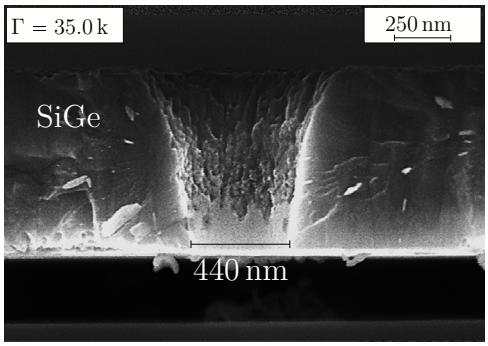


Figure 4.19: SEM cross-section of an already patterned SiO_2 hardmask (1) (finally ≈520 nm) on a SiGe (≈900 nm) on USG (≈200 nm) (4), after an F-based RIE (CHF_3, CF_4, Ar) is applied to create etch-access channels (2) in the SiGe at: a. centre and b. edge of a wafer.

Nevertheless, by optimising the applied time, etch-access channels can be realised via fluorine-based RIE. This is demonstrated in Figure 4.20 a.. Here, the result is shown after the patterning of a SiGe structural layer through hardmasks with effective side-wall spacers and, additionally, simultaneous sacrificial-layer-release and mask-removal etch by the use of vHF, were applied. This result is compared to Figure 4.20 b. which shows the same condition after having applied a DRIE Bosch process. The effect of side-wall spacer is exploited more effectively by applying DRIE. First, the shape of the channels helps to evaluate the effectiveness of the etch processes. Second, minimal diameters of about 440 nm in a. are compared to about 350 nm in b. The characteristic shape in 4.20 b. is due to the applied Bosch-process, where an alternating sequence of etching and passivation was run. It is assumed that the designed diameter of 500 nm showed about more

than 600 nm after patterning the 1st hardmask, as already seen in Figure 4.17 a.. Unfortunately, in b. stiction occurred due to further applied process steps as for example stripping a previous lithography mask. This leads to an outlook: an important consequence, closing the diaphragms must be applied until further lithographic or wet cleaning processes can be applied.
On the basis of Figure 4.20 a., a disadvantage of an RIE process for etch-access-channel etching can be discussed. Due to an imperfect anisotropy of the examined RIE processes, the etch-access channels become widened again. This is avoided by the alternating Bosch-process because the sequential exposure to C_4F_8 gas leads to the deposition of a thin passivation layer, which is the partially opened due to the accelerated ions resulting in a vertical ion bombardment. Furthermore, the selectivity of SiGe compared to SiO_2 is very high ($\gg 50:1$) [184]. The SiGe etching rates of the applied SF_6-based DRIE process are in the magnitude of 20 nm/s to 30 nm/s. Here, reported etch rates of 15 nm/s to 25 nm/s can be confirmed [184]. Therefore, a very good uniformity over the complete wafer area can be expected. The total thickness of the hardmask may further be smaller than diaphragm thickness thanks to the very high selectivity. This simplifies the dimensioning of layer thicknesses and process effort.

a. 

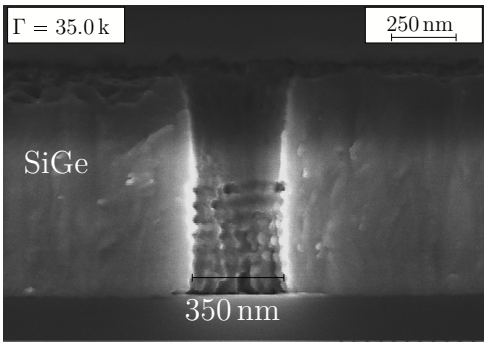
b. 

Figure 4.20: SEM cross sections of patterned 900 nm SiGe structural layers after applied hardmask processes and vapour HF exposure: a. RIE, b. DRIE.

In conclusion, an appropriate setup to pattern the SiGe structural layer consists of two hardmasks, of which the 1st has a layer thickness of about the diameter of the designed etch-access channels, i.e. 500 nm. The 2nd hardmask can be USG as well, whereas TEOS-SiO_2 is used in the presented results. Here, the lateral layer thickness must not exceed the diameter of the patterning, which is etched into the 1st hardmask. Otherwise, the side-wall spacer would be ineffective. Amongst

the applied etching processes to pattern a SiGe structural layer in the order of 900 nm thickness, minimal etch-access-channel diameters can be realised with the aid of the Bosch-process, which therefore is the most effective method.

4.2.4 Sacrificial-Layer-Release-Etch Technology

Sacrificial Layer Patterning

The angle of the sacrificial layer's side wall has an impact on the diaphragm suspension (stress, fracture, shape). Smooth side wall angles much lower than 90° are desirable to minimise parasitic mechanical effects. In this thesis a focus variation in the photoresist exposure is evaluated. In order to explain the idea of defocusing, the best focus is defined as placing the plane at the centre of a photoresist. A positive focal position is focusing above the centre of a photoresist and a negative focal position means focusing below this position. A negative focus error will cause the top of the photoresist to be more out of focus than the bottom. The cross-sectional view will look a photoresist profile that has a sharper, more ideal shape at the bottom than at the top. A positive focus error, however, will move the bottom farther out of focus than the top and the bottom will have a more rounded, out-of-focus shape than the top [201].
By this means and under fixed conditions of exposure time, oxide etch and photoresist removal conditions, the side wall angle is controllable in a wide range. The results of a focus variation are shown in Figure 4.21. The SEM cross sections of three different focus settings ranging from 0 µm to 0.6 µm are shown in a. to c. which indicate that the optimum of about 50° can be found for a slightly higher focus than 0.6 µm.
An option, which can be applied additionally or alternatively, can be an exposure to vapour HF after RIE of the masked sacrificial layer in order to decrease the side wall angles. This step should be kept very short and should immediately be concluded by a resist removal step. It is reported that photoresist remained stable after etching in these tests, but peeled when rinsed [184].

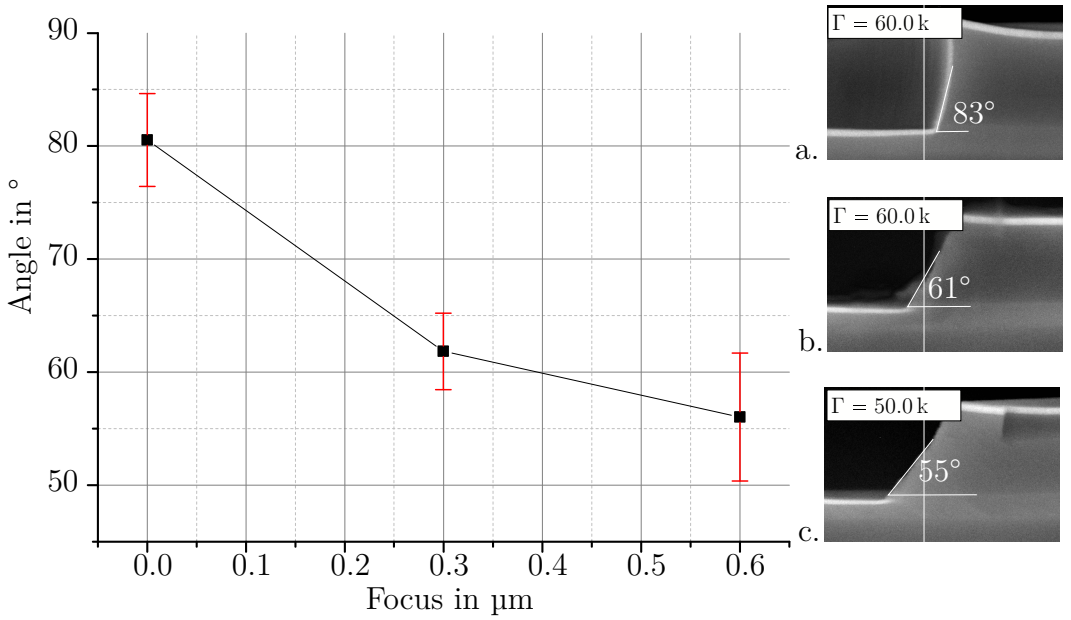


Figure 4.21: Focus variation and resulting side-wall angle of SiO_2 sacrificial layer after RIE with shown SEM cross sections (which show an additionally sputtered thin metal layer for improved contrast), a. $f = 0.0$, b. $f = 0.3$, c. $f = 0.6$.

Vapour-Phase Sacrificial Layer Etching

The development of an appropriate process chain is absolutely dependent on the characteristics of the sacrificial layer release etch. Here, vapour HF etching against SiO_2 is the preferable choice compared to vapour XeF_2 against amorphous Si, as introduced before. In principle, a successful release is achieved if the released structure is intact, free of any stiction effects and all the sacrificial layer is removed.

In order to evaluate the sacrificial layer release process, test structures are fabricated. These include a patterned TEOS SiO_2 with a thickness of about 500 nm and a further structural layer made of SiC with a thickness of about 200 nm. A thin SiC is chosen in order to enable high visibility of the under-etching via microscope inspections. The results are drawn in Figure 4.22 a.. The test structures, which are shown in Figure 4.22 b. to d., are used to determine the specific progress of under etching a structure layer after applying vapour HF against a SiO_2 layer with a thickness of about 500 nm. Here, an error of reading of $\pm$ 2 µm is assumed.

The specific etch rates show a light decline over the applied exposure time. Possi-

ble reasons may be diffusion limitations of either HF from the surface of the liquid layer, or of the etching products. This could lead to concentration gradients in the space close to the edge frontier and cause a decrease of the etching rate. Another potential reason could be stress of the thin layers used here, which may cause a reduction in the cross-sectional area due to intrinsic layer stress. However, this phenomenon is not further investigated because it becomes insignificant for two reasons: low specific etching rates and the stiction effect.

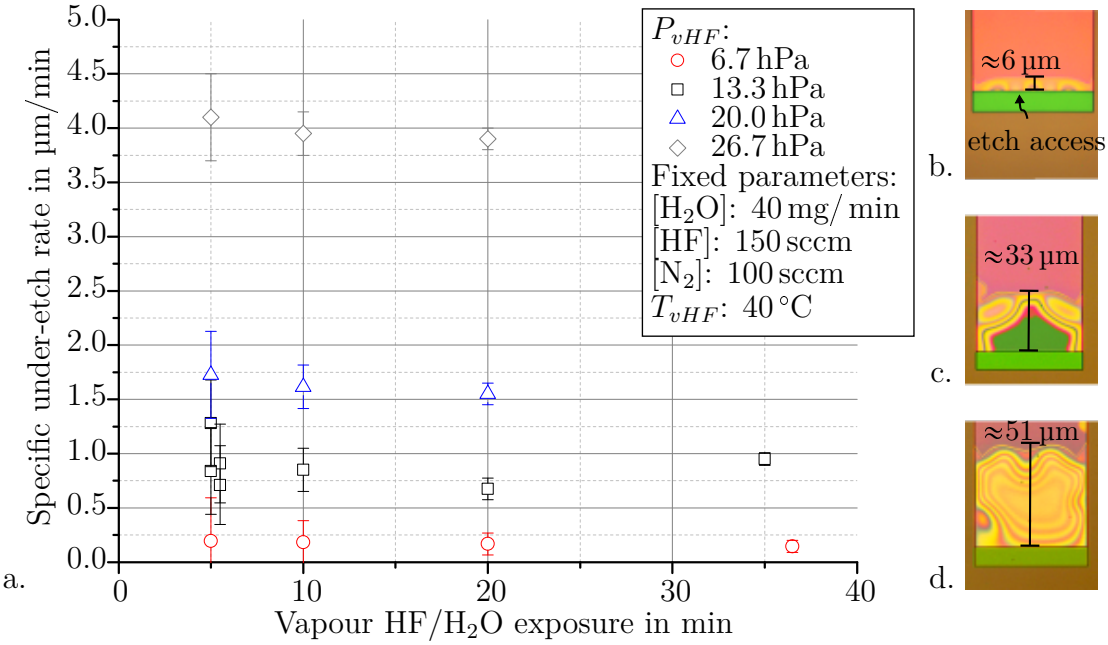


Figure 4.22: a. Specific vapour HF etch rate for a TEOS SiO_2 sacrificial layer height of $\approx$ 500 nm versus pressure and versus time. The corresponding data are collected with test structures shown in b., c. and d., which have an etch-access at the lower edge, show the etch progress after 5 min, 36 min and 56 min at 13.3 hPa vapour HF process pressure.

The etch rates are so low that the release process of diaphragms with diameters of 100 µm to 300 µm becomes very time consuming. For example a given diaphragm diameter of 300 µm, a sacrificial layer thickness of 500 nm and vertical arranged etch-access openings at the edges of the diaphragm area would consume about 2.5 h at a process pressure of 13.3 hPa with a given specific under-etching rate of 1 µm/min at maximum. In Figure 4.23 the etch progress is made visible via microscope inspection for three different design options of the etch access. Single diaphragms with a diameter of 300 µm are shown after a vapour HF exposure time of 1 min and 35 min, respectively. The depicted diaphragms obtain

surface perforations with a designed diameter of 500 nm arranged in a pitch of 2 µm over a diaphragm diameter of 300 µm, or in a band with a width of 15 µm, respectively (see Figure 4.23 column one and two). The third design option shows 4 slits in the form of 1/8 circle segments. The surface perforation design in column one perfectly demonstrates the advantages of very quick sacrificial layer release within a few minutes. In this configuration, a 5 min to 10 min vapour HF exposure at 13.3 hPa would have been sufficient.

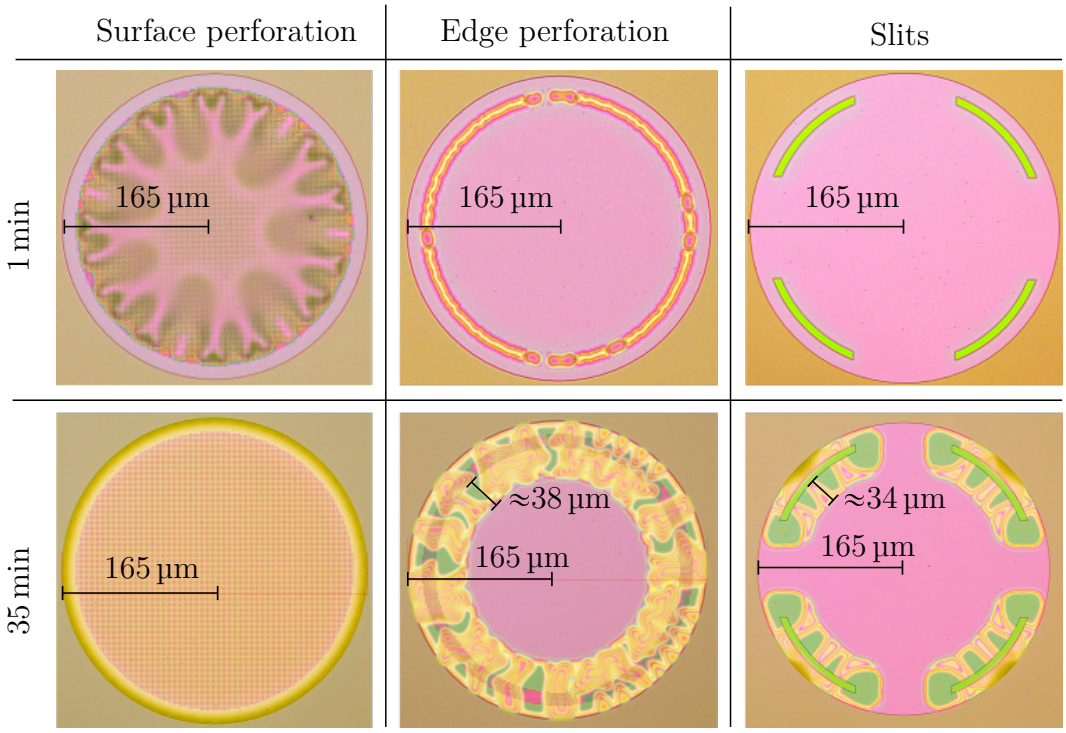


Figure 4.23: Etch progress after 1 min and 35 min vapour HF exposure at 13.3 hPa of different etch-access designs.

Higher vapour-phase etching process pressure are beneficial to completely release large MEMS structures. However, the stiction effect is observed at a threshold of a vapour HF process pressure of about 13.3 hPa. Since H_2O is a by-product of the sacrificial layer etching reaction, the stiction effect occurs most probably due to a large surplus of water. Unfortunately, there has been no method reported so far, as to how to undo the stiction effect by methods of surface micromachining, whereas some methods are known how to prevent the occurrence of stiction, as discussed in Equation 2.2.3, Stiction. None of the mentioned methods is included in the process chain so far, because all require additional, partly very

special process steps or are hardly available. Thus, a design considering a surface perforation of diaphragms with diameters of 100 µm to 300 µm and cavity heights in the range of 300 nm to 1000 nm with a high density of etch-access channels and a vapour-phase etching process pressure of 13.3 hPa or less is identified as a preferable parameter setting for a stiction-free release etch. This verifies the observations in [202]. Further, no iterative processes are necessary, as applied in [70, 109], but a single, continuous procedure can be applied.

4.2.5 Diaphragm and Etch-access Channel Cover

Within this caption, the closing of the open diaphragms by cover layers is evaluated. So far, vertical etch-access channels turned out to be very advantageous regarding the sacrificial layer release. However, to close these channels is another challenge. The primary purposes of closing the diaphragms are to provide:

- Protection from the external environment (dust, humidity etc.).
- A controlled cavity pressure by limiting any diffusion from environment and by avoiding any outgassing effects of the sealing layer.
- Electrical isolation.

In this thesis three approaches are discussed: First, an anisotropic ICPECVD process utilising TEOS SiO_2 as cover material is investigated. Second, an isotropic low temperature CVD process for SiGe is developed and evaluated as cover. Third, a heterogeneous ALD composite layer made of Al_2O_3 and ZnO is investigated as a selective etch membrane, which further supports the cover layer.

SiO_2 ICPECVD Diaphragm Cover

First, diaphragms are lithographically patterned and released stiction-free with the aid of vapour-phase etching. Subsequently, an appropriate anisotropic PECVD is applied to directly cover these diaphragms. The results are shown in Figure 4.24. Here, a total cover layer height of 1.5 µm is applied. It can be seen that a cover layer thickness of at least 500 nm is necessary to close etch-access channels with a diameter of about 630 nm. The sealing material is a TEOS SiO_2. The deposition parameters are optimised to promote the sealing due to an edge over-growth. Figure 4.24 indicates the deposition inside the cavity through the

relatively large etch accesses. These bumps show a height of up to 250 nm at some positions.
On the one hand, a PECVD cover process shows the little advantages of reduced and only local deposition in the cavity. The tuning in order to support an improved layer growth at the edges to close the channels more quickly with even less deposition into the cavity is possible, as well as applying low temperature processes.

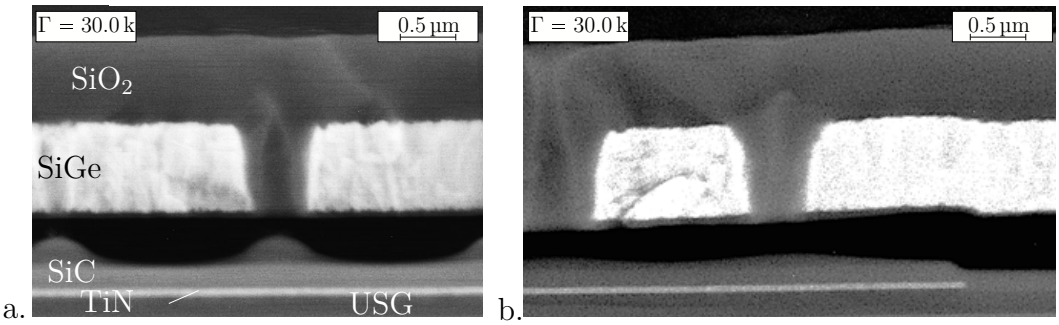


Figure 4.24: SEM cross-section of a SiGe diaphragm with etch-access channels with diameters of ≈ 400 nm, through which 500 nm SiO_2 sacrificial layer is released via vHF. The 1st MEMS wiring level is 50 nm TiN protected by ≈ 150 nm SiC. The diaphragm is closed by ≈ 600 nm ICPECVD SiO_2. a. further shows the deposition into the cavity, while b. shows the edge of the TiN as 1st MEMS wiring level.

On the other hand, there is the disadvantage of extra heat induced due to plasma in the centre of diaphragm, which hardly dissipates to the substrate. This effect even increases for larger distances between the diaphragm centre to edges, at which the heat can principally dissipate into the substrate. This locally increased heat is assumed to cause a difference in material expansion, which can lead to either an increased deflection or a curvature in the opposite direction of the intended deflection. Such a buckling effect is observed.

SiGe CVD Diaphragm Cover

An alternative approach is to apply a CVD process. The first intention is, to prevent plasma induced heat. In general, CVD layer growth can be divided into different phases: First during nucleation growth (coalescence) the formed grains show tendencies to bond with each other resulting in tensile stress. Second, beginning the vertical grain growth phase: if grains grow in a V-shaped manner,

compressive strain is generated. This means, stress depends on layer thickness. In this thesis, a filling of the etch-access channels is desired. This means, layer thicknesses of about 200 nm to 400 nm become necessary. The investigated layers should be in this range. In the case of fully filled etch-access channels, the layers can be etched back with a stop on PECVD SiGe by the use of endpoint detection for the dopant B, if necessary.

The SiGe CVD and PECVD processes are all performed in a *Precision* 5000 cold wall CVD-system by AMAT in a *Centura CxZ* chamber. The substrate temperature for all depositions is about 375 °C and the process pressure is kept at the available minimum of 2.67 hPa.

In Figure 4.25 the growth of CVD SiGe (4) with different R_{GeH_4} on undoped 800 nm PECVD SiGe test structures (3) is shown. For increasing ratios, the surface roughness and, thus, the grain sizes are visibly increasing. Further, different incubation times can be observed. These are due to different surface characteristics of the exposed materials, such as crystal grains. In the shown example, the areas between the PECVD SiGe show the gradual formation of a nucleation layer. Here, the growth is inhibited because SiO_2 (2) is exposed to the process gases instead of SiGe (3). Incubation times are reported in the range of minutes for SiO_2 [153].

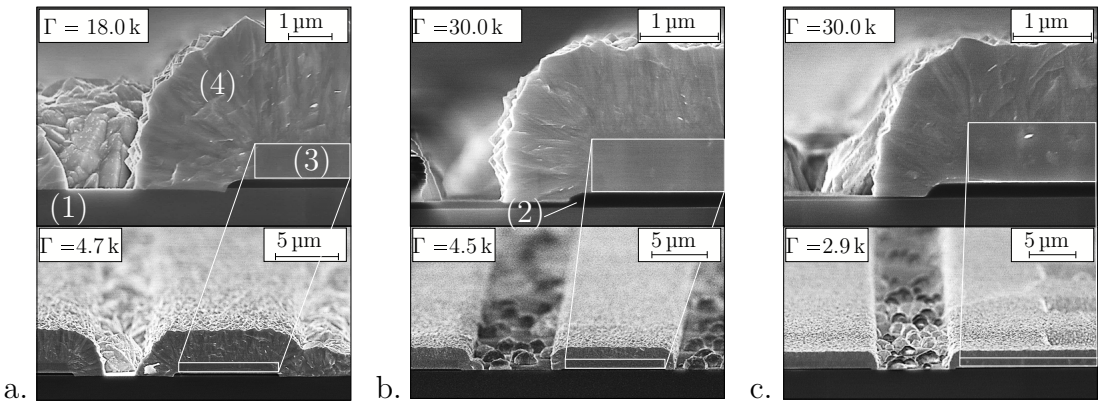


Figure 4.25: CVD-SiGe deposition with fixed GeH_4-flow on 800 nm undoped PECVD SiGe test structures, which are patterned via photoresist mask and RIE etching. a. $R_{GeH_4} \approx 60\,\%$, b. $R_{GeH_4} \approx 50\,\%$, c. $R_{GeH_4} \approx 40\,\%$.

In Figure 4.26 the schematic process flow for the fabrication of test structures is shown, which are used to evaluate the CVD SiGe developments regarding their

impact on diaphragms. Simple test structures comprise a Si substrate (1), a SiO_2 sacrificial layer (2) and a PECVD SiGe layer (3), which is patterned as described via DRIE. Thus, etch accesses are established (4). Here, no side-wall spacer is applied in order to minimise the efforts. By applying a time-controlled vHF release etch, the cavity is created (5). Finally, the patterned SiGe layer is used as seed layer to develop an appropriate CVD SiGe cover layer process. This CVD layer will potentially show deposition inside the cavity (6).

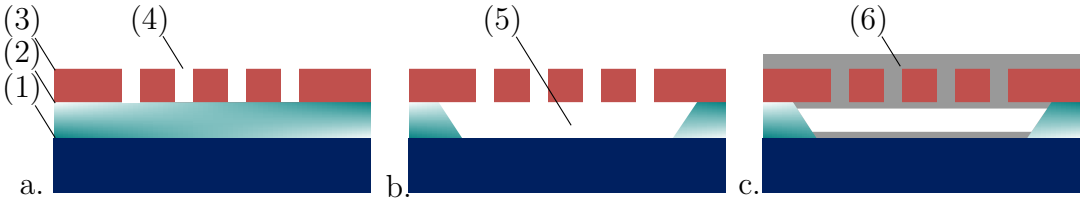


Figure 4.26: A Si substrate (1) utilised and a sacrificial layer is deposited (2), followed by a PECVD SiGe layer (3). This layer is patterned (4) via a photoresist and DRIE (a.). The vapour HFrelease etch is applied and a cavity is created (5, b.). Finally, the CVD SiGe (6) process is applied with possible depositions in the cavity (c.)

By using the sketched test structures, the influence of a few deposition parameters on layer stress has been evaluated. First, the influence of Ar during the CVD of SiGe is investigated. Second, the influence of the GeH_4 to SiH_4 ratio at a constant SiH_4 flow of 150 sccm min is evaluated. To determine the influence on the intrinsic layer stress, the wafer bow was measured by a wafer geometry measuring instrument *MX208* from *E+H Metrology*. The differences of the measured centre bows ΔB_c are used to calculate the intrinsic layer stress after estimating the layer thickness t_f of the SiGe CVD process with the aid of SEM cross sections with [203]

$$\sigma_i = \frac{4 \cdot \Delta B_c \cdot t_s^2}{3 \cdot d^2 \cdot t_f} \cdot 180.4\,\text{GPa}, \tag{4.2}$$

where t_s is the nominal thickness of the substrate and d is the wafer diameter. The wafer diameter is assumed to be constantly 200 mm and an edge exclusion of 8 mm must be considered. The substrates thickness t_s is about 725 µm. Further, equation 4.2 considers the anisotropic biaxial module of $\langle 100 \rangle$ Si with 180.4 GPa. First trials utilising a CVD SiGe process to cover PECVD SiGe diaphragms have been evaluated in [42]. Applied process parameters of a NTGF of 0.25 and R_{GeH_4} of $\approx$ 0.58 showed a small tensile stress of about 65 MPa on plane substrates.

Here, B_2H_6 has been applied. If a layer with tensile stress is suspended above a substrate and anchored to it at only few points, the layer will be stretched by the substrate. Thus, applying this layer to SiGe diaphragms with laterally-arranged etch-access channels showed an upturned deformation. This deformation was reversible, as demonstrated by a removal via a RIE process [42].
In this thesis, the situation is different due to the vertically-arranged etch-access channels. First, the cover layer must not be conductive in order to maintain the electrode arrangement of a capacitive pressure sensor. Second, as sketched in Figure 4.26, the deformation of a diaphragm is probably influenced by the deposition in the channels, at the backside of the cavity and at the surface of the diaphragm. To simplify this situation, the etch-access channel filling is neglected. Due to the introduced side-wall spacer sub-flow, the etch-access channels finally become significantly smaller compared to the overall layer thickness. Thus, there is a three-layer stack consisting first of the PECVD SiGe in the centre. Second, a thin CVD SiGe layer is deposited at the backside of the diaphragm, while the layer thickness is determined by the radius of the etch-access channels. Third, a CVD SiGe layer with variable thickness on the surface is considered.
In Figure 4.27 the results of applied process variations are shown with the aid of SEM cross sections at the edges of cavities. The variation of the TGF from 0.25 to 0.75 under a fixed R_{GeH_4} of ≈ 0.58 shows that the selectivity of the deposition can be controlled. In Figure 4.27 a. the SiO_2 remains free from CVD SiGe (2), while an increased TGF tends to conformally cover all of the exposed surfaces, which are SiGe (1) at the diaphragm surfaces, the SiO_2 (3) of the sacrificial layer, and the surface of the Si (4) substrate (Figure 4.27 b.). Similar deposition rates are observed for different TGFs.
In comparison to this, in Figure 4.27 c. and d. the effect of no Ar dilution shows selective deposition properties, which exlude the sacrificial layer surface. The comparison of a difference in etch-access diameter of 200 nm is in aggreement with the measureable layer thicknesses in the cavity, which are about 390 nm in Figure 4.27 c. and about 180 nm in Figure 4.27 d.. The forming of columnar crystals during the deposition, which grow vertically and in-plane, usually leads to a high deposition rate, and often does result in compressive stress. This is because the formed crystals push their neighbours. Lower deposition rates, on the contrary, are observed if the growth is initially amorphous. If the layer changes to

crystalline during further growth, equi-axed, largely isotropic crystals can result. These crystals have higher densities and, thus, tend to show tensile stress with small stress gradients. Intrinsic layer stress control is desired in order to form a convex shape of closed diaphragms.

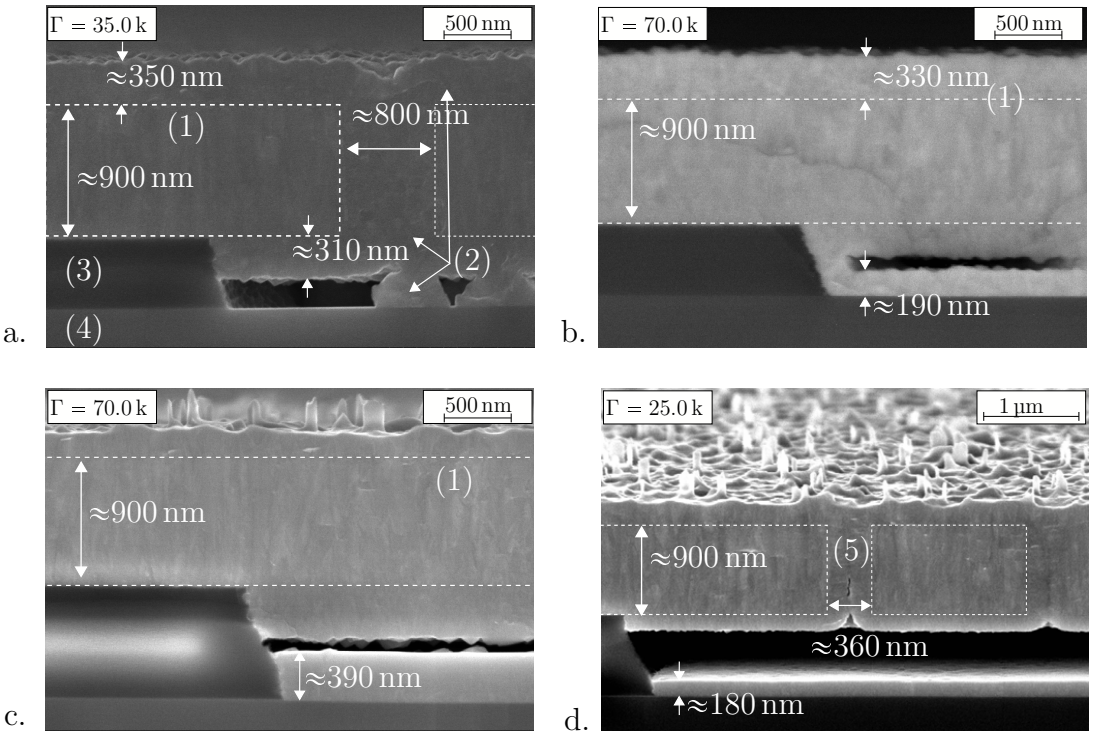


Figure 4.27: SEM cross sections of test structures with etch-access channel diameters of about 800 nm and varied CVD process parameters: a. with a NTGF of 0.25 and R_{GeH_4} of ≈ 0.58, b. with a NTGF of 0.75 and R_{GeH_4} of ≈ 0.58. In c. and d. different etch-access channel diameters are covered without Ar-dilution and a R_{GeH_4} of ≈ 0.52.

While variations in the NTGF in Ar-diluted processes showed hardly any impacts on layer stress and deposition rates, Ar-free processes with high GeH_4 content are more promising regarding the adaptability of intrinsic layer stress. A variation of R_{GeH_4} for a constant GeH_4 flow of 150 sccm is investigated in a range of about 50 % to 70 % with the presented test structures shown in Figure 4.26 d.. The intrinsic layer stress of Ar-free SiGe CVD is controllable in a range of about 100 MPa to −100 MPa, if depositions are applied on wafers which are patterned such as described above. The deposition rates vary from about 25 nm/min to 70 nm/min. These rates are for example comparable with literature [153]. Here, any potential incubation time is neglected due to the PECVD SiGe seed layer environment. According to [153], the thickness of a CVD SiGe layer significantly

influences the layer stress. This is because of the different growth mechanisms, which start from island-based growth process and results in vertical grain growth. In the evaluation shown in Figure 4.28 the influence of the layer thickness on the intrinsic layer stress is neglected for two reasons: first, comparable layer thicknesses of about 300 nm to 400 nm are evaluated in this context. Second, the mechanism of island growth is weak or even non-existent for Ar - free CVD of SiGe on a PECVD SiGe seed layer.

From the curves drawn in Figure 4.28 it can be derived that a small tensile layer stress is achieved for a R_{GeH_4} in the range of 50 % to 52 % under the given constant process parameters at 375 °C, a process pressure of 2.67 hPa and for a fixed GeH_4 flow of about 150 sccm. While a process with 52 % was applied to a wafer with a released cavity, a machine defect occurred. Most probably for this reason, the measured stress shows an unexpected deviation.

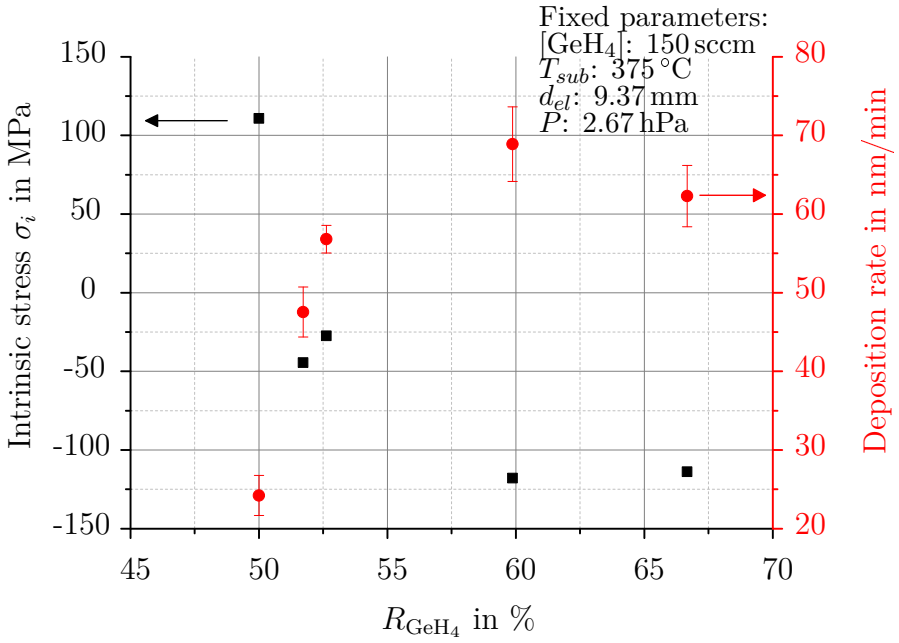


Figure 4.28: Intrinsic stress σ_i and deposition rates of Ar-free CVD SiGe layers shown against R_{GeH_4} for a constant GeH_4 flow of 150 sccm.

In conclusion, the development of a CVD SiGe cover process enables pure SiGe diaphragms, which show some advantages compared to the state of the art sealing. For example, no plasma induced heat is induced, which can cause buckling and induce extra stress. The deflection of covered diaphragms due to intrinsic layer stress becomes controllable. Etch-access channels are filled homogeneously.

This enables an additional etching to reduce the diaphragm thickness and reduce intrinsic stress. Outgassing of any residuals and humidity due to relatively high, but a CMOS-compatible temperature of 375 °C is assumed to be beneficial for the cavity pressure. Because only reactive gases are utilised, the effect of gas trapping should be minimised.
The choice of SiGe CVD process does not completely prevent depositions inside the cavity, but it can be controlled in interesting ways. First, the PECVD SiGe diaphragm with etch-access channels is used as seed layer for the CVD SiGe growth. This situation enables high deposition rates. Second, the process parameters are controlled in such a way that a certain selectivity of the separation is generated. For example, no deposition on SiO_2 surfaces is achieved, while the PECVD SiGe surface shows homogeneous deposition. Additionally, the deposition inside the cavity can significantly be reduced by a) the diameter of etch accesses, and b) the pitch of the etch accesses. The developed side-wall spacer can effectively reduce the etch-access diameters. The pitch can be varied by design.
The most outstanding feature is that pure SiGe diaphragms ideally do not show any CTE mismatches, which can induce additional stress and limit the sensor performance. As presented in Chapter 2.1.4, some of the best options reported so far for post-CMOS compatible sealing of a diaphragm are a SACVD SiO_2 and sputter deposited AlCu [43]. Both show significant disadvantages. There are for example large CTE mismatches with factors of 5 to 10. These technologies requires relatively high layer thicknesses to yield appropriate sealing. This in turn directly affects the sensitivity and, thus, large diaphragm areas might become necessary. Further, metals usually suffer from creep [107]. SiO_2, however, is usually sensitive to humidity, which would require an additional protection layer. Therefore, the presented fabrication scheme of pressure sensor diaphragms can overcome these major challenges of the state-of-the-art in post-CMOS pressure sensor fabrication.

Intermediate Nanoporous ALD Composite for Sacrificial Layer Release and Cover Layer

An alternative option has been developed in order to further minimise any deposition in the cavity and, thereby, increase the diaphragm deflection range. In this thesis, a porous ALD composite layer is exploited as a membrane within the

vertical etch-access channels for the sacrificial layer release etch. The vaporous etch media as well as the etching products are intended to diffuse through this porous ALD composite layer. Because this layer is deposited before sacrificial layer etching, it can minimise any deposition inside the released cavity while the cover process is applied. The desired effect of the porous ALD composite layer (1) regarding the deposition of the cover layer without any deposition inside the cavity is schematically shown in Figure 4.29.

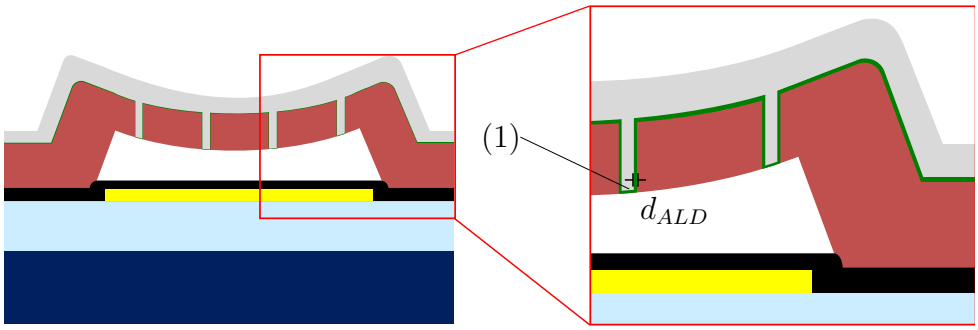


Figure 4.29: Schematic sketch of intermediate porous ALD composite layer with a thickness d_{ALD} integrated in a diaphragm between the in-situ boron-doped PECVD SiGe and CVD SiGe layers. The ALD composite layer is to deposit on a perforated diaphragm before the vapour phase release etch is applied.

The post-CMOS compatible fabrication of such a nanoporous ALD layer is based on a homogeneous composite of two ALD materials, one of which can be selectively etched. Such a composite can be achieved by utilising the principle of island growth. If the number of ALD cycles is held small enough, the touching of neighbouring islands can be prevented [204]. By alternately applying small numbers of ALD cycles for Al_2O_3 and ZnO, a homogeneous composite can be achieved instead of a nanolaminate. Exposing the ALD composite to vapour-phase HF, ZnO particles are selectively etched along the grain boundaries, so that pores are implemented in an etch-resistant Al_2O_3 backbone. The etching of ZnO by HF is significantly different from the etching by HCl, for example. It is observed that HF is more likely to etch weak grain boundaries within the crystal structures and, therefore, is preferred for texture-etching of polycrystalline ZnO [205, 206]. This is exploited for this thesis to realise a porous layer within the etch-access channels. An ALD composite layer comprising of Al_2O_3 and ZnO is deposited just before the sacrificial layer release etch. Here, four cycles

for each oxide have been applied alternately with 30 repetitions at a process temperature of 270 °C. This resulted in composite thicknesses of about 15 nm. Used precursors are trimethylaluminum ($AlMe_3$) and water vapour (H_2O) for Al_2O_3 and diethylzinc (DEZ) and H_2O for ZnO. While exposing the prepared wafer to vapour phase HF first, a texture etching of ZnO creates porosity. By this means the etch-access to the underlying sacrificial layer is enabled. While carrying out the etch process, the sacrificial layer is etched through the resultant ALD composite layer.

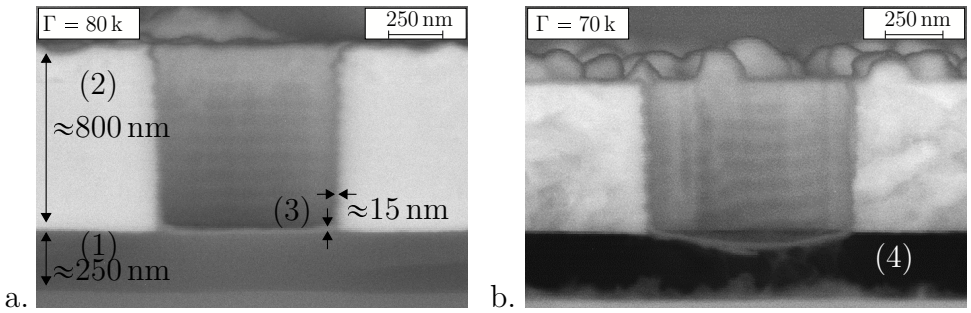


Figure 4.30: SEM cross sections of test structures with a ≈ 250 nm SiO_2 sacrificial layer (1) and a PECVD of ≈ 800 nm SiGe diaphragm layer (2), which are patterned via DRIE and then covered with a thin Al_2O_3:ZnO composite layer (3), are shown a. before and b. after vapour-phase etching. Etch residuals are visible (4).

In Figure 4.30 SEM cross sections are shown before (a.) and after (b.) vapour phase HF/H_2O exposure. Successful in-situ ZnO (3) and sacrificial SiO_2-layer (1) etching is shown, as some remaining residuals of the USG SiO_2 indicate (4). Afterwards, these residuals are completely removed by annealing at 200 °C under vacuum.

The result shown in Figure 4.30 is only the prerequisite to prove the compatibility of an intermediate nanoporous ALD composite in the presented process scheme. Further, the ALD composite layer must not inhibit the growth of a CVD SiGe layer on the PECVD SiGe (2). In Figure 4.31 the results after applying the sacrificial layer release etch and a CVD SiGe-layer (4) are shown. Interferometric inspections show a visible over-etching before (a.) and after (b.) applying the CVD of a SiGe cover layer (4). In (c.) and (d.) it is demonstrated that the CVD is in principle possible on an intermediate nanoporous ALD composite layer. Moreover, the deposition inside the cavity is significantly inhibited. It can be observed that the sacrificial layer (1) is not entirely removed.

This is in line with expectations because the intermediate ALD layer (3) first needs to become porous with the aid of vapour-phase etching, so that an etch-access to the sacrificial layer is granted through the pores. The sacrificial layer release etch in connection with the intermediate ALD composite layer is not examined in more detail. In the shown example, the vapour-phase etching was applied at 10.7 hPa for 12 min. For comparison, a similar test structure without this intermediate ALD composite layer has successfully been etched at 6.7 hPa for 5 min in vapour HF.

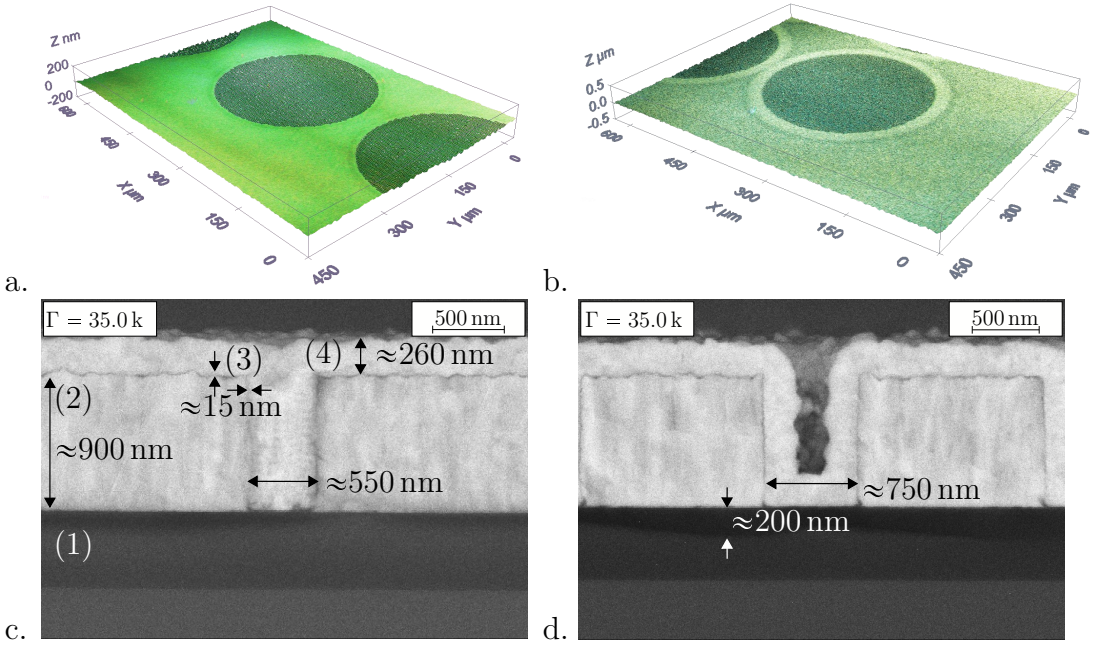


Figure 4.31: Test structures with a SiO_2 sacrificial layer (1) and a PECVD of ≈ 900 nm SiGe diaphragm layer (2), patterned via photoresist and DRIE, equipped with a thin Al_2O_3:ZnO layer (3). Interferometric inspections after release etch show a visible over-etching before (a.) and after (b.) the sacrificial layer release etch and the CVD of a SiGe cover layer (4). SEM cross sections of the etch-access channels with different diameters are shown in c. and d..

It is shown that an additional ALD-composite layer comprising of Al_2O_3 and ZnO (3) can be used successfully as a diffusion layer between a perforated PECVD SiGe diaphragm layer (2) and a sacrificial layer. However, the etching time for diaphragm release is increased by at least a factor of 3.
Further, the application of this additional ALD composite layer does not seem to inhibit the deposition rate of the CVD SiGe (4) for the covering process. As desired, the applied ALD-diffusion layer prevents undesired deposition inside the

cavity, which may lead to increased sensor signals.
The diaphragm characteristics are not further evaluated because of limited machine availability. For this reason, the ALD composite layer is a future option.

4.2.6 Bond Pad Metal Stack

Additional contacts become necessary, if wire bonding is intended to be applied to the top surface of either a stand-alone MEMS or test structures fabricated in the developed post-CMOS technology. For this purpose, additional process steps comprise the opening of the 2nd MEMS wiring level, the deposition of an contact electrode stack comprising 40 nm Ti, 80 nm TiN and a 900 nm AlSi, and finally, the patterning of this stack. The deposition and patterning of the contact electrode stack is inspired by already established technologies at Fraunhofer IMS MST Lab&Fab. Therefore, only a short description is given. In Figure 4.32, SEM cross sections of the edge of an assistance contact pad are shown. In Figure 4.32 a. the designated bond area can be seen in the right half of the image. The shown contact between TiW (1), SiGe (3) is evaluated in Chapter 4.2.3. The overlaying Ti/TiN barrier (4) and AlSi (5) layer as bondable electrode material have been contacted in order to measure the resistance of the corresponding test structures. A slight reduction of the specific resistances is found. In the magnified view shown in Figure 4.32 b. a thin oxide layer is left between the TiW/SiGe contact and the Ti/TiN/AlSi stack.

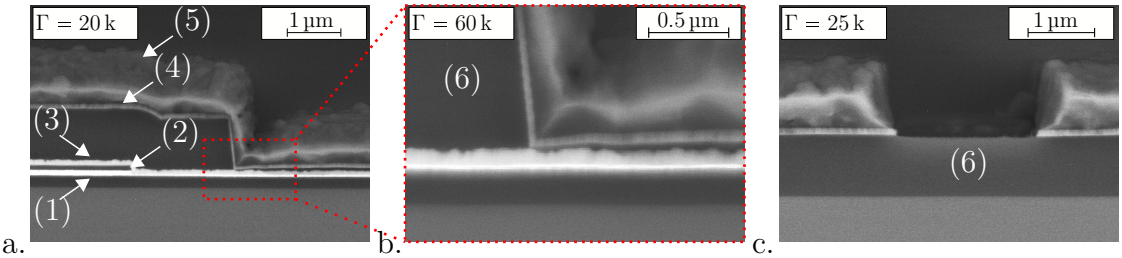


Figure 4.32: SEM cross sections at the edge of an bond pad metal stack comprising a contact between TiW (1), SiGe (3), a Ti/TiN barrier (4) and a AlSi (5) as bondable electrode material (a.). After an oxide etch followed by a sputter pre clean for 9 sec, a thin residual layer remains visible (b.). c. shows that the patterning of the Ti/TiN/AlSi stack perfectly stopped on an intermediate SiO_2 layer (6).

The discussed issue is resolved simply and reliably by increasing the layer

thickness in the PECVD SiGe process from 200 nm to 1 µm. Then, the risks of excessive etching are eliminated and a comfortable step height can be established in order to assure appropriate contacts. The contact between PECVD SiGe and a Ti/TiN/AlSi-stack has been characterised in [42]. It may be worth evaluating a pure SiGe/AlSi connection without Ti/TiN barriers to investigate the creation of a SiGe/AlSi alloy, which could create even stronger bondings. Similar approaches reported the contact of SiGe and AlCu [43, 207, 208].

5 Experimental Verification

In this chapter, the characterisation of pressure sensor related test structures is presented. However, since capacitive sensor elements are not yet fabricated, the following investigations describe diaphragms, which are tested for suitability for the integration into capacitive sensors. One of the major challenges of this thesis is the covering and sealing of released diaphragms. In Chapter 4.2.5, a CVD SiGe process has been developed as an appropriate choice to cover perforated PECVD SiGe diaphragms. Amongst others, the main advantages of a CVD SiGe cover process are: first, the prevention of large CTE mismatches by the single material diaphragm, and second, the avoidance of buckling due to plasma-induced heat in the centre of the diaphragm.
Some of the most interesting questions concern the quality of hermeticity and robustness regarding pressure-related stress impacts of a pure SiGe diaphragm. Investigations of the properties of pure SiGe diaphragms have not been reported until now to the best knowledge of the author. The following experiments comprise He leakage, pressure cycle, overpressure and temperature cycle tests. The chapter concludes with a comparison of the calculated performance compared to some state-of-the-art capacitive pressure sensors.

5.1 Fabrication of SiGe Diaphragms

A schematic and SEM cross sections of test structures are shown in Figure 5.1. A Si substrate (1) is equipped with an 800 nm SiO_2 sacrificial layer (2), upon which the in-situ boron-doped PECVD SiGe layer (3) is deposited. Then, etch-access channels are dry etched by DRIE through a photoresist mask (4) with an accurate etch stop on the SiO_2. Since no side-wall spacer has been applied, the minimal etch-access channel diameters of 500 nm are defined by the mask design. After resist removal by plasma stripping, the sacrificial layer release etch via vapour-

phase HF etching is applied. The etching of the here used test structures must be controlled by time, because the sacrificial layer was not patterned. An annealing process at 200 °C under vacuum is applied afterwards to remove any remaining residuals in the cavity due to the SiO_2 etching. Subsequently, the SiGe cover layer (5) is deposited with R_{GeH_4} of 52 % in a gaseous mixture of only GeH_4 and SiH_4. Further process conditions are 375 °C, a process pressure of 2.67 hPa and a fixed GeH_4 flow of about 150 sccm. These process parameters allow selective deposition and the resulting layer exhibits low stress. The selective deposition is visible inside the covered cavity (6), where no SiGe is deposited at SiO_2 interfaces. The PECVD SiGe diaphragm, however, serves as a seed layer. Unfortunately the stress has become slightly compressive, as shown in Chapter 4.2.5 in Figure 4.28.

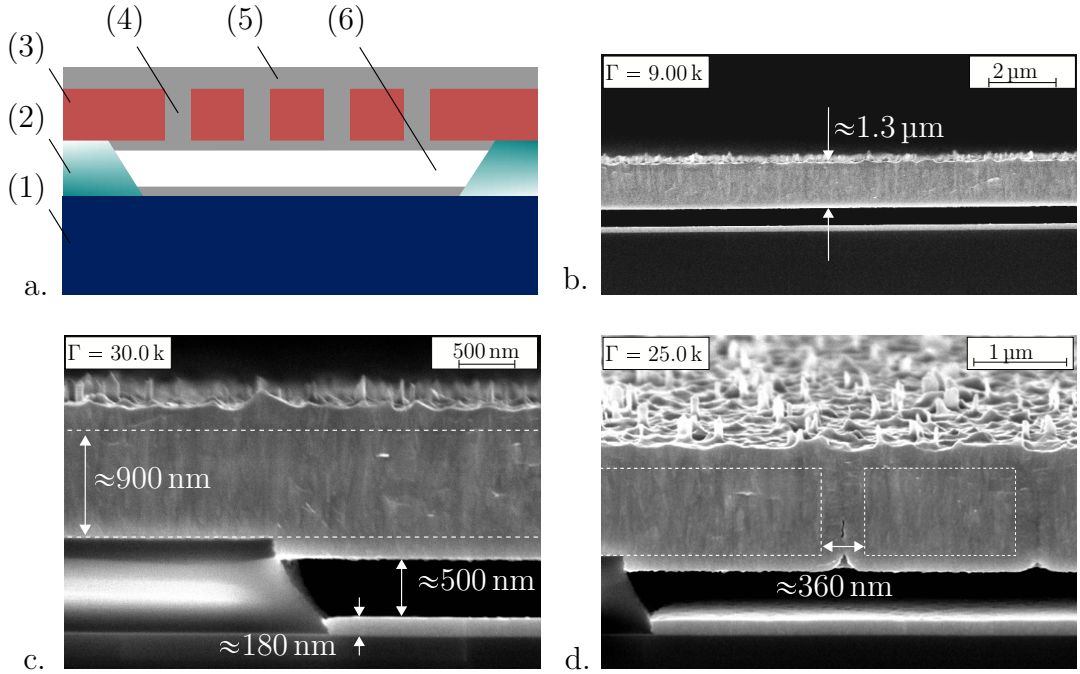


Figure 5.1: a. Schematic sketch of test structures comprising Si substrate (1), an sacrificial oxide layer (2) a patterned PECVD in-situ boron-doped SiGe diaphragm (3) and a selectively deposited CVD SiGe (5) cover layer. SEM cross sections at the centre, b., and an edge of a covered diaphragm, c., show the effects of selective deposition inside the cavity (6). In d. filled etch-access channels are indicated (4).

The fabrication of these test structures is concluded by a chlorine-based RIE process in order to increase the diaphragm sensitivities and reduce the deflection due to intrinsic layer stress. Finally, the diaphragm stack consists of about 900 nm PECVD SiGe, 180 nm CVD SiGe at the bottom side of the diaphragm, and

about 220 nm CVD SiGe on top. Thus, the total layer thickness is 1.3 µm. After etching, elevations remain on the surface. These are possibly grain boundaries of polycrystalline SiGe at which the etching was less effective. However, this side effect of the RIE process step is not further evaluated.
Assuming the etch-access channels are sufficiently closed, no foreign gases are trapped and there is no outgassing inside the cavity, the substrate temperature T_{CVD} of 648 K (375 °C) and the deposition pressure P_{CVD} of 2.67 hPa define the cavity pressure P_{cav} at ambient conditions according to the ideal gas law:

$$P_{cav} \approx P_{CVD} \cdot \frac{T_{ambient}}{T_{CVD}} = 2.67\,\text{hPa} \cdot \frac{298\,\text{K}}{648\,\text{K}} = 1.23\,\text{hPa} \tag{5.1}$$

Because no CTE mismatch is assumed, the impact of the linear extension of the materials regarding the volume of the cavity, is considered to be small and, thus, neglected. The contribution of a common CTE in the order of 10^{-6}/K is assumed to be negligibly small compared to the volume change due to the difference between the cavity pressure and the ambient pressure.
Further, the gases for the CVD SiGe process are GeH_4 and SiH_4. Due to the high reactivity of the CVD process described in chapter 4.2.5, it can be assumed that both gaseous reactants are entirely consumed once the etch-access channels are completely closed. This means that the amount of trapped gas could further be reduced and thus, the cavity pressure P_{cav} is most likely lower than 1.23 hPa, as estimated in Equation 5.1. The main characteristics of the fabricated test structures are summarised in Table 5.1.

Further, it is ensured that the buckling of the diaphragms is almost exclu-

Table 5.1: Characteristics of fabricated test structures.

Indication	Symbol	Value	Unit	Comment
Diaphragm thickness	t_{dia}	1.3	µm	-
Diaphragm diameters	$2r_0$	100, 150 and 300	µm	200 µm N/A
Etch-access channel diameter	d_{ae}	500	nm	nominal
Remaining cavity height	h_{cav}	500	nm	-
Max. applied process temperature	T_{CVD}	375	°C	-
CVD gas ratio	R_{GeH_4}	52	%	compressive stress
Cavity pressure	P_{cav}	⩽1.23	hPa	-

sively caused by layer stress and not by other effects such as outgassing. Finally,

the buckling is observed even if a complete closure has not yet been reached. In addition, the deflection of the diaphragm decreased after having applied a chlorine-based RIE process in order to reduce the thickness of the CVD sealing layer. For example, the deflection under atmospheric pressure of a diaphragm with a diameter of 100 µm is reduced by about 300 nm after a reduction of the CVD SiGe layer thickness by about 250 nm.
From this it can be concluded that the stress-induced diaphragm deflection can significantly be reduced by the planned use of the side-wall spacer technology, which has been developed in Chapter 4.2.3. This technology has not yet been used in the subsequently analysed test structures.

5.2 Optical Evaluation of Diaphragm Characteristics

As the realised pressure sensitive test structures are not yet equipped with electrical interfaces, the optical characterisation is one of the remaining methods to investigate the properties of the diaphragms. In principle, the diaphragm deflection can be measured with the method of phase shift interferometry with a high vertical resolution down to 0.1 nm [209]. A *Photomap* $3D$ system provided by *Fogale nanotech* is used in this thesis. It is equipped with an environmental chamber to vary the applied pressure between vacuum and up to 2000 hPa. This enables the diaphragm investigation as a function of the applied pressure. The setup of the optical interferometer relies on the measurement principle of the Michelson interferometer.
The shape of a surface, e.g. the deflection of a diaphragm, is expressed at any point on the surface by $z(x, y)$:

$$z(x, y) = \frac{\lambda}{2} N(x, y), \tag{5.2}$$

where $N(x, y)$ is the order of the fringes at a point (x, y) and λ is the wavelength of the monochromatic light which is obtained by filtering the white light. The measurement system limits the maximum step height measurements to about 130 nm. Usually, this is not an issue for smooth shapes as for example diaphragm shapes. The vertical measurement range is limited to about 20 µm due to the fringe visibility. In Figure 5.2 a. a diaphragm with a diameter of 300 µm shows

the corresponding interferogram under atmospheric pressure. Within the range of fringe visibility, a defined number of images (usually 32 or even 64) is integrated into the phase shift algorithm on each measurement step [210, 211].
This method is applied by an automatic interference pattern analysis because the investigated area is free of any sharp borders or structures, thus the deflection of diaphragm surfaces varies smoothly. The unwrapping of this phase map (Figure 5.2 b.) results in a fractional interference pattern with high fidelity at every point, as shown in Figure 5.2 c.. These data are used to generate a 3D figure and a cross sectional profile over the diaphragm diameter, as shown in Figure 5.2 d. and e..

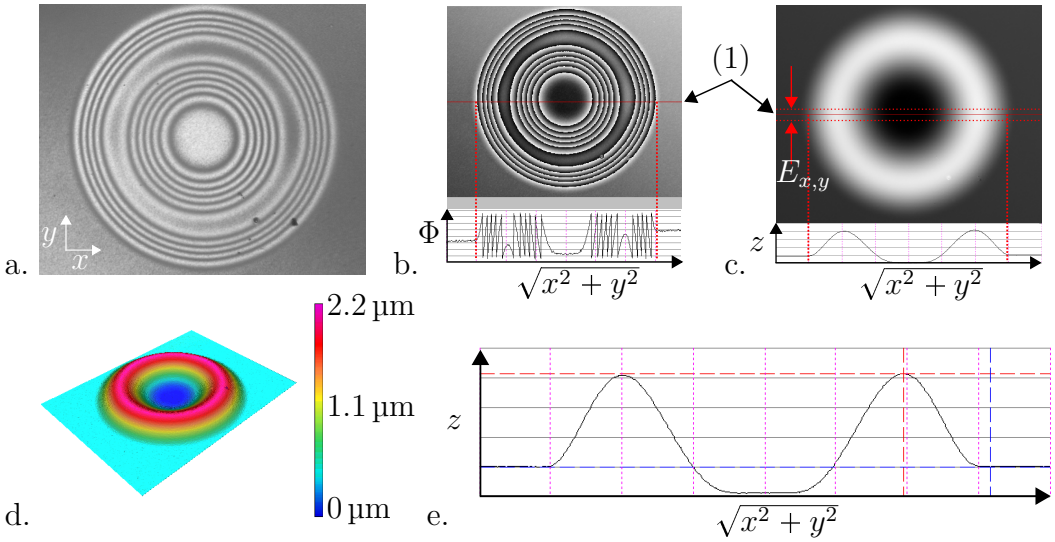


Figure 5.2: Test method: a. Camera view on the interferogram due to the surface profile of a diaphragm under applied pressure, b. wrapped phase, which is then unwrapped to a topographic map c.. This contains the $z(x, y)$ information, which is plotted as a 3D figure in d. and as a profile along the intersection line (1) in e..

Some sources of measurement errors E must be taken into consideration. They are discussed with the help of Figure 5.2. First, the measurements are temperature stabilised by the climate control of the laboratory, generating a deviation of $\approx \pm 2.5\,\mathrm{K}$. Even though the temperature sensitivity in terms of deflection is unknown so far, reported values [183] are considered to estimate the impact. Thus, temperature variations are assumed to result in an equivalent pressure change in a range of 3 hPa/K to 5 hPa/K.
Further, the cross section line through the centre of an individual diaphragm is drawn manually. As presented before, the layer stress in the diaphragms of

the realised test structures is unfortunately compressive resulting in an upturned paraboloid shape. Depending on the applied pressure, mainly two different diaphragm shapes are of importance:

- An upturned paraboloid if the applied pressure is too small to overcome the restoring force of the diaphragm.
- A diaphragm with torus-like turning points close to the diaphragm edges if the applied pressure is higher than the restoring force of the diaphragm.

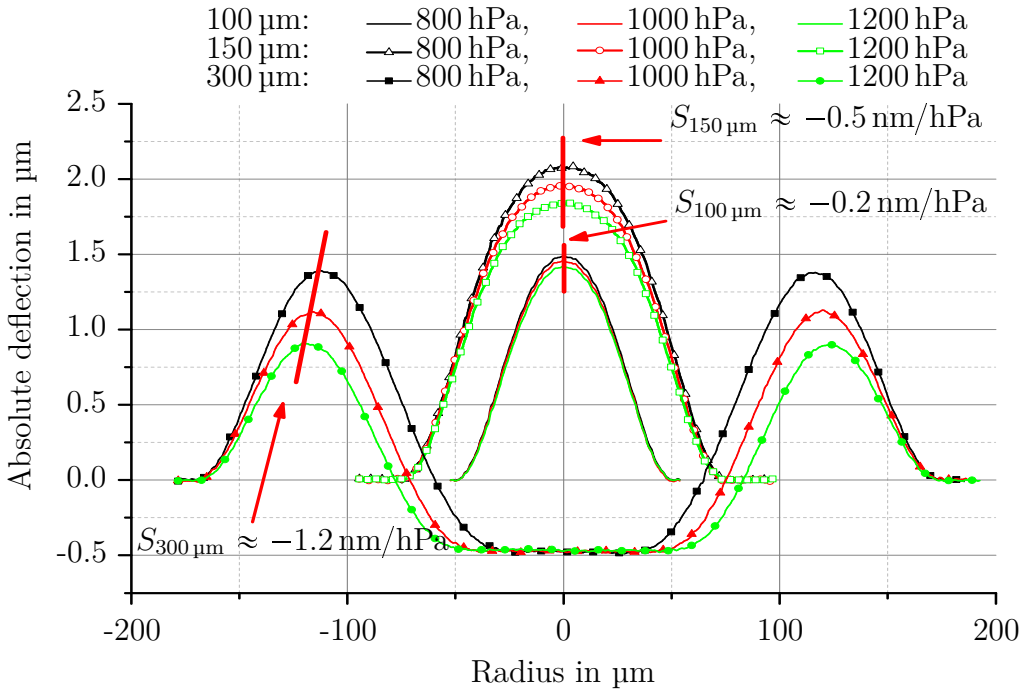


Figure 5.3: Determination of mechanical sensitivities of pressure sensitive test structures with diameters of 100 µm, 150 µm and 300 µm.

These examples demonstrate different impacts of the x-y error. If one desires to detect the maximum of a paraboloid, a small deviation in X or Y can cause large errors in Z, especially if the paraboloid shows a steep slope. In this case, the repeatability showed errors of up to 35 nm for 100 µm diaphragms. Diaphragms with a diameter of 300 µm obtain a slightly reduced error, since the probability of identifying the maxima is increased. For these diaphragms the cumulated error is about 20 nm.

The fabricated diaphragms with a diameter of 300 µm show the highest sensitivity, so these become very interesting for the operation in contact mode. Despite

the originally upturned shape of the diaphragm due to intrinsic stress, very large capacitive signals become possible. As described before, a large area of the diaphragm is deflected to the minimum distance to the bottom capacitor plate. Further, the C-P characteristics become highly linear in the contact mode. The most interesting questions for this operation mode are the pressure hysteresis and burst pressure stability with respect to the high sensitivity. In Figure 5.4 the characteristics of the diaphragm deflection lines are drawn for a pressure range from 10 hPa to 1920 hPa. The point when the diaphragm touches the cavity bottom is called CPP. At this point, the diaphragm does not further deflect, but the diaphragm contact area increases. In the given example, the CPP is at about 500 hPa.

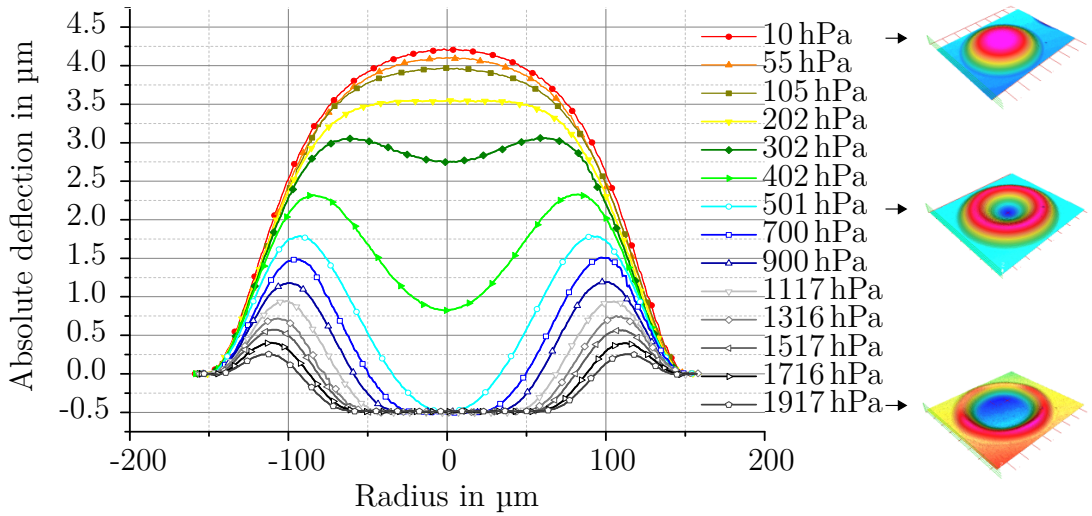


Figure 5.4: Pressure sensitivity of patterned SiGe test structures with a diaphragm diameter of 300 µm covered by 500 nm CVD SiGe, which is subsequently reduced by about 250 nm due to chlorine-based RIE.

In Table 5.2 the sensitivities in non-contact mode of 100 µm, 150 µm and 300 µm diaphragms obtained by the measurements shown in Figure 5.3 and Figure 5.4 are compared to calculated expected values due to Equation 2.5 and Equation 2.6 introduced in Chapter 2.1.3. Deviations between the modelled and measured sensitivities in non-contact mode in a range from about 30 % to 70 % can be calculated. The deviations are probably due to two reasons. The sensitivities for 100 µm and 150 µm are obtained in a range near the absolute maximum deflection, which means saturation. It can be assumed that applying higher pressures will yield increased sensitivities and, thus, improve the match with the

Table 5.2: Comparison between modelled and measured mechanical sensitivity S of 100 µm, 150 µm and 300 µm diaphragms. Used parameters for the calculation are: $t = 1.3\,\mu m$, $E = 149\,GPa$, $\nu = 0.25$.

Diameter	100 µm	150 µm	300 µm
S measured in nm/hPa	≈0.2	≈0.5	≈13.9
$<S$ modelled in nm/hPa	0.3	1.7	27
Deviation in %	33	71	48

model. The sensitivity of diaphragms with a diameter of 300 µm, however, is not obtained close to the saturation due to applied pressures up to and including the CPP. Nevertheless, a deviation of about 50 % is obtained. This can be explained by the shape of the deflection lines, which include turning points. These are also dependent on the pressure. Therefore, it can be assumed that the buckling of the diaphragms lead to the observed deviations between model and measurement.

5.3 Hermeticity of the CVD SiGe Cover

An interesting question is whether the CVD SiGe layer yields a hermetic and robust covering of the cavity. Any defect in the cover layer will cause leaks. Conventionally, leak tests are divided into gross and fine leak tests. Different methods have to be applied to detect large or small leaks. A summary of known methods can be found in [212]. There are two standards to classify leak rates as listed in Table 5.3 [213, 214]: Noble gasses, as e.g. Ne or He are suitable for leak

Table 5.3: Classification of leak rates in $Pa\,m^3/s$, after [215].

Class	Ultra-Fine	Super-Fine	Extra-Fine	Fine	Moderate	Gross
$Pa\,m^3/s$	$<10^{-14}$	10^{-14} to 10^{-11}	10^{-11} to 10^{-9}	10^{-9} to 10^{-7}	10^{-7} to 10^{-5}	$>10^{-5}$

detection, because they are not absorbed by any getter material [215] and are chemically inert. Therefore, the determination of the He leak will show whether there is a leak with molecular or even viscous flow, or whether diffusion becomes dominant. Here, the permeation by He does not indicate a leak. Care must be taken to understand the level of permeation to prevent misinterpretation of results. Similarly, some materials may absorb helium and yield false results when

tested. It is reported that He can diffuse through semiconductor materials such as Si and SiGe [216].
Considering that the partial pressure of He in atmospheric conditions only amounts to 0.5 Pa, the hermeticity of a sealing layer against He can be neglected for MEMS, which are exposed to atmospheric conditions [217]. In turn, for completely gas-independent pressure sensors, the He tightness can also become important.
The basics of leak measurements based on the ideal gas law are:

$$P \cdot V = N k_B T \Longleftrightarrow P = n k_B T = \tilde{n} R T, \tag{5.3}$$

where P (Pa) is the pressure inside a volume V (m^3), N (1) is the number of gas molecules inside the cavity, n ($1/m^3$) is the particle density, $\tilde{n}$ (mol/m^3) is the molecular particle density, T (K) is the temperature, k_B (J/K) is the Boltzmann constant, and R (J/(mol K)) is the molar gas constant.
The time derivative of the general gas equation denotes the measurable leak rate q_{leak} (Pa m^3/s) for a given cavity volume assumed to be constant, here V_{cav}:

$$q_{leak} = \frac{\delta P_{cav}}{\delta t} V_{cav} \tag{5.4}$$

where δP_{cav} is the change of the pressure inside the cavity. The leak rate q_{leak} represents a gas flow into the cavity, which is usually described as a linear function of the pressure difference between the pressures outside and inside the cavity, P_{cav}. The applied pressure outside the cavity is called bombing pressure P_b.

$$q_{leak} = L \cdot (P_b - P_{cav}) \tag{5.5}$$

where the proportional factor L is labelled as flow conductance, which describes the flow rate under a pressure gradient.
According to [215, 218], the cavity pressure P_{cav} between the bombing pressure P_b and the initial cavity pressure $P_{cav,i}$ as a function of the time t_b is yielded by the help of Equation 5.4 and Equation 5.5:

$$\begin{aligned} P_{cav}(t_b) &= P_b - (P_b - P_{cav,i}) e^{\left(\frac{-L}{V_{cav}} t_b\right)} \\ \Rightarrow L &= -\frac{V_{cav}}{t_b} \ln\left(\frac{P_b - P_{cav}(t_b)}{P_b - P_{cav,i}}\right) \end{aligned} \tag{5.6}$$

Under the assumption that the difference between the applied bombing pressure P_b and the cavity pressure P_{cav} is much larger than the pressure increase in the

cavity, $\delta P_{cav}(t_b)$, Equation 5.6 can be approximated by:

$$\delta P_{cav}(t_b) \approx \frac{L}{V_{cav}} \cdot t_b \cdot P_b \tag{5.7}$$

The leak rates for an individual gas can be used to derive the leak rates for other gases. If molecular flow can be assumed, the following equation is used to calculate the molecular flow conductivity L_g, which depends on temperature T and the molecular mass M of the tracer gas [215]:

$$L_g = L_{\mathrm{He}} \cdot \sqrt{\frac{M_{\mathrm{He}}}{M_g} \cdot \frac{T_g}{T_{\mathrm{He}}}} \tag{5.8}$$

In Table 5.4 the properties and conversion factors of ambient gases are summarised [219], where the molecular weight for air is calculated based on the partial pressures of the air components: For defect-free test structures, the path of a gas

Table 5.4: Properties of some molecular species after [219].

Gas	molecular weight in g/mol	Diameter in nm	L_g/L_{He}
He	4.0	0.22	1.00
O_2	32.0	0.36	0.354
N_2	28.0	0.38	0.378
CO_2	44	0.46	0.301
Air	28.7	0.37	0.373

through the diaphragm is due to permeation through a solid. This is a two-phase process, which first concerns adsorption of the gas at the surface and, second, the diffusion. The diffusion rate can depend on the non-perfect density of the solid due to internal porous structures, the space between grain boundaries or the number and size of grains. The transport of a gas through a material depends on the gas permeability of the solid (material property), the difference in the potential (e.g. pressure gradient), the thickness of the solid material (geometric property) and the exposed area (geometric property). Then, the gas permeability coefficient K correlates directly with the gas flow rate through a solid with a specific area per applied pressure. In literature, K can be found either as mass,

volume, or molar permeability [220]:

$$\begin{aligned} K_m &= \frac{\dot{q} \cdot t_{dia}}{\Delta p \cdot A_{dia}} && \text{kg/(s Pa m)} \\ K_V &= \frac{\dot{V}_{cav} \cdot t_{dia}}{\Delta p \cdot A_{dia}} && \text{m}^3\text{/(s Pa m)} \\ K_{mol} &= \frac{\dot{n}_{cav} \cdot t_{dia}}{\Delta p \cdot A_{dia}} && \text{mol/(s Pa m)} \end{aligned} \tag{5.9}$$

The volume permeability coefficients of gases for different material classes are roughly divided as listed in Table 5.5 [219]:

Table 5.5: Classification of volume permeability coefficients of gases for different materials after [219].

Material class	Polymers	Glasses / Ceramics	Metals / Semiconductors
$\text{m}^3/(\text{s Pa m})$	10^{-17} to 10^{-11}	10^{-19} to 10^{-17}	10^{-22} to 10^{-20}

5.3.1 Optical Leak Testing

The optical leak testing method allows measuring very fine pressure changes at a high total pressure [218, 221–225]. The method uses interferometry to measure the pressure driven deflection of a diaphragm. By monitoring this deflection over time, the leak rate can be determined. If the sealed diaphragm contains a fine leak or if diffusion occurs, the deflection will decrease over time until the pressure inside and outside the cavity is equal. This principle is drawn in Figure 5.5:

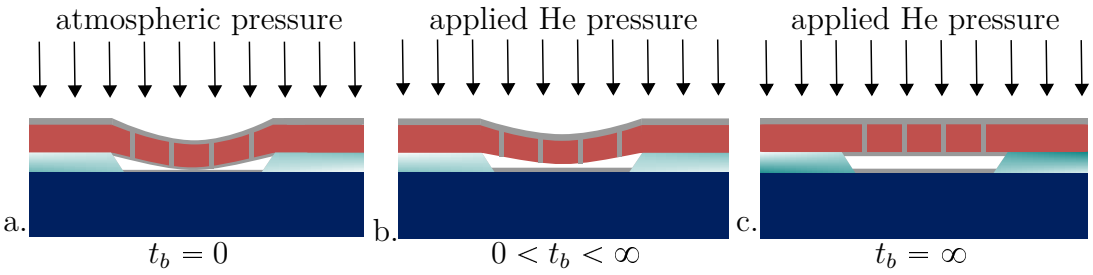


Figure 5.5: Schematic cross section of a test structure in He leak test: a. represents the test structure after calibration at $t_b = 0$ under ambient condition, b. while He bombing is applied and $P_{cav} < P_b$, and c. at equilibrium, when $P_{cav} = P_b$.

For MEMS packaging structures, the reported detectable leak rate is about $10^{-11}\,\text{Pa m}^3/\text{s}$ [212, 221]. Pressure-sensitive structures show significantly higher

sensitivities and allow a much more precise leak detection using commercially available optical systems that are capable of detecting nanometre changes. MEMS in-situ test structures such as a micro pirani gauge [221] or capacitive deflection structures [226] have been developed for this purpose. Thereby, the detection of ultra low leak rates down to $10^{-16}\,\mathrm{Pa\,m^3/s}$ is reported.

5.3.2 Results of He Leak Tests through CVD SiGe Cover

He 5.0 gas (purity of 99.999 %) is used to detect any diffusion inside the diaphragm cavity. Most likely permeation paths are either CVD-SiGe etch-access fillings or any defects. Also possible is the diffusion through oxide at the edges of the tested samples. The experiments are performed with a quarter of a 200 mm wafer, on which the evaluated test structures are unevenly distributed. The distances of the investigated positions to the edges, where an access to the oxide is given, range from some mm to some cm. The possibility that diffusion into the cavity is dominated primarily by the further path through the oxide is therefore neglected. The exposure He is also referred to as bombing. At room temperature, the He bombing is applied to the diaphragm when they are stored in the environmental chamber of the interferometer. Then measurement can be carried out directly in the gas. If, the He bombing is carried out under elevated temperatures, the sample is stored in a separate pressure bomb made of aluminium, which is located on a heating plate. For both setups an evacuation of the vessels is applied for at least 5 min, before He is introduced. In the case of He bombing under an elevated temperature, the dwelling times after release are hold in the range of a few minutes. Therefore, the settings of the interferometer are not changed between the measurement times and the diaphragms are measured directly after release from the He exposure. Due to the good heat conduction properties of silicon (substrate) and aluminium (sample holder), a temperature influence on the shape of the diaphragm is assumed to be negligible.

Reference Measurements before He Exposure

The investigated diaphragms are characterised before any He exposure. The characteristic of one diaphragm is shown in Figure 5.6.

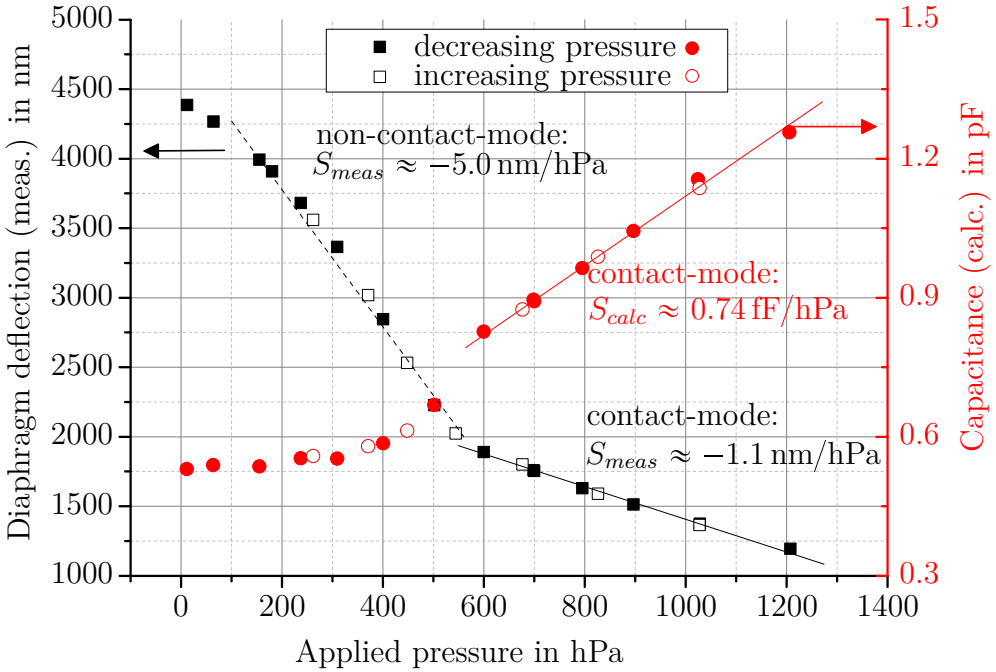


Figure 5.6: Pressure dependent characteristics of one single diaphragm with a diameter of 300 µm evaluated before He diffusion experiments.

The measured deflections in dependency of the applied pressure in a range of 5 hPa to 1200 hPa at 23±3 °C refer to the left Y-axis. Here, the maximum deflection point is measured. However, the data which refer to the right Y-axis show capacitances. These are calculated by integration over the deflection lines through the centre of a diaphragm according to Equation 2.7. Further, the capacitances are determined assuming a minimal distance between the virtual capacitor plates of 300 nm, which is in agreement to the CVD SiGe layers inside the cavity shown in Figure 5.1. As described before, there are two operation modes in the applied pressure range: contact and non-contact. In order to determine any impacts due to He permeation into the cavity, the following characteristics are evaluated:

- Shifts of the CPPs
- Deviation of the calculated capacitance at atmospheric pressure based on the deflection line

It is assumed that the diaphragm sensitivity remains unaffected because no chemical reaction is expected due to the inertness of He. The obtained data before He exposure are therefore used as reference, to which the change in cavity pressure

can be referred, and the calculated capacitances can directly be compared.
In Table 5.6 the sensitivities within these modes are summarised for 5 evaluated diaphragms. From the deviation of the calculated capacitive sensitivity of about 7 % it can be seen that the 5 diaphragms from different wafer positions have comparable characteristics. The arithmetic mean of the calculated capacitive sensitivities is about 0.75 fF/hPa.

Table 5.6: Summarised sensitivities S in contact mode of 5 diaphragms with diameters of 300 µm used for He gas permeability tests.

Diaphragm	$S_{meas.}$ in nm/hPa	$S_{calc.}$ in fF/hPa	R^2 in %	Mean $S_{calc.}$ in fF/hPa	1σ error in %
1	-1.106	0.721	99.9		
2	-1.110	0.830	99.6		
3	-1.172	0.675	99.7	0.753	7.1
4	-1.124	0.750	99.7		
5	-1.120	0.789	99.9		

Shift of Contact Pressure Point

The partial pressure of He inside the cavity can be identified by determining the shift of the CPP. As a consequence of the He diffusion, the pressure in the cavity has increased while the DUT is exposed to the He bombing. In Figure 5.6, the pressure dependent diaphragm deflection characteristic is shown before He exposure is applied. The same diaphragm is evaluated again in order to determine the shift of the CPP, which represents the He partial pressure inside the cavity, namely ΔP_{cav}. The CPP can be evaluated as the intersection of the linear regression lines for the contact and non-contact operation modes, as shown in Figure 5.7. The linear equation systems are solved for the contact pressure of both the pre and the post measurements. The difference between both is assumed to be equal to the partial pressure of the diffused He. These coefficients, the coefficients of determination R^2, and the results for the CPPs are listed in Table 5.7. By this method the shift results in a ΔP_{cav} of about 112 hPa. A major disadvantage of this method is the large number of measurements, which are necessary for identifying reliable linear regressions in contact and in non-contact mode. If more devices are included, the dwelling time is significantly increased. The dwelling time at atmospheric conditions causes an exponential decay of the

He partial pressure inside the cavity. Thus, the dwelling time should be held at a minimum. For this reason, even though a significant shift of the CPP can be identified, it is not useful to calculate any leak rates by changes in cavity pressure obtained by this method.

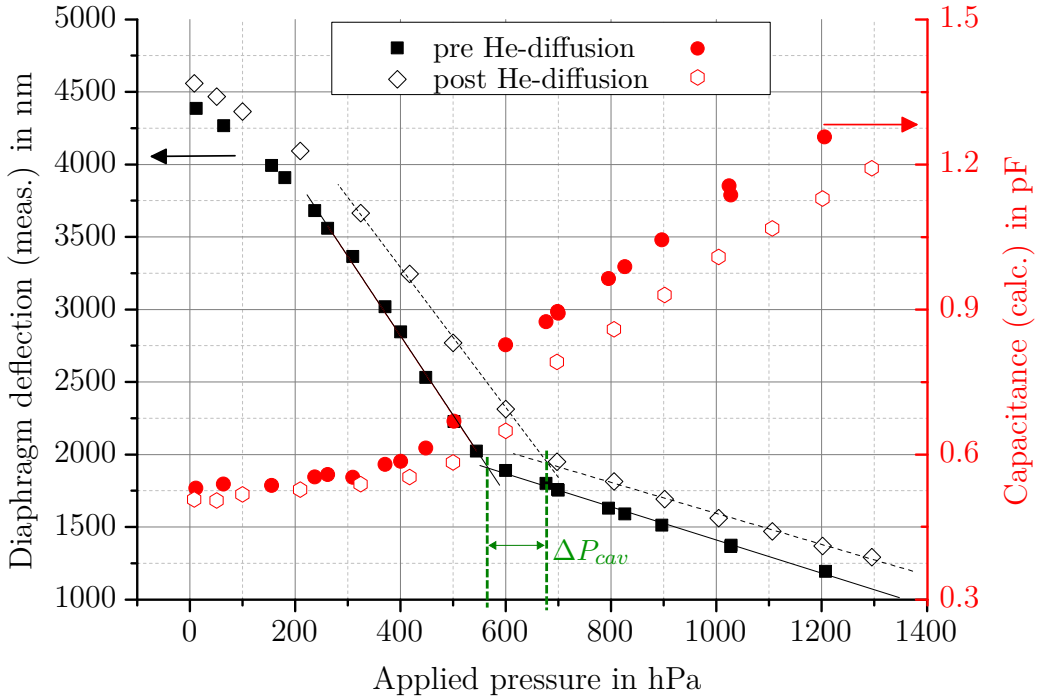


Figure 5.7: Shift of the CPP of a diaphragm with a diameter of 300 µm due to He leak tests.

Table 5.7: Determination of ΔP_{cav} by the aid of linear regression, described as $y = a \cdot x + b$, to describe the sensitivities of one single diaphragm with a diameter of 300 µm in contact and non-contact mode, evaluated before and after He diffusion experiments (see Figure 5.7).

	modus	a in nm/hPa	b in nm	R^2 in %	CPP in hPa	ΔP_{cav} in hPa
pre	non-contact	-5.970	5224.3	99.9	556.5	111.5
	contact	-1.114	2521.9	99.6		
post	non-contact	-4.994	5298.4	99.8	668.0	
	contact	-1.105	2700.5	99.4		

Variation of Deflection Line Integrals due to He Permeation

A more efficient way to hold the dwelling time to a minimum, is to only measure deflection lines at atmospheric pressure in order to determine the change of the

cavity pressure due to He bombing. This requires notably fewer measurement points. With the aid of the reference functions obtained before the He bombing at 1424 hPa was started, the deviation can easily be calculated by measuring the diaphragm deflection at a single pressure point. Here, the dwelling time is held less than 10 min. The calculated change of the capacitances for 5 diaphragms with a diameter of 300 µm are presented in Figure 5.8. The relative change of calculated capacitances is drawn over the applied He exposure time t_b at P_b of 1424 hPa.

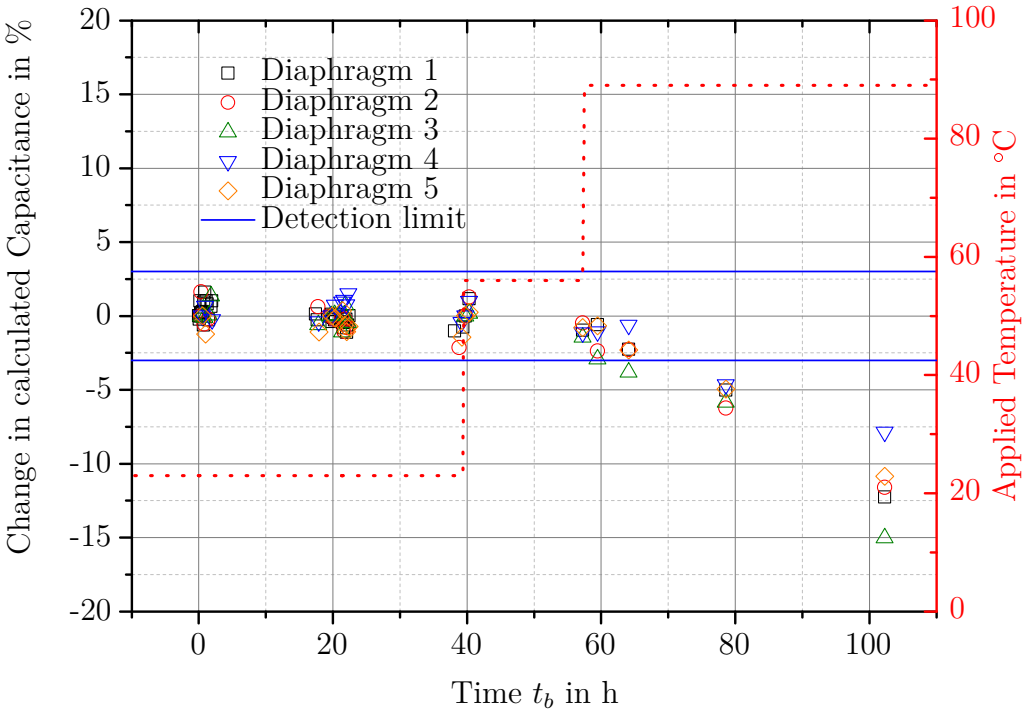


Figure 5.8: Measurement results of relative change of calculated capacitances at ambient conditions of 5 diaphragms with a diameter of 300 µm with respect to the calibrated capacitance-to-pressure functions in dependency of the bombing time t_b. A He partial pressure of 1424 hPa is applied at different temperatures, the dwelling time t_d is 10 min.

Note that three different temperature ranges are applied for the He bombing. After about 40 h the temperature is increased from 23 °C to at least 56 °C and, finally, at least 89 °C is applied. An increase of the He bombing temperature is applied due to the ultra-fine leak rates, which are definitely lower than the detection limit. The detection limit in terms of pressure is evaluated to be around 35 hPa, based on the cumulated errors due to reproducibility, accuracy of applied

pressures and pressure measurements, and temperature-related impacts on the diaphragms.

Within about 40 h at 23 °C, no change of the calculated capacitance with respect to the detection limit is observed. The increment of the temperature to 56 °C for about 18 h and to 89 °C for about 45 h causes significant changes of the diaphragm deflection lines. With respect to the reference data obtained before He bombing was applied, the change of the cavity pressure is calculated for all the measurement data. This is plotted in Figure 5.9.

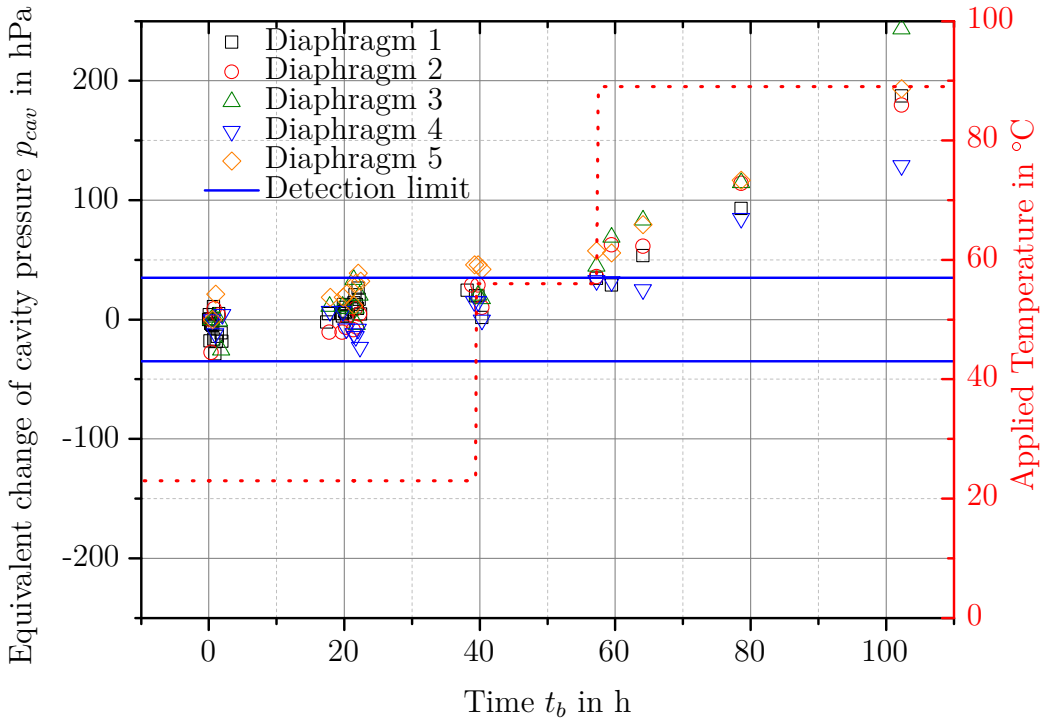


Figure 5.9: Measurement results of relative change of the cavity pressure P_{cav} at ambient conditions of 5 diaphragms with a diameter of 300 µm with respect to the calibrated capacitance-pressure functions in dependency of the bombing time t_b. The He partial pressure of 1424 hPa is applied at different temperatures, the dwelling time t_d is 10 min.

The changes of the cavity pressures shown in Figure 5.9 and an average volume V_{cav} of $1.3 \times 10^{-14}\,\mathrm{m}^3$ are used for the following calculations using Equation 5.4. Here, the maximum leak rate averages $4.5 \times 10^{-16}\,\mathrm{Pa\,m^3/s}$, which is less reliable, since the observed changes of the signals do not exceed the detection limits. Moreover, the true leak rate can be much smaller at 23 °C. In the 89 °C

period, however, the leak rates can be determined to $1.2 \times 10^{-15}\,\mathrm{Pa\,m^3/s}$. Here, a reliable increase can be determined, thus, the detection limit is exceeded. For the diaphragm geometries evaluated here, a detection limit of about $5\,\mathrm{Pa\,m^3/s}$ can be assumed. The calculated leak rates are drawn in Figure 5.10.

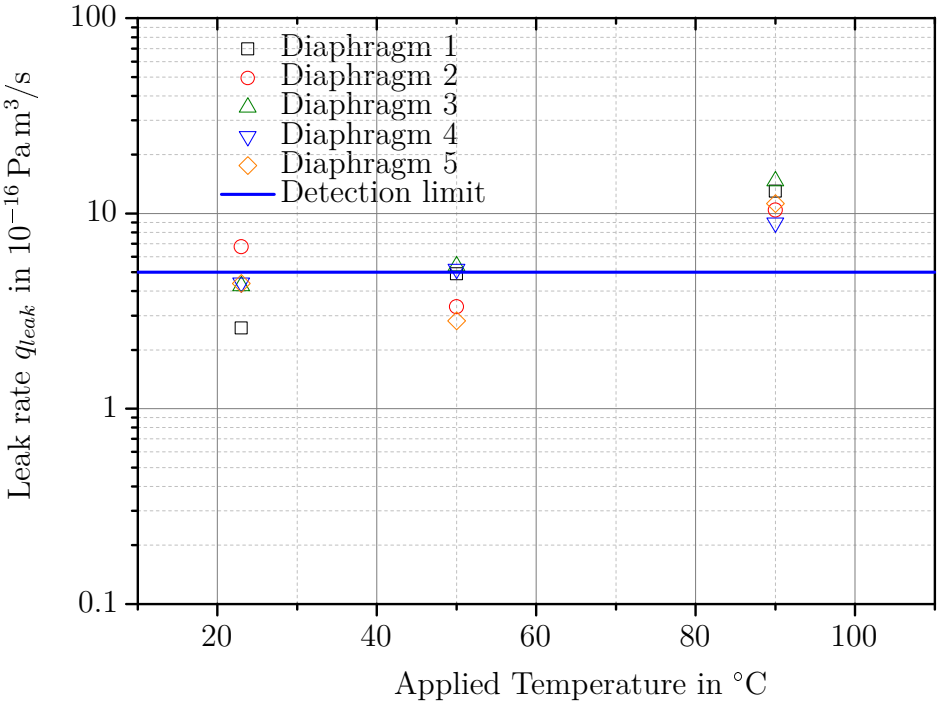


Figure 5.10: Determined leak rates q_{leak} over the applied temperatures while He bombing at 1424 hPa was applied.

Diffusion experiments to characterise highly pressure-sensitive MEMS structures are hardly reported in literature. A related report [190, 227] evaluated the diffusion of He, N_2 or H_2 through pressure sensor diaphragms made of 1.5 µm poly-Si and compared different sealing layer properties. Results for a SiO_2 (2 % PSG) and a 200 nm LPCVD Si_3N_4 sealing layer can be considered. While the SiO_2 layer represents incompatible hermeticity properties, the sealing by the LPCVD Si_3N_4 represents the state-of-the-art sealing of a monolithically integrated capacitive pressure sensor technology fabricated at IMS, see [37, 51, 64, 191], which is an approved technology.
Further, the hermeticity results from the post-CMOS SiGe diaphragm developments by IMEC (introduced in Chapter 2.1.4, compare for example Figure 2.7 on page 29) are used as comparative values [43, 72].

The results are compared to the above-mentioned literature in Table 5.8. Here, the leak rates Q_{leak} of selected gas-solid combinations are compared with SiGe-diaphragm results fabricated in this thesis. The results should be treated with some caution because the leak rates are obtained by different methods, namely by flow measurements through the diaphragm [227], or bombing under air and laboratory conditions [43]. For reasons of comparability, the determined leak rates

Table 5.8: Leak rates Q_{leak} of selected gas-solid combinations compared with SiGe-diaphragm results (mean of 5 diaphragms).

Gas-solid combination	Q_{leak} at 23 °C in Pa m^3/s	Q_{leak} at 56 °C in Pa m^3/s	Q_{leak} at 89 °C in Pa m^3/s	Reference
He-SiO_2(PSG)	3.6×10^{-10}	7.4×10^{-10}	1.6×10^{-9}	[227]
He-Si_3N_4 on poly-Si	-	-	1.8×10^{-15}	[227]
Air-SACVD SiO_2 on SiGe	1.0×10^{-16}	-	-	[43]
Air-AlCu on SiGe	5.5×10^{-16}	-	-	[43]
He-SiGe (PECVD+CVD)	4.5×10^{-16}	4.3×10^{-16}	1.2×10^{-15}	present

presented before are used to calculate material specific gas permeability coefficients according to Equation 5.9 for a normalised pressure difference of 1013 hPa. In Table 5.9 the gas permeabilities κ of selected gas-solid combinations are listed.

Table 5.9: Gas permeabilities κ of selected gas-solid combinations compared with SiGe-diaphragm results (mean of 5 diaphragms), after [219].

Gas-solid combination	κ at about 23 °C in m^2/s	κ between 89 °C to 100 °C in m^2/s	Reference	Comment
He-SiO_2 (Quartz)	1.0×10^{-13}	4.2×10^{-13}	[228]	
He-7740 Glass	8.5×10^{-15}	7×10^{-14}	[229, 230]	Material
He-1720 Glass	1.5×10^{-19}	1.0×10^{-17}	[230]	analysis
He-96 %Al	3.0×10^{-20}	2.0×10^{-18}	[219]	
He-SiO_2 (2 % PSG) on polySi	9.1×10^{-14}	4.1×10^{-13}	[227]	MEMS
He-LPCVD Si_3N_4 on polySi	-	4.5×10^{-19}	[227]	pressure
Air-SACVD SiO_2 on SiGe	9.9×10^{-21}	-	[109]	sensor
Air-AlCu on SiGe	3.3×10^{-20}	-	[109]	diaphragms
He-SiGe (PECVD+CVD)	$\approx 7.9 \times 10^{-20}$	$\approx 2.4 \times 10^{-19}$	present	

Results and Discussion of Hermeticity Experiments

A thin-film CVD SiGe cover to seal perforated PECVD SiGe diaphragms with diameters of 300 µm and a total thickness of 1.3 µm has been investigated regarding hermeticity. The variation of the deflection lines due to He permeation was investigated. The determined leak rates vary in dependency of the applied temperature from $4 \times 10^{-16}\,\mathrm{Pa\,m^3/s}$ to $1 \times 10^{-15}\,\mathrm{Pa\,m^3/s}$ and thus, can be classified as ultra-fine leaks (compare Table 5.8 or [215]). The obtained He gas permeability coefficients confirmed that the diaphragms can be treated as a pure SiGe layer. The He gas permeability of a diaphragm stack comprising PECVD and CVD SiGe is in the range which can be expected for metals and semiconductors (compare Table 5.5 or [219]).
Recent developments evaluated SACVD SiO_2 with a thickness of 0.9 µm and sputter-deposited AlCu with a thickness of 1.5 µm on a PECVD SiGe layer with a thickness of 3.5 µm [109]. The corresponding He gas permeabilities of the sealing layers were estimated under air condition and found to be hermetic. The determined gas permeability of the pure SiGe diaphragm in this thesis under He conditions provides at least similar values. Considering Equation 5.8, the obtained leak rate of $4.5 \times 10^{-16}\,\mathrm{Pa\,m^3/s}$ at 23 °C can be translated for air. Then, molecular flow through a virtual pipe has to be assumed as all other components of air have larger molecular diameters and are less noble than He (see Table 5.4). The virtual leak rate for air is calculated as $1.7 \times 10^{-16}\,\mathrm{Pa\,m^3/s}$. This result is in agreement with the best obtained sealing in [43] (SACVD SiO_2 layer with $1.0 \times 10^{-16}\,\mathrm{Pa\,m^3/s}$).
It is evident, therefore that a hermetic sealing by the use of the developed CVD SiGe layer applied to a perforated PECVD SiGe diaphragm has been achieved. Further, the results of He exposure to poly-Si diaphragms sealed by 200 nm LPCVD Si_3N_4 are comparable as well. However, Si_3N_4 can possibly provide an even better hermeticity. Due to the detection limit in [227], the real leak rate might not have been found.
Even though the obtained results exceeded the expectations, it is worth comparing the results to a pure SiGe diaphragm with additional sealing layer to verify the results.

5.4 Exposure to Pressure Sensor-related Stress Impacts

In this section, 7 samples with an area of about 1 cm^2 from an identical substrate are chosen to evaluate the characteristics of 14 diaphragms with a diameter of 300 µm after applying different, typical stresses. These measures can be used to make application-specific predictions about life expectancy. In the event of failure, these tests help to identify weak points. An application-specific and pressure sensor-related stress for example is overpressure. A barometric sensor should usually withstand at least twice the working pressure. In the case of sensors that are operated in contact mode, the overpressure stability defines the maximum dynamic range.
Other sensor-related stresses are for example pressure and temperature cycle tests. If applied over a wide range, these tests can potentially detect fatigue fractures and define minimum cyclic strength. The largest available diameters of 300 µm with the highest available sensitivity are chosen for two reasons:

- In order to identify any trends in a reasonable time and effort.
- In order to use the largest possible number of pixels at highest magnification for the characterization of the membrane surface (compare Section 5.2).

Out of 14 diaphragms, 2 are taken as references and are not exposed to any stress other than laboratory conditions (23 ±3°C, 35 ±10%RH and 1015 ±35hPa). These are characterised together with the remaining 12 diaphragms, of which 4 of each are exposed to temperature cycles, overpressure, or pressure cycles.
In order to determine the impact of the applied stresses, the sensitivities of the individual diaphragms are evaluated at 3 points at least within a range of about 700 hPa to 1500 hPa at 23 ±3°C. The stress-related impacts can affect the diaphragm sensitivities which are assumed to be constant in the given temperature ranges. This is because the changes in membrane deflection caused by thermal expansion are clearly within the range of linear expansion and the range of diaphragm deflection evaluated in this work. By this method, temperature-related effects are intended to be compensated. The applied method lacks an accurate temperature control of the substrate while the optical characterisation

under applied pressure is performed. Temperature sensitivities of pressure sensor diaphragms can occasionally compete with the pressure sensitivities, and are therefore often compensated by calibration.
In addition, the diaphragm characteristics expressed as calculated capacitive sensitivities are considered. This offers the advantage of considering all the measurement data along the diameter of a diaphragm instead of single point measurements at the maximum and thus, the evaluation becomes less faulty.

5.4.1 Experimental Setups

Temperature Cycle Test

Temperature cycles are performed in a *Thermal Shock Chamber TSA-71H-W* by *ESPEC*. The programmed, fully automatic test sequences varied the temperatures from $-40\,^{\circ}\mathrm{C}$ to $115\,^{\circ}\mathrm{C}$ within ramp times of less than 3 min and hold times of about 15 min in accordance to the JEDEC standard *JESD22-A104-B*, test condition *I* [231].

Overpressure Stability Test

The overpressure stability test provides that the diaphragms are stored in a pressure vessel under a high load for 12 h. The further storage conditions are an N_2 atmosphere and $23 \pm 3^{\circ}\mathrm{C}$. After a waiting period of at least 6 h, a control measurement is performed. The loads are increased incrementally in 1000 hPa steps in a range from 3000 hPa to 6000 hPa with an accuracy of about $\pm$ 1 hPa.

Pressure Cycle Test

Another method to determine the reliability and endurance of the diaphragms is a pressure cycle test. The idea is to apply many thousands of cycles within a wide pressure range. For this purpose, a cycle test setup has been developed in this thesis. This setup is shown in Figure 5.11 a.. Two different pressures are provided by vessels having constant pressures of 250 hPa and 2100 hPa. These pressures are chosen with respect to the characteristics of the diaphragms under testing. The CPP is about 600 hPa for diaphragms with a diameter of 300µm, see for example Figure 5.7 on Page 139. The selected pressure range from 250 hPa to 2100 hPa causes diaphragm deflections which pass through the CPP. This ensures

a touch down of the diaphragms in every pressure cycle. This should ensure a significant cyclic stress load. These pressures are applied to a pressure vessel, in which the DUT are stored (1). The applied pressure is monitored by a pressure sensor (2). Two 3/2-way magnetic pressure valves (3) are controlled via a high precision pressure control unit (4) and a PC. The valves can either ventilate or evacuate the pressure chamber within a very short time. The test setup is utilised to apply an individual pressure cycle within 1.6 sec, initially starting at 1000 hPa, increasing to 2100 hPa, then decreasing to 250 hPa, each with maximum dwelling times of about 0.5 sec. The short load durations allow a high number of cycles in reasonable test time. This procedure is shown in Figure 5.11 b.. The maximum deviations of 20 shown cycles are below 1 % of the nominal applied pressure. This indicates that the pressure cycles are applied highly reproducibly.

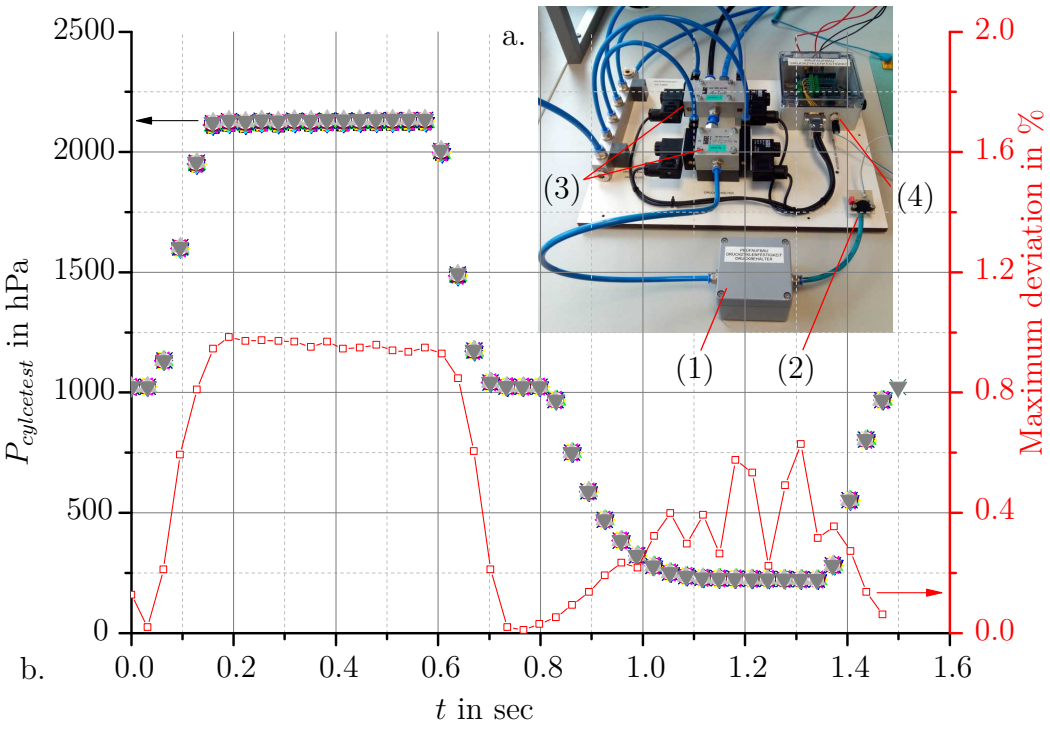


Figure 5.11: a. Photograph of the pressure cycle test setup consisting of a pressure vessel (1), a reference pressure sensor (2), two 3/2-way magnetic pressure valves (3) and a pressure control unit (4). b. Characteristics of 20 pressure cycles from 250 hPa to 2100 hPa.

There are standards as for example *DIN75553* or *AEC-Q100-Rev-H* which define pressure cycle test procedures. According to *DIN75553*, for example, 100 000 pressure cycles should be applied with a frequency of 4 / min, of which 20 000 should be applied at the highest specified temperature and between 0 and the

highest pressure in the specified dynamic range. The remaining 80 000 pressure cycles are defined to be applied at 20 °C. Thus, the developed setup enables procedures, which are related to the standard *DIN75553*. While a number of 80 000 cycles at 20 °C and the required maximum pressure can be designed according to the standard, the test procedure deviates from the standard *DIN75553* with regard to the cycles at elevated temperature and the frequency. A temperature control is not realised in the shown setup and the cycle frequency is increased to about 37 / min for time reasons.

5.4.2 Results of Stress Applications

The experimental design for the different types of stress exposure is shown in Table 5.10. The reference diaphragms are measured after 72 h, 159 h, 182 h and 286 h, together with the pressure cycled diaphragms after 37 000, 150 000, 180 000 and 250 000 runs and the diaphragms which have been exposed to overpressures of 3000 hPa, 4000 hPa, 5000 hPa and 6000 hPa. Further, 400 and 580 temperature cycles are applied. The results of the diaphragm deflection measurements

Table 5.10: Experimental design for stress application.

Diaphragm	Stress	Control measurement			
		post1	post2	post3	post4
1-2	Time at atmospheric conditions in h	72	159	182	286
3-6	Amount of pressure cycles	37 000	150 000	180 000	250 000
7-10	Overpressure in hPa	3000	4000	5000	6000
11-14	Amount of temperature cycles	400	580	-	-

are drawn in Figure 5.12. First, the upper plot shows the calculated sensitivities in fF/hPa, which are obtained by taking the double integral of the cross section lines and the diaphragm area. At least, three pressures of 700 hPa, 1050 hPa and 1500 hPa are applied to determine the sensitivities.
Second, the coefficients of determination, R^2, are drawn to demonstrate the linear correlation of the diaphragm displacement. For all measurements, the values of R^2 are higher than 0.99. On the one hand, this shows that only linear elastic deformations have been forced and, on the other hand, that no significant shift of the CPPs can be observed. The diaphragms are still in contact mode. Thus, it

can be claimed that no leaks occurred due to defects, which would have enabled molecular gas flow.

Third, the lower plot shows the deviation in % of the control measurements with regard to the initial (pre) measurement. It can be seen that the reference diaphragms show variations of about ± 5 %. This indicates a higher measurement error compared to the measurements in Section 5.3.2, where 3.5 % has been found. This may be due to an additional reproducibility error, which is caused by different setups. Here, a higher effort of opening and closing the pressure vessel is required, which is accompanied by a large movement and refocusing of the optical aperture. For this reason, the detection limits are drawn as red dotted lines at the ±5 % levels in order to compare the stress-affected deviations of the capacitive sensitivities with regard to the reference diaphragms.

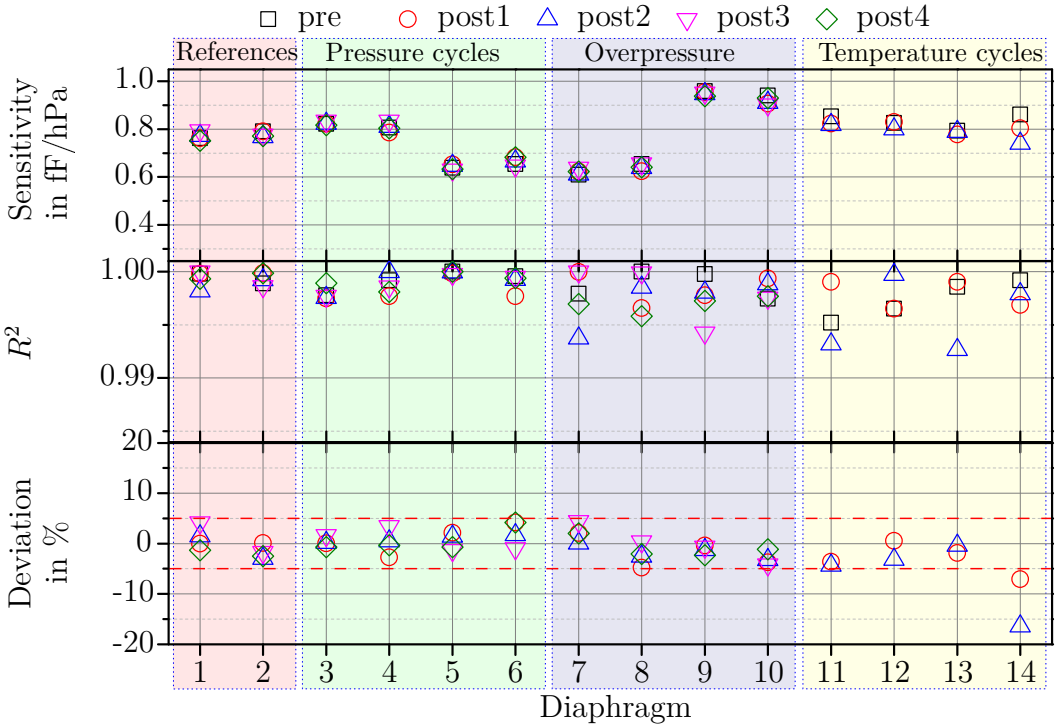


Figure 5.12: Variation of the capacitive diaphragm sensitivities, the coefficient of determination R^2 for the linear regression, and the deviation from initial (pre) measurement after stress exposure (pressure cycles, overpressure storage, temperature cycles) compared to reference diaphragms. The detection limits are drawn as red dotted lines at ± 5 %.

With respect to the reference diaphragms, it can be observed that the application of the different stresses neither causes higher deviations than 5 % from the

initial measurement, nor are trends to be observed. An exception is provided by diaphragm 14, which shows deviations smaller than −5 % and a significantly declining sensitivity. This indicates that this diaphragm could suffer from a leak caused by small defects which enable molecular gas flow.
A different perspective is drawn in Figure 5.13 a. in order to visualise potential trends. Here, the data are arranged next to each other as bars. The majority of data points alternates between positive and negative deviations, thus showing no trends.

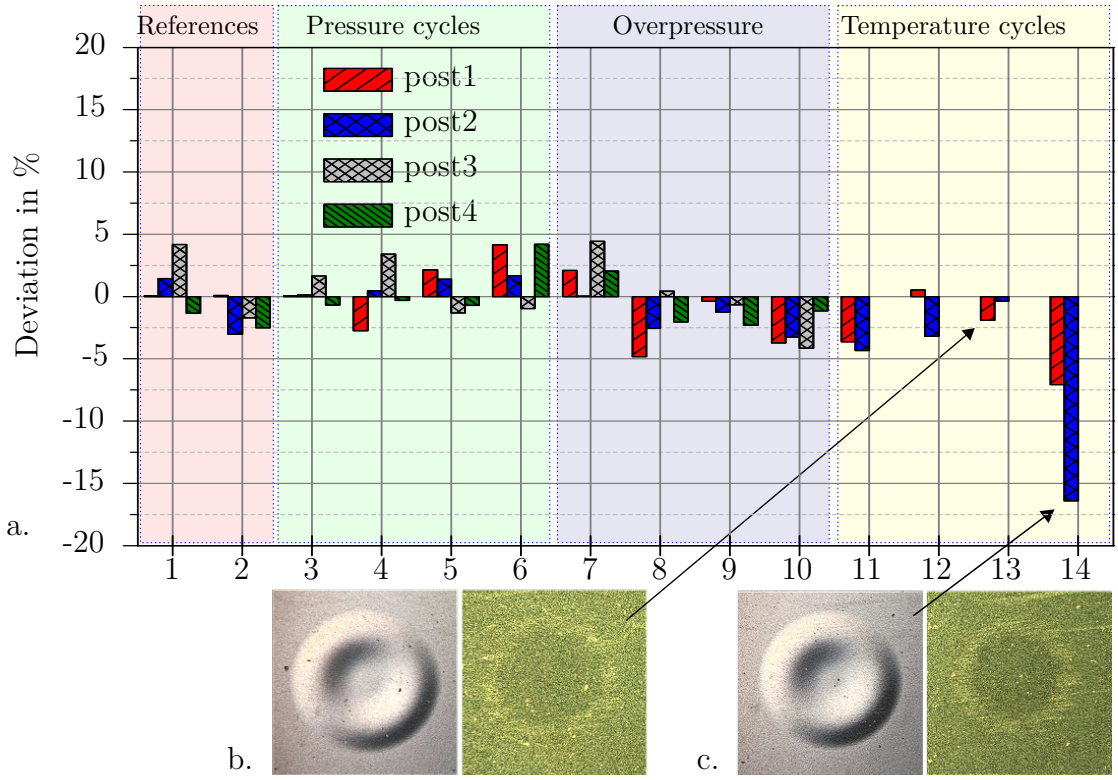


Figure 5.13: a. The deviation of the capacitive sensitivities from calibration measurement after stress exposure (pressure cycles, overpressure storage, temperature cycles) compared to reference diaphragms. Bright and dark field microscopic images of the diaphragms 13 (b.) and 14 (c.) are shown at the time after the 2nd control measurement (post2).

Further, in b. and c. bright and dark field microscopic images of diaphragm 13 and 14 at atmospheric pressure are shown. As both diaphragms are located on the same device, the differences between the deviations of both diaphragms is not assumed to be a consequence of the applied temperature cycles. The comparison of the microscopic images shows that there are some scratches visible on the surface around diaphragm 14. This indicates that mechanical damage may have

caused the unusual measurement results. Such damage could have originated while handling the sample in the test system.
For these reasons, diaphragm 14 is excluded from the following summary in Table 5.11. The arithmetic means, the one sigma standard deviation and the absolute maximum deviation of the diaphragm sensitivities presented in Figure 5.12 and Figure 5.13 are calculated for the corresponding partitions.
The absolute maximum deviations vary from 4.2 % to 4.8 % for all partitions. As no trends can be observed for 13 diaphragms, the results can further be averaged over all diaphragms. For 13 diaphragms, a mean deviation of −0.7 % is obtained with an 1σ error of 2.2 %. The maximum observed deviations are within the evaluated detection limit of the applied method. Therefore it can be assumed that the developed diaphragms show no significant differences in terms of measurement accuracy with respect to the unstressed references. Thus, the pure SiGe diaphragms can be deployed in contact as well as in non-contact mode up to 2000 hPa for at least 250 000 pressure cycles, for at least 580 temperature cycles from −40 °C to 115 °C, and have a burst pressure stability of 6000 hPa for at least 12 h.

Table 5.11: Summary of impacts due to applied stress regarding the capacitive sensitivity.

Diaphragm	Stress	Summarised results in %		
		Mean dev.	1σ dev.	|Max. dev.|
1-2	References	−0.4	2.1	4.2
3-6	Pressure cycles	0.8	2.1	4.2
7-10	Overpressure	−1.1	2.5	4.8
11-13	Temperature cycles	−2.2	2.1	4.3
$\sum 13$	Arithmetic mean	−0.7	2.2	4.4

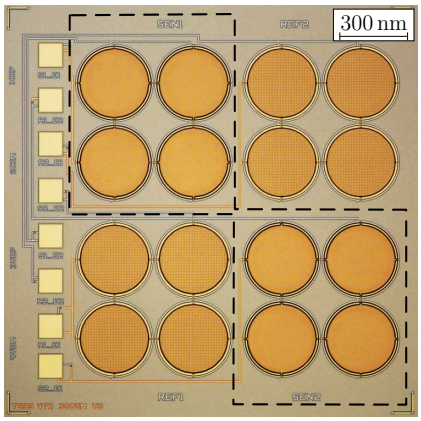
5.5 Comparison of Calculated Sensor Performance to State of the Art

The evaluated test structures in this thesis are to be used as post-CMOS compatible pressure sensor elements. However, the test structures developed in this

thesis can not be measured electrically, as explained before. Therefore, the evaluated capacitive performance so far, which is for example shown in Figure 5.6 on Page 137, is calculated by integration over a deflection line through the centre of a diaphragm according to Equation 2.7. The data are obtained by phase shift interferometry, which is explained in Chapter 5.2. Further, the capacitances are determined assuming a minimal distance between the virtual capacitor plates of 300 nm, which is in agreement to the CVD SiGe layers inside the cavity as shown in Figure 5.1 on Page 126.

The obtained capacitive performance of 300 µm diaphragms in contact mode is multiplied by the factor of 8 because 8 diaphragms are measured in parallel. The wiring of such a sensor is shown in Figure 5.14 a.. The diaphragms shown here cannot yet be electrically contacted. The final sensor will be integrated first hybrid, later monolithically in an ultra-low noise capacitive read-out ASIC developed at Fraunhofer IMS [183]. The intended sensor die area is 4 mm^2. The compatibility of this ASIC is, amongst others, demonstrated with a capacitive pressure sensor element which was fabricated in 1.2 µm intermediate-CMOS compatible technology at Fraunhofer IMS [183].

a.



b.

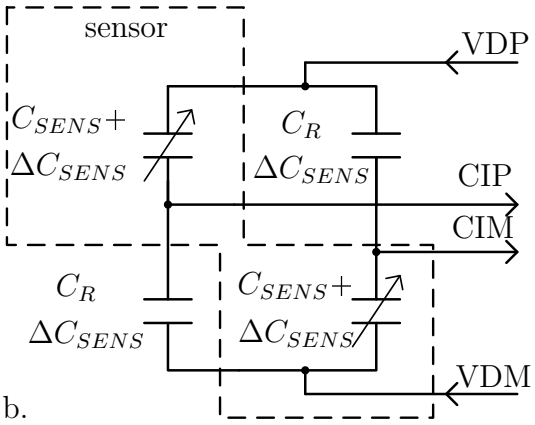


Figure 5.14: a. Microscope view on a sensor comprising 8 sensitive (within dashed line) and 8 reference diaphragms with 300 µm diameters, arranged in groups of 4 diaphragms and wired to be directly wire bonded to an ultra-low noise C2V read-out ASIC as drawn in b. (after [183]).

The basic concept of the sensor element is as followed. There are pressure-sensitive and pressure-insensitive diaphragms which are wired in such a way that a differential output signal is generated and a pre-compensation of side effects is achieved. As mentioned before, the fabrication of the diaphragms is not finalised

due to unforeseen machine downtime which impeded the CVD SiGe sealing of so far fabricated wafers. The wiring to connect the sensor to the ROIC is drawn in Figure 5.14 b. (after [183]).

A **F**igure **O**f **M**erit (FOM) is created which comprises the capacitive signal, the **D**ynamic **R**ange (DR) and the net total sensor area of sensitive diaphragms. Thus, a calculated capacitive signal density per net sensor area is defined. In order to classify the calculated capacitive performance with respect to other reported capacitive sensors, a comparison is listed in Table 5.12 after [232]. Some characteristics of hybrid and monolithic capacitive pressure sensors are listed and the corresponding FOM are calculated. The comparison of the created FOM

Table 5.12: Capacitive pressure sensor performance after [232] (*capacitance values for this thesis are calculated).

Year	Reference	CMOS-MEMS integration	Diaphragm geometry	Net Sensor Area in mm^2	Sensitivity in fF/hPa	DR in hPa	On-Chip ROIC	FOM in pF/mm^2
2001	[233]	Hybrid	Circular	4.00	26.6	600 to 800	No	1.3
2005	[234]	Hybrid	Square	0.64	8.0	800 to 1060	No	3.3
2010	[235]	intermediate-CMOS	Square	0.50	9.40	300 to 500	Possible	2.3
2011	[236]	Hybrid	Circular	0.03	15	10 to 20	No	12
2012	[72]	post-CMOS	Square	0.04	0.07	0 to 1000	Yes	1.8
2015	[232]	Monolithic	Elliptical	0.43	0.78	100 to 1000	Yes	1.6
2017	[183]	Hybrid	Circular	0.08	1.8	150 to 1500	No	30.3
2018	This thesis	Monolithic	Circular	0.57	6.4 *	500 to 2000	Possible	16.8

shows that the calculated capacitive characteristics of the diaphragm test structures are very promising. An FOM of about 17 pF/mm^2 is calculated which is based on the deflection measurements in contact mode. It should be noted that the dynamic range is not exhausted for the presented diaphragms. The measurements are limited to 2000 hPa due to restriction in the optical measurement system. Therefore, there is a limited comparability to the system with the highest rating. The hybrid pressure sensor reported in [183] achieves a calculated FOM of about 30 pF/mm^2. This sensor contains diaphragms with a CPP of about 1600 hPa. This means that the non-contact mode is used for operations in which the sensitivity is naturally higher. A second limitation is the increased CVD SiGe deposition inside the cavity. As already discussed, this can be effectively minimised by applying the developed side-wall spacer technology or increasing the pitch of the etch-access channels. The deposition inside the cavity influences the capacitive sensitivity directly because it increases the thickness of the isola-

tion layer t_{iso}. It has a linear reciprocal influence on the capacitance in contact mode as shown in Chapter 2.1.3, Equation 2.11. Thus, significant improvement potential has been identified for both limitations. Therefore, it can be assumed that the FOM of the presented system is a rather pessimistic value. Compared to other sensors, the FOM represents a very promising value and clearly demonstrates the potential of the developed technology for a post-CMOS integration of capacitive pressure sensors.

6 Conclusions

The development of a CMOS-compatible technology for the fabrication of pressure sensor elements is described. This thesis demonstrated the general feasibility of a CMOS-compatible fabrication of pure SiGe diaphragms which are partially boron-doped for the use in capacitive pressure sensors. The maximum applied process temperature is 375 °C for SiGe deposition, thus the temperature limit of 400 °C is maintained. Substantially, the results regarding the following topics are summarised:

- Sufficient protection of any CMOS substrate, especially against etching media needed for sacrificial layer release.
- Sacrificial layer release technology with focus on:
  - Utilisation of vapour-phase etching.
  - Prevention of stiction.
  - Efficient etch-access design to enable efficient release times of diaphragms with diameters in a range from 100 µm to 300 µm.
- Sufficient cover of etch-access design.

SiC Protection Layer In order to enable a sufficient protection of any CMOS substrate, a low-temperature SiC layer was developed. This enables applying vapour release technologies in post-CMOS processing. An appropriate gas flow ratio setup for H_2:CH_4:SiH_4 of 3 : 0.5 : 1 at 300 °C, a deposition pressure of 2.7 Pa, 100 W RF Power, 2000 W ICP power was found to enable sufficient protection. This layer features a mechanical stress in a range of −300 MPa to −150 MPa.
The protection of underlying SiO_2 layer during vapour-phase etching in HF/H_2O was demonstrated by a SiC layer thickness even of about 100 nm. A vapour HF process range from 6.7 hPa to 26.7 hPa was applied at 40 °C and utilising HF, H_2,

N_2 as process gases. The SiC were characterised by the use of EDX, XRD, SEM, and Raman spectroscopy. SiC layers comprising Si, α–SiC ($4H$, $6H$, $8H$) and amorphous SiC were achieved with a deposition rate of about 3.3 nm/ min.

Vapour HF Release Etch Vapour-phase HF etching is an appropriate technology to release free-standing MEMS structures. By the use of the vapour phase, stiction can be avoided. Stiction can be caused by mechanical stress on MEMS due to attractive capillary and adhesive forces. The release process is based on the water-assisted condensation of the vapour HF:H_2O mixture on the surface of the sacrificial oxide. Therefore, physical parameters influence process properties such as the amount of condensed liquid film or the etching rate. It was demonstrated that stiction is avoided by process pressures below 13 hPa. The etching rate is then limited to about 1 µm/ min. The efficient sacrificial layer release etch was established by vertically arranged etch-access tunnels. It is thus independent from the diameters of the diaphragms.

Pressure Sensor-related Evaluation of SiGe Diaphragms One of the main challenges in the development of post-CMOS compatible pressure sensor elements is the sealing process. The approach of using a CVD SiGe process to cover perforated PECVD SiGe diaphragms has successfully been tested with the largest and most sensitive diaphragms with diameters of 300 µm and thicknesses of about 1.3 µm. The presented results characterised diaphragms which have been released stiction- and residual-free with the aid of vapour-phase HF etching in vapour H_2O. The quality of a CVD SiGe layer is examined by He leak testing. The gas permeabilities of the PECVD and CVD SiGe diaphragm are dependent on the temperature and are about $7.9 \times 10^{-20}\,\mathrm{m^2/s}$ at 23 °C and about $2.4 \times 10^{-19}\,\mathrm{m^2/s}$ at 89 °C. These results are in compliance with literature values for solid semiconductor materials, such as Si or SiGe. Thus, a complete and sufficient closing of the open diaphragm is achieved.
Further, diaphragms have been exposed to pressure sensor application related stress impacts and compared to unstressed reference diaphragms. Here, the impacts on the capacitance-to-pressure sensitivity is evaluated. For 13 diaphragms, a mean deviation of $-0.7\,\%$ is obtained with a 1σ error of 2.2 %. No trends can be observed after extensive application of temperature cycles, overpressure,

or pressure cycles. Moreover, the individual observed maximum deviations are smaller than the evaluated detection limit of the applied method. The maximum deviations of the stressed diaphragms are equal or less than the deviations of unstressed reference samples. Therefore the developed diaphragms show no significant differences under stress in terms of measurement accuracy. Thus, the results indicate that the SiGe diaphragms can be deployed in contact as well as in non-contact mode up to 2000 hPa at least. These can be exposed to at least 250 000 pressure cycles, for at least 580 temperature cycles from −40 °C to 115 °C, and have a burst pressure stability of 6000 hPa for at least 12 h.

Although the applied evaluation method is not ideal to evaluate the pressure sensor performance and the obtained results represent more relative than absolute importance, it is a very appropriate and available method for the fabricated test structures. Future work will have to evaluate the sensor performance by means of electric sensor signals to obtain absolute results. Additionally, further parasitics have to be considered. For example, the determination of the influence of humidity on SiGe will then become more comfortable than by applying optical methods. Only then, the need for further sealing layers (e.g. ALD Al_2O_3 or Si_3N_4) can be finally revealed.

The results achieved so far clearly indicate that the presented method of fabricating a pure SiGe diaphragm is highly promising to be used for post-CMOS-compatible, capacitive pressure sensors. The calculated capacitive sensitivity is about 0.8 fF/hPa for a single 300 µm diaphragm in a pressure range of about 500 hPa to 2000 hPa. In this range, the diaphragms operate in contact mode and, thus, obtain a relatively linear characteristic. Contact mode operation is also suitable for overcoming the inherent non-linearity of capacitive sensor elements present in normally used non-contact operation. In contact mode, the investigation of the pressure hysteresis should have high importance. The pressure curves presented in the this work do not show a significant hysteresis. Because the optical method of investigation applied here is not appropriate for a required dynamic evaluation of the diaphragm performance, a potential hysteresis is not evaluated in detail. Nevertheless, pressure hysteresis is not observed so far. This may be due to the high restoring forces introduced by the compressive layer stress in the diaphragm. A further explanation could be the increase in the roughness of the inner cavity surfaces caused by the deposition of CVD SiGe in the cavity. Both

circumstances are assumed to be beneficial to minimise any potential pressure hysteresis. The question for pressure hysteresis will have to be addressed with the aid of electrical functional sensor devices, analogous to the presented results in [183].

Discussion on Process Chain The test structures which were evaluated regarding the quality of the CVD SiGe cover layer were fabricated differently to the developed process chain. Apart from the 1st MEMS wiring level and the protection layer, the main difference was that the sacrificial layer was not patterned. As the results of the test structures successfully demonstrated, the fabrication offers potential for integration in a complete post-CMOS compatible process chain. A schematic process flow is shown Figure 6.1.
The basis is again a 1st MEMS wiring level (TiW) (a.). The deposition of a sacrificial layer (SiO_2), which is patterned enables a connection to the 1st MEMS wiring level (b.). By the deposition of the 2nd MEMS wiring level (PECVD SiGe), the connection is established (c.). The processes to create vertically-arranged etch-access channels comprise the deposition of two hardmasks. By these side-wall spacer processes, the etch-access channels are patterned by DRIE (d.). An in-situ removal of both the hardmasks and the sacrificial layer is possible by applying vapour HF (e.). The deposition of the diaphragm cover (CVD SiGe) closes the diaphragms (f.). Subsequently, the patterning of the 2nd MEMS wiring level and the deposition of a sealing is shown (g.). Finally, a bond pad metal stack can be applied if necessary (f.).
In comparison with the developed process chain in Chapter 4.1.3 (Figure 4.5), this process chain may show some advantages. The main differences are summarised:

- There are three possible reasons why the use of a SiC protection and isolation layer may become redundant between a. and b.:

    1. The entire wafer surface is protected from vapour HF etch attack by SiGe 1st MEMS wiring level, which is only patterned by etch-access channels.

    2. If the capacitor area of TiW 1st MEMS wiring level is designed larger than the area of vertically-arranged etch-access channels, the substrate is protected from vapour HF etch attack by the TiW.

3. The then missing isolation function could be established again by the CVD SiGe deposition inside the cavity. However, the layer growth characteristics of CVD SiGe on TiW is not known, but should be the prerequisite.

- Additional processes to modify the side wall angle of a patterned sacrificial layer are removed. The side wall angle is fixed to zero. Thus, the measurement results should become more consistent to theoretical models.
- One photolithographic process step can be eliminated because a patterning of the sacrificial layer is omitted. Instead, the cavity area is defined by the vapour-phase etch on time and the area equiped with vertical etch-access channels. Thanks to the independency from diaphragm diameters, all diameters can be released within the same etch time.

This improved process flow may also involve some disadvantages that should be evaluated. For example, there are open surfaces of the sacrificial oxide within the cavity which are not covered by the CVD SiGe layer. Here, cross sensitivities due to humidity or outgassing can be generated.

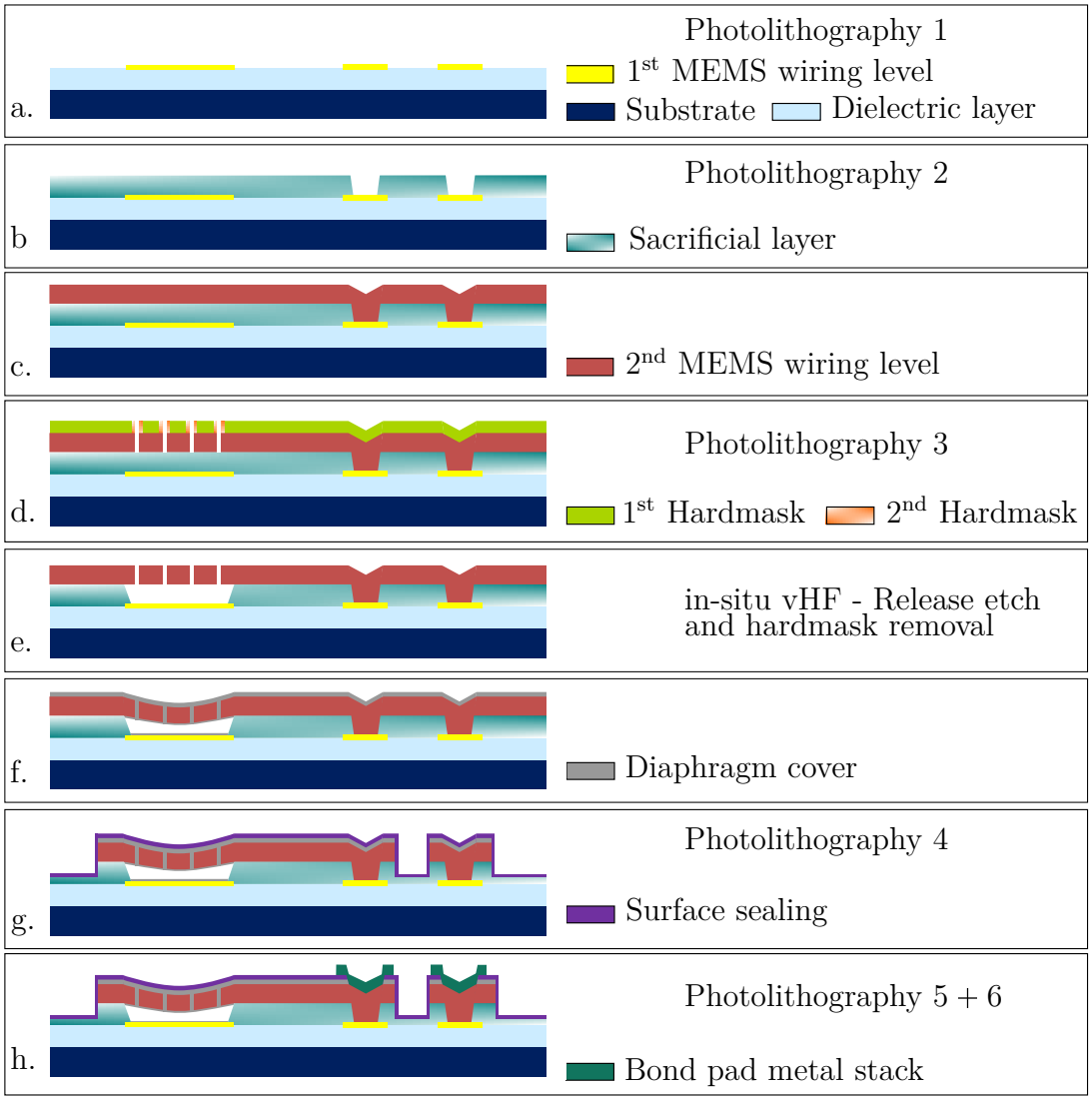


Figure 6.1: Alternative process chain based on the fabricated test structures: a. 1st MEMS wiring level (TiW), b. sacrificial layer (SiO_2) with via opening to the 1st MEMS wiring level, c. deposition of 2nd MEMS wiring level (PECVD SiGe), d. DRIE of etch-access channels through side-wall spacer processes (hardmasks), e. in-situ removal of hardmasks and sacrificial layer release, f. deposition of diaphragm cover (CVD SiGe), g. patterning of 2nd MEMS wiring level and deposition of sealing, f. bond pad metal stack.

7 Outlook

For the ongoing industrialisation of a capacitive post-CMOS pressure sensor further work is necessary. Some future tasks are presented in this chapter which may help to reach commercial maturity. The outlook is sorted by short-, medium- and long-term tasks for necessary developments.

The developed diaphragm stack comprising a perforated, in-situ boron-doped PECVD SiGe layer which is then covered by a CVD SiGe should be further evaluated regarding stress and deflection. After a significant machine repair and maintenance, the evaluated CVD SiGe characteristics regarding stress and substrate dependent incubation times have to be verified. Finally, the CVD parameter setting should be identified to establish an optimised layer stress in order to yield a desired shape of the diaphragm. An optimised shape should rely on a layer stack which is almost free from intrinsic stress.

For the purpose of applying the CVD cover layer, the developed side-wall spacer technology to minimise the etch-access channels should be used and, thus, demonstrate the effects of minimised deposition inside the cavity. Consequently, a beneficial effect is expected regarding the shape of the diaphragm due to a reduced required cover-layer thickness.

The electrical characteristics of the two wiring levels and the pad electrodes needs to be evaluated with respect to the SiGe diaphragm stack comprising in-situ boron-doped PECVD SiGe and undoped SiGe.

The necessity of an additional sealing layer (e.g. Si_3N_4 or ALD stack comprising Al_2O_3 and or Ta_2O_5) must be clarified. Because Ge is reported to be more affected by humidity compared to Si, oxidation can become an issue. GeH species are more unsteady than SiH species [144, 148, 149]. If an additional sealing becomes necessary, the effects on the diaphragm deflection must be evaluated and optimised.

The principle functionality of a porous ALD composite layer was shown. The

benefit of this option would be a significant minimisation of any depositions inside the cavity. However, further evaluations regarding stress and the efficiency of diaphragm sealing are still pending. Additionally, the homogeneous distribution of the components of the composite layer over the entire wafer surface could be a critical point. To achieve a high yield in the sacrificial layer release etching, homogeneous thickness and ratio of the components is assumed to be crucial.
An electrical evaluation of capacitive sensor elements with focus on pressure sensor characteristics, such as hermeticity, cross sensitivities (temperature, humidity) are absolutely necessary to verify and to complete the so far obtained results, which are based on optical characterisation with relatively large measurement errors.
The approach of post-CMOS integration of capacitive pressure sensor elements promises a reduction of parasitics. This is going to be evaluated in terms of **S**ignal to **N**oise **R**atio (SNR). For this purpose an ultra-low noise ROIC was developed at Fraunhofer IMS which is well suited to evaluate the noise performance of capacitive MEMS such as pressure sensor elements or accelerometers. By the use of the same ROIC substrate the results can directly be compared to a hybrid system which is already publicised in [183].
A future topic can be SiGe laser annealing to further reduce the process temperatures to below 250 °C [237, 238]. This method could become interesting if the temperature limits become even stricter. This could be the case, for example, for even more advanced CMOS circuits.

A Appendix

The aim of this thesis was to develop capacitive pressure sensor elements, which fulfil the requirements regarding post-CMOS fabrication. For the post CMOS integration of the capacitive pressure sensor elements, potential ROICs were considered. For this purpose the *IMS-CAP51* was developed by Fraunhofer IMS [183] in parallel to this thesis. This ROIC is fabricated in a standard 0.35 µm technology at Fraunhofer IMS automotive certified CMOS fab. It is an analog readout circuit for capacitive MEMS sensors such as accelerometers, gyroscopes or pressure sensors. In Figure A.1 a single ROIC with edge length of 3.5 mm x 3.5 mm is shown.

Excluding the pad frame, a reduced area of about 3.1 mm x 3.1 mm can potentially be utilised by post-CMOS sensor fabrication. A flexible interface allows connecting a wide range of types of capacitive sensing elements. The ROIC was designed with focus on ultra-low noise operation and high analog measurement performance. The measured input referred noise is below $50\,\mathrm{zF}/\sqrt{\mathrm{Hz}}$ within a bandwidth of 10 Hz to 10 kHz. Four adjustable gain settings allow the adjustment to full scale measurement ranges from ±750 fF to ±3 pF. This ensures the compatibility with a wide range of sensor applications. The full input signal bandwidth ranges from 0 Hz to more than 50 kHz.

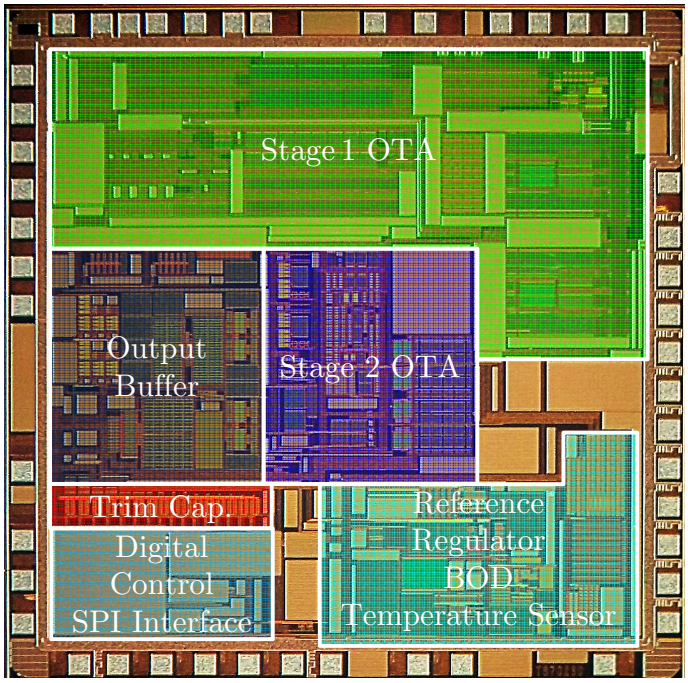


Figure A.1: Photograph of a single ASIC for ultra-low noise capacitance to voltage conversion, after [183].

Various types and configuration of capacitive sensors can be chosen to this ROIC. A capacitive bridge configuration has to be formed by the sensor and additional external or internal components to establish a fully differential four-wire interface. Figure A.2 illustrates four possible interconnections. Sensors with three electrodes can be connected using reference capacitors for the lower half of the measurement bridge (Figure A.2 a.). For fully differential sensors, as well as for sensors with a nominal capacitance less or equal to 2.5 pF, these reference capacitors can be omitted (Figure A.2 b. and c.). Single ended sensors with only two electrodes can also be connected as illustrated in (Figure A.2 d.).
This ROIC was used to evaluate the characteristics of capacitive pressure sensor elements (MEMS) fabricated in an established intermediate CMOS fabrication on the one hand. A hybrid system comprising the ROIC and the MEMS was realised, which was electrically contacted by means of wire-bonding. This is shown in Figure A.3. The characteristics of the hybrid system will be compared to a system with post-CMOS integrated pressure sensor elements, which are developed in the frame of this thesis.

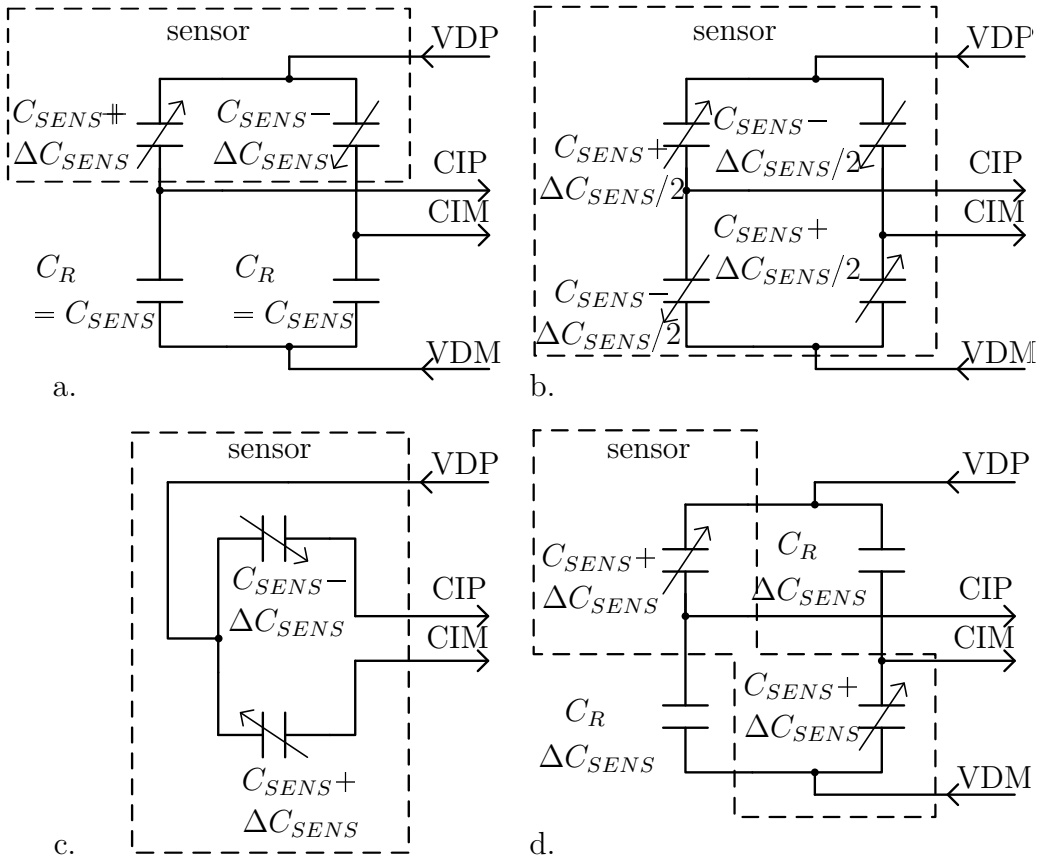


Figure A.2: Different interconnection options for different types of sensing elements: a. differential sensing element using reference capacitors, b. fully-differential sensing element without external devices; c. differential sensing element with low nominal capacitance and d. single ended sensing element [183].

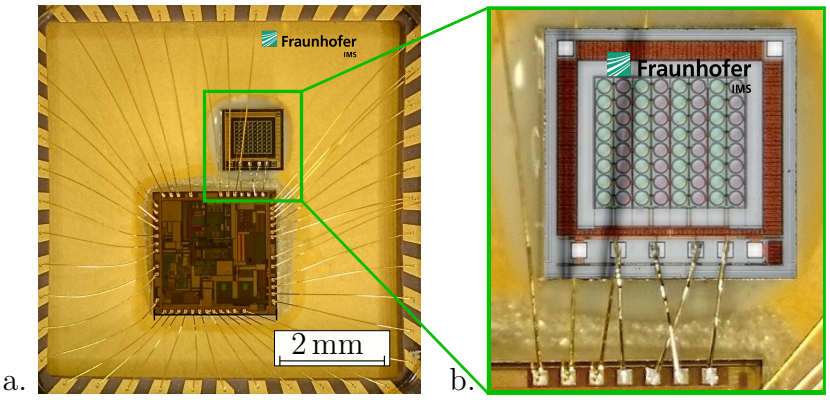


Figure A.3: a. Hybrid sensor system comprising the capacitive pressure sensor element with diaphragm diameters of about 92 µm and the C2V converting ROIC, both mounted in a CLCC44 package. b. Magnification of the pressure sensor element.

Own Publications

Peer-Reviewed Journal Articles

A. Utz, **C. Walk**, N. Haas, Norbert, T. Fedtschenko, A. Stanitzki, M. Görtz, M. Mokhtari, M. Kraft and R. Kokozinski, 'An ultra-low noise capacitance to voltage converter for sensor applications in 0.35 µm CMOS', *Journal of Sensors and Sensor Systems*, **6**, 2017, 285–301.

J. Weidenmüller, **C. Walk**, Ö. Dogan, P. Gembaczka, A. Stanitzki and M. Görtz, 'Telemetric multi-sensor system for medical applications – The approach', *tm - Technisches Messen*, **84**, 2017, 53–58.

Conference Proceedings

C. Walk, Ö. Dogan, M. Görtz, W. Mokwa and H. Vogt, 'Post-CMOS MEMS Capacitive Pressure Sensor: Compatible Porous ALD Membrane for Sacrificial Layer Release and Diaphragm Sealing', *Smart Systems Integration, Proc.*, **12**, 2018.

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