

Power Electronic Control Device for High Voltage Test Transformers

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Motivation

“Remove the stones from your way toward the target, don’t leave small problem behind, it will appear again ”

Prof. Dr.-Holger Hirsch

In AC high voltage tests such as partial discharge (PD) measurements and dielectric test, the test’s voltage source quality can influence the test results accuracy. Therefore, the international standards for high voltage testing techniques [1,2] determine a limit of distortion value of a sinusoidal voltage wave shape. The ratio of the voltage peak to its root mean square value (RMS) must be within $\sqrt{2} \pm 5\%$, and a total harmonic distortion (THD) less than 5% as well. Practically due to the presence of harmonics in power network and using a step up transformer for AC tests, the distortion of an AC sinusoidal signal could exceed the standard limit.

Voltage breakdown is an expectable result of a high voltage (HV) dielectric test. Immediately after a breakdown an electric arc will form, which is fed from the test voltage source. To allow further investigations in case of solid state insulation materials, the applied voltage must be switched off very fast. For this purpose an early detection based on voltage fall time and current rise time of the breakdown channel is required. The breakdown has to be detected fast in order to switch off the applied voltage.

Performing a HV test using other frequencies such 60 Hz and 16.7 Hz are on market demand. Several methods are used to generate these frequencies, like motor generator (MG) system and static frequency converter. MG systems are bulky, heavy weight and require a lot of maintenance due to attrition of the mechanical parts. Recently MG are replaced by modern static frequency converters which are based on power electronic components, these converters are still having challenges to perform a PD measurements and HV tests due to their output signal quality, especially the total harmonic distortion (THD) and the background noise.

Partial discharge measurement is an effective method used for early detection of insulators age degradation. In real power grid time varying harmonics are present, where the insulation system of the devices in the grid are exposed to. During tests the voltage form has to be free from distortions, which does not necessarily represent the real challenges. For further fundamental investigations a source is needed, which allows the generation of a test voltage with a specific harmonic content. Such a device will also support the development of new techniques and intelligent machines which are able to separate between harmonic data and real PD pattern data for on-line PD measurements process[3].

In this dissertation a system will be introduced, which gives a solution to the above mentioned challenges.

Abstract

Electrical insulators reliability and age degradation estimation can be evaluated accurately by test. Beside other test procedures high voltage dielectric test(HV-DI) and partial discharge (PD) measurements are used for this purpose. Since the accuracy in test is an essential issue, HV-DI test and PD measurements have to be accomplished in nearly ideal signal quality of the test's voltage source, as well as controllable distortions(in presence of harmonics)in order to investigate all possible circumstances. Performing the test using other frequencies(16,7 Hz, 50 Hz, 60 Hz) are also on market demand.

For the dimensioning of the power electronic system, the essential components of a HV test system need to be characterised. The characterisation focus on the properties relevant for the use cases High Voltage Dielectric Tests and Partial Discharge Measurements. Based on this characterisation the required parameters for a single phase DC-AC-Inverter and the corresponding PWM parameters are derived.

The goal of spectral purity disallows the use of standard PWM schemes. Based on the Naturally Sampled PWM scheme as described in the literature [10], a new PWM scheme (Enhanced Unipolar PWM) is developed which allows its use for HV testing. The new driven algorithm is implemented in Digital Signal Processor (DSP) unit which is controlling an H-Bridge and an attached 100 kV, 5 kVA test transformer.

The fast Switch-Off unit in case of breakdowns is based on a detection algorithm which is implemented in a second DSP. The accurate detection of a breakdown uses signals from a current sensor in the primary circuit and the voltage signal from a HV divider.

Finally the functioning of the whole system is demonstrated in an experimental investigations.

For all those who have respect and love to the prophets and messengers, especially for Noah, Abraham ,Moses, Issa(Jesus) and Mohammed Peace be upon all of them

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Abbreviations

DSP	Digital Signal Processor
EMC	Electro Magnetic Compatibility
En-Unipolar-PWM	Enhanced unipolar pulse width modulation
EUT	Equipment Under Test
FFT	Fast Fourier Transform
HF-Unipolar-PWM	High Frequency Unipolar PWM
HV-DT	High voltage Dielectric Test
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
IH	Intended Harmonics
LPF	Low Pass Filter
MG	Motor Generator
MI	Measuring Instruments
NS-PWM	Naturally Sampled Pulse Width Modulation
NWHA	Network Harmonics Analyser
Pec-HV	Power electronics control device for high voltage test transformers
PU-DSP	Protection Unit Digital Signal Processor
PWM	Pulse Width Modulation
RMS	Root Mean Square
RS-PWM	Regularly Sampled Pulse Width Modulation
SWF	Switching Frequency
THD	Total Harmonic Distortion

Symbols

Symbol	Quantity	Unit
B	Magnetic flux density	T
H	Magnetic field strength	A/m
μ	material permeability	H/m
ϕ	Flux	weber
V_{PWM}	A general PWM signal	V
V_{OPWM}	Unfiltered H-bridge output voltage PWM signal	V
V_o	Filtered H-bridge output voltage PWM	V
V_{sine}	Desired sinusoidal signal	V
$V_{sine'}$	Inverted desired sinusoidal signal	V
V_{tri}	Carrier triangle signal	V
$V_{p_{sine}}$	Peak voltage of the desired sine signal	V
$V_{p_{tri}}$	Peak voltage of carrier triangle signal	V
m_a	Modulation index	
m_f	Modulation frequency ratio	
V_{DC}	DC voltage of the H-Bridge	V
ω_{sine}	Desired sine angular frequency	rad/s
ω_{tri}	Carrier triangle angular frequency	rad/s
α	Switching angel of the PWM	rad
T_{tri}	Time of one cycle of the carrier triangle signal	s
V_{sineh1}	First harmonic of V_{sine} or the fundemantal frequency	V
V_{sineh3}	3rd harmonic of V_{sine}	V
d_t	Dead time	s

f_{tri}	Triangle carrier signal frequency	Hz
f_{sine}	Desired sine signal frequency	Hz
T	Time of one cycle of the V_{OPWM}	s

1. Introduction

1.1 Thesis principles and aims

1.1.1 Signal quality in high voltage test

Dielectric tests (DT) are used for the validation of the selection of a suitable insulation materials, and Partial Discharge (PD) measurements allows to estimate the ageing behaviour of the materials. In classical way in order to perform a dielectric or PD test a step up transformer is used to generate high voltage, where the Equipment Under Test (EUT) is connected to the transformer's secondary winding. The step up transformer's primary voltage is variable, that can be done with a motor driven or manually operated variable transformer.

Unfortunately the voltage from the grid nowadays is not a pure sinusoidal signal due to the high number of nonlinear devices (e.g switched mode power supplies) connected to the grid. Nonlinear loads are the reason behind the appearance of a low voltage signals appear as multiple frequencies of the fundamental(main sinusoidal frequency) , these are known as Harmonics. Harmonics will adversely effect the test accuracy, that is why an international standards[1,2] has put a limit for the Total Harmonic Distortion (THD) for AC high voltage test. It has to be less than 5% and the ratio of sinusoidal peak voltage to its RMS must be within $\sqrt{2} \pm 5\%$. Harmonics are not stable in the power grid, the amount of THD will change according to the load. The Union of the Electricity Industry - EURELECTRIC has made a study on Europe power quality[5,6] which shows that the THD is increasing every year, more over it may exceed the standard limit(5%). Moreover, the step up transformers in HV tests will amplify the harmonics present in the voltage source and they produce additional harmonics due to the non-linearity of the iron core[7,13,14,29,46]. In Lab experiments the distortion factor could be more than 5% especially when the applied voltage is over $\frac{2}{3}$ from the transformer's primary rated value. Therefore, the requirements of the standards are hard to fulfil in such cases.

In [29,30,8] devices based on power electronics are presented. These devices are intended to do PD measurements and dielectric tests, they and many other devices described in companies websites e.g[53] or in other literature are focusing on the output signal quality of the device itself which is still not pure sine(THD roughly 3 – 5%) . Furthermore those devices do not allow the compensation of the generated harmonics by the test transformer itself, which in some cases is a real challenge to fulfil the HV-tests standards requirements.

1.1.2 Safety and protection in dielectric test

In dielectric tests which are used for the insulation investigations, the voltage applied to the dielectric material is gradually increased. At a certain point a breakdown occurs. The breakdown voltage is the amplitude of the voltage immediately before the breakdown. After the breakdown event an electric arc is built within the breakdown channel, which is fed by the power supplied through the test transformer. In case of solid state materials the arc leads to larger areas of damage so that further investigation on the break down development is nearly impossible. Therefore, the power feeding into the test transformer needs to be interrupted within a short time.

The concept of the system protection in dielectric tests is based on a fast detection of voltage fall time and/or current rise time in the breakdown channel. When a breakdown is detected a Solid State Circuit Breaker(SSCB) is triggered in order to switch off the voltage source, that will limit the injected energy in the breakdown channel.

Insulated Gate Bipolar Transistors (IGBT) or Thyristors (SCR) are commonly used as external SSCB unit. The rated switch off time is between few 100's of μs and few ms[25,26,27,28].

A previous development work of an external fast switch-off units was done at ETS institute at University of Duisburg Essen[24]. It consists of two IGBTs as switching off elements and the break down detector which is based on the voltage fall time. The switching off time for this device is roughly 500 μs (relatively high) and required extra semiconductor elements for construction, i.e. using the same semiconductors (IGBTs) of the H-bridge inverter will be an advantage.

1.1.3 Frequency conversion

The power frequency used worldwide is either 50 Hz or 60 Hz. For some railway systems the power frequency of 16.7 Hz is used. Therefore according to the market demand, performing HV-DT and PD tests with the power frequencies 50 Hz, 60 Hz and 16.7 Hz are requested.

Using a static frequency converter as a voltage source for HV tests and PD measurements is a great step forward in the field of HV tests. The test can be accomplished with variable frequencies(16,7Hz, 50Hz, 60Hz) as well as controllable amplitudes. The test source output signal quality still have two challenges; THD and background noise which are adversely influence on the test accuracy [17,8,18,22,16,29,22].

In order to analyse the reasons behind these challenges, the source of harmonics distortions and the background noise has to be comprehensively understood (from the frequency converter side).

A single phase static frequency converter consist of four main parts:

- AC-DC rectifier and DC link capacitor.
- DC-AC inverter which contains four switching elements (e.g. IGBTs)
- DSP which includes the PWM software algorithm and controls the switching elements through a specific driver.
- Passive low pass filter (LPF).

The heart of a frequency converter is the PWM algorithm, which is embedded in the DSP. The output signal quality depends on the PWM switching scheme parameters and type. Unipolar PWM switching scheme with triangle carrier frequency has more advantages among other PWM schemes; such as less THD, duplicate the switching frequency without increasing the switching power losses and it has acceptable implementation complexity [10,11,12,31,32,33,34].

To generate a unipolar PWM signal, two sinusoidal signals (desired output) have to be compared with a triangle carrier frequency (switching frequency), the result is a voltage pulse with variable width proportional to the amplitude of sinusoidal signal. In the ideal case the switching has to occur simultaneously with the intersection points between the sinusoidal and triangle signals, this is known as Naturally Sampled PWM (NS-PWM). On the other hand, practically the sinusoidal signal is stored as samples in the DSP memory, sampled sine signal instead of analogue continuous one has an influence on the signal output quality, especially the THD and the filtration of the background noise, thus it has been considered as a different switching scheme (Regularly Sampled PWM /RS-PWM)[10], RS-PWM is the conventional method of implementing the naturally sampled unipolar PWM [11,31,34,35], more details are given in clause 2.5.

Different methods and researches were done to eliminate the harmonics and background noise of PWM converters such as:

- designing an enhancement cascade closed-loop control structure to reduce the THD[8,16].
- controlling the pulses timing in order to eliminate harmonics especially with low switching frequency (<500 Hz)[15,19,20,21]
- adding shielding layers on the test transformer's windings in order to reduce the common mode electromagnetic interference and thus the background noise in PD measurements.[17]
- optimization of the inverter operating parameters.[22]
- modifying the methods and the tools of PD measurements[23].

In spite of complexity of some of these methods, the background noise is still high (few 10s of pC), and the THD problem is not completely eliminated(roughly 3.5%) [8,16,15,19,20,21,17,22,23].

In addition, these methods are applied for conventional frequency converters, but in this work the new Pec-HV is able to perform signal preconditioning and to generate a controllable harmonics.

1.1.4 Generation of harmonics

Recently according to technology progress, nonlinear loads in electrical power system are increasing. Nonlinear loads are the main harmonic sources in the electrical grid. As a concept, generation of power harmonics in lab is required in several tests investigations and in researches, for example to test its effect on electrical apparatus[37], or for equipments immunity to harmonics tests[IEC-61000-4-13], as well as it is also helpful to perform PD measurements in nearly real circumstances, and recently used to develop a new techniques for on-line PD measurements[3].

PD measurements are made in the labs with nearly pure signals. Nevertheless, harmonics are present in real installations and may influence the PD behaviour of the high voltage insulation. In order to investigate this influence a sources is needed which is able to generate intended controllable(amplitudes/phase shift) harmonics.

A combination of arbitrary signal generator and power amplifier or HV-amplifier are used to generate the required harmonics[54,37]. The main disadvantages of using amplifier in order to generate harmonics are the relative low power efficiency (roughly 90% in best cases) and limited output power to few kW [36,38].

1.2 Requirements of a power electronic control device for high voltage test transformers

As shown above the solutions available in the market or described in the literature are individually designed for specific application fields. Typically they can not be used for another application. There is so far no holistic solution. Therefore this dissertation aims to the realisation of a holistic approach. The contributions of this dissertation and the goals for the device are:

- Signal preconditioning: Based on a new unipolar PWM algorithm. The new PWM method is enhanced to generate harmonics(En-Unipolar-PWM). With these new features it is possible to perform the signal preconditioning process in order to accomplish the HV tests in nearly ideal conditions. That can be done by manually¹ changing the En-Unipolar-PWM algorithm's parameter in order to compensate the harmonic distortions, thus having a clean signal (THD 0.5%).
- Fast switching off the applied voltage: A new switching-off topology based on the PWM inverter switching elements(H-bridge IGBTs) which reduces the hardware complexity is presented. Furthermore the detection breakdown process is

¹at the moment, further development can be done in future.

improved to be faster and reliable based on voltage fall time and current raise time.

- High quality output: In order to have a pure sinusoidal signal for HV-DI tests or PD measurements, the signal has to be free from low order harmonics (frequencies below 2 kHz) and acceptable filter complexity/cost for high frequency region (100 kHz to 500 kHz). That is achieved by bridging the gap between the regularly sampled and naturally sampled PWM (Ideal case), thus eliminating the low order harmonics and reducing the filtration complexity of the background noise. The new Enhanced Unipolar PWM algorithm based on calculating the intersection points between the desired and the carrier frequencies using programmed Matlab model. According to the mentioned intersection points the PWM signal duty-cycle values are calculated. The outcome, which is actually a duty-cycle values, are stored in the DSP memory, multiplying the duty-cycle values with a factor will control the output voltage amplitude, while the time of processing each duty-cycle value will determine the desired output frequency (16,7 Hz, 50 Hz, 60 Hz).
- Generation of intended harmonics: The power electronic control device for high voltage test transformers (Pec-HV) is able to generate intended harmonics for lab investigations, these harmonics (3rd and 5th) are fully controllable; phase-shift and amplitude. Intended harmonics are generated based on the Enhanced Unipolar PWM algorithm (explained in previous paragraph), where the duty-cycle values of the fundamental frequency and the intended harmonics are added together (simplified concept) to generate the wanted harmonic. The challenge is to keep the real measured THD close to the desired one, and to keep the background noise around 1 pC. A Matlab model is used for optimizing the En-Unipolar-PWM parameter such as the dead time and switching frequency to achieve the desired goals. The difference between desired THD and the measured in case of intended harmonics generation is $\pm 1\%$ and the background noise remains below 1 pC. Furthermore the generated harmonics can be employed eliminate the dead time problem in the unipolar single phase PWM inverter.

2. Conceptual Framework of controlling HV test transformers

2.1 General

AC high voltage test quality is the major interesting point in this research. Beside other issues, the test quality depends on the test's voltage source. The purity of the test source signal and its ability to compensate the generated distortion by the test transformer's iron core are the two main challenges. Since the used voltage test source in this research is a DC-AC inverter (the developed Pec-HV), the implemented PWM switching scheme will influence the quality of Pec-HV.

In order to achieve the goals of this research (clause 1.1) the effort is focused on the PWM switching schemes starting from choosing the best PWM method from quality point of view (less THD), and then filling the gaps in the selected PWM scheme to get the optimal quality and to enhance it to generate intended controllable harmonics to support the required Pec-HV features and functionality. Figure 2.1 shows the area of this research which is focused on the test signal quality.

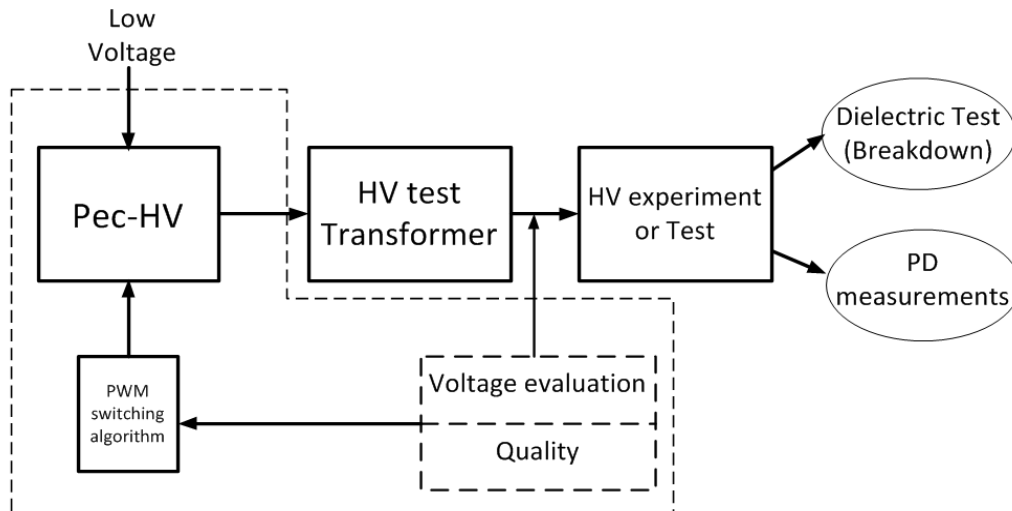


FIGURE 2.1: Pec-HV, Research mainframe

2.2 High voltage dielectric breakdown test

Any electrical system or equipment consists of three main parts: Conductor material, semiconductor elements and insulators. Testing electrical devices or elements is important from reliability point of view. Current flow test can be done to assure the device/element functionality. High voltage test is performed to assure the insulators reliability where the insulation is a significant part of high voltage devices.

Nowadays the dielectric stress to materials can be calculated with the appropriate computation tools. From the understanding of the dielectric behaviour of the material and the mechanism of breakdowns, the maximum permissible electric field strength can be estimated. However, the experience shows that breakdowns are strongly influenced by impurities, local inhomogeneities and surface effects (roughness, dust, humidity). Since these items are hard to implement in calculation models, each high voltage device used in the power grid will be tested (type tests or routine tests) .

Insulators are able to withstand voltages higher than rated until a specified limit, then due to increasing of electric field stress the insulator will collapse and a current will flow through it. That is the basic description of insulator voltage breakdown. The breakdown test can be done by applying a power frequency voltage (50 Hz, 60 Hz, 16.7 Hz) through a step up transformer (up to 100 kV in this work). Two electrodes are connected to the secondary winding of the test transformer, where the tested insulator specimen is fixed, then gradually increase the electric field (Voltage) until a breakdown is detected, and then the applied voltage has to be switched off (see figure 2.2) [42,43,44,1,2].

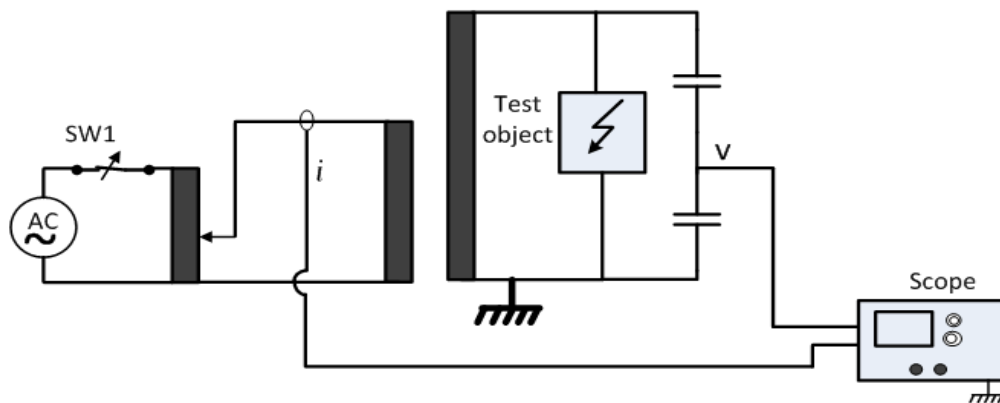


FIGURE 2.2: AC High voltage dielectric test, principle schematic

Figure 2.3 shows a simulated breakdown process of the above shown schematic. Before the breakdown occurs, the transformer's primary current is relatively low (few amps), but after the breakdown where the voltage falls to nearly zero, the current raise up immediately to a destructive values (few hundreds Amps). Detecting the breakdown and switching off the applied voltage very fast is a significant issue in such test.

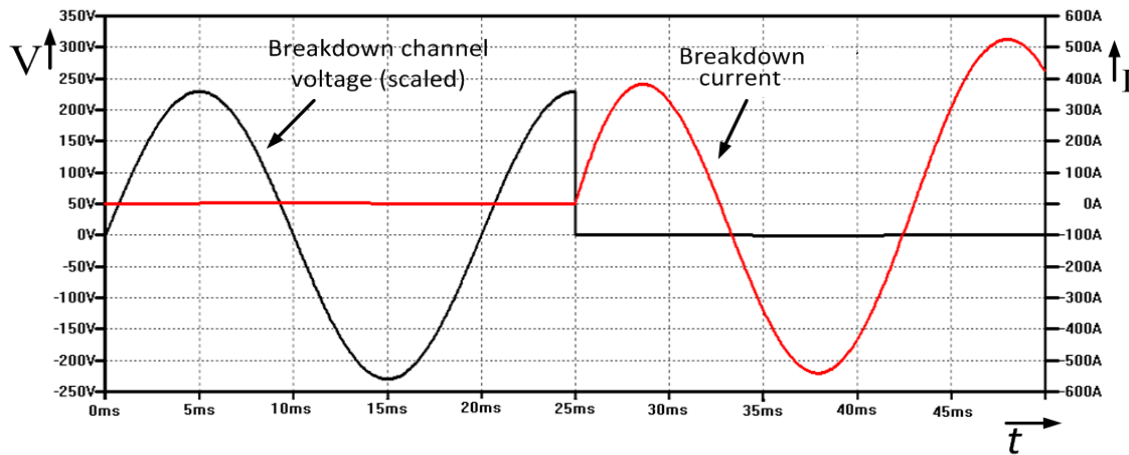


FIGURE 2.3: Breakdown, voltage and current characteristics, the diagram shows the voltage at the output of HV divider and the primary current

In this study, The experimental investigations were done using two spheres as electrode, and the air as an insulating material. The new device (Pec-HV) has the ability of interrupting the applied voltage within roughly $50 \mu\text{s}$ in case of breakdown. The device also allows a lab dielectric breakdown tests with a pure voltage sinusoidal signal as well as with different power frequencies and an optional generated intended harmonics in order to investigate a real conditions where the harmonics are present in the power grid.

The well known theories of Townsend mechanism and Streamer mechanism describe the behaviour of charged gaseous particles under the influence of electric field and how that leads to gaseous breakdown. For simplicity, gaseous breakdown can be explained as shown in figure 2.4, where the three main steps are [42,43,44]:

1. Ohmic behaviour
2. Saturation: That will occur if all charges produced by radiation (influence of high electric field) are used for current transport.
3. The current will start to flow between the electrodes (avalanche) which leads to the insulator breakdown.

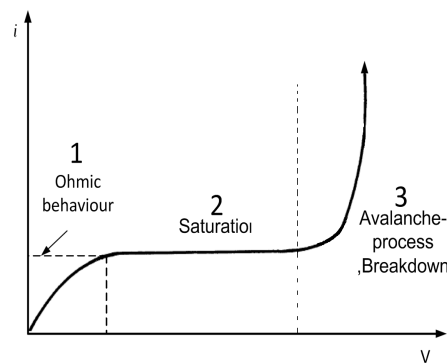


FIGURE 2.4: Insulator Breakdown process

2.3 Partial discharge measurements

The best definition for Partial discharge is from the International standard (IEC 60270)[45] “Partial discharge (PD) is a localized electrical discharge that only partially bridges the insulation between conductors and which may or may not occur adjacent to a conductor ”

PD could occur :

- Between sharp edges and ground, where high voltage is applied toward the ground in gaseous media , which is known as corona discharge(figure 2.5).
- Internal in cavity or voids inside insulation material(normally in solid) ,which is known as cavity discharge. If the electric field steers is continuous, it could be worse and more PD will form a tree discharge(Figure 2.6) which leads to voltage breakdown and damaging the insulator.
- At the boundary of different insulating material, which is known as surface discharge.

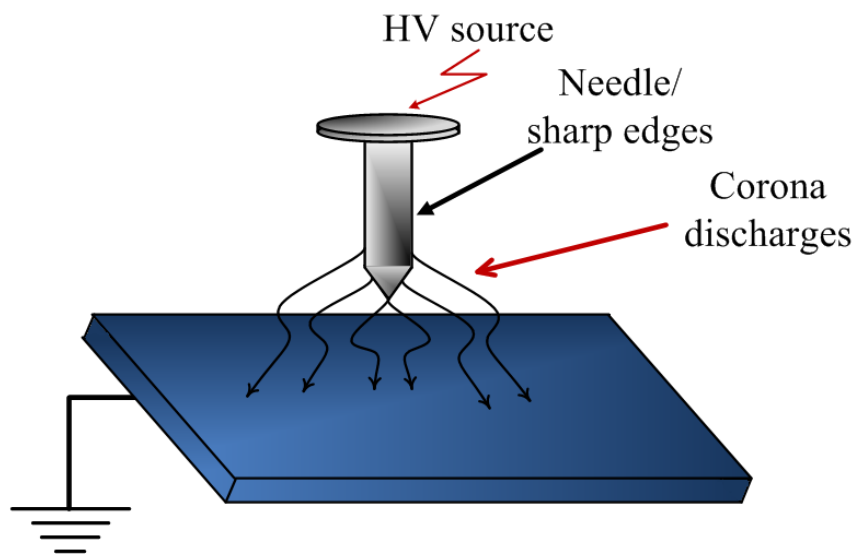


FIGURE 2.5: Corona discharges between sharp edges and ground

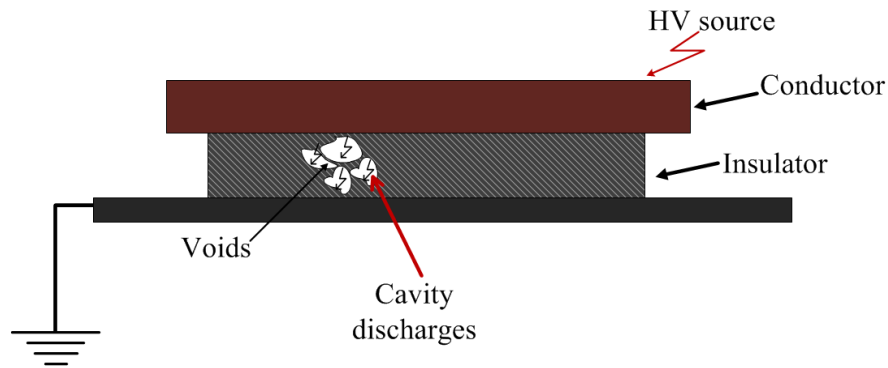


FIGURE 2.6: Cavity discharge

So PD occurs due to high stress electric field on insulators where high voltage is applied. These discharges appears as small voltage dips(pulses) in a range of few millivolts as amplitude and a few nanoseconds as width. Thus a conventional voltage or current measurement devices are not able to measure PD pulses. That is why a special device is needed.[45,44,17,57,56]

Figure 2.7 shows one of the common circuits which is used to measure PDs. A coupling capacitor is connected in series with a coupling device, where both are in parallel to the tested object. The coupling device contains a passive element (R,L,C) which has relative low impedance (roughly 100Ω or less). The coupling device and the capacitor also work as high pass filter. The connecting cable between the coupling device and the Measurement Instrument (MI) could be an optical fibre or a coax cable.[45,44,55]

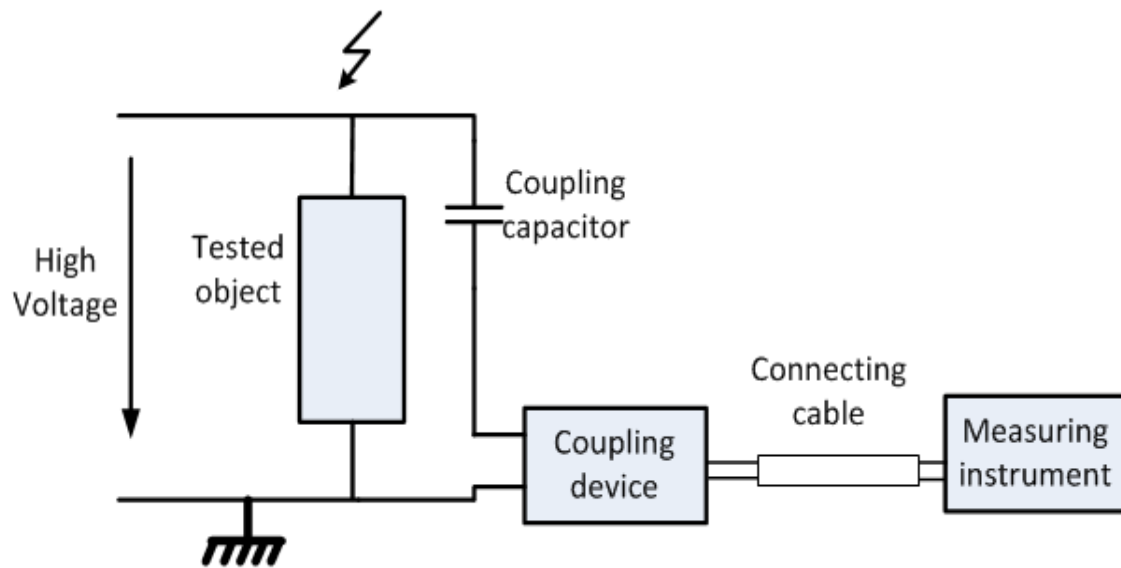


FIGURE 2.7: PD measurements test setup

The PD current pulses is detected by the MI and analysed by two methods:

1. Integration along the pulse boundary in time domain: The PD is a narrow current pulse (few nano seconds), where the integration of the current pulse is the charge q which is expressed in pC. Figure 2.8(a).

2. Integration of PD in frequency domain: Since PD's are narrow in time domain, they have a wide band in frequency domain. Where the charge q is equal to Q_{FD} at ($f=0$). Due to flat spectrum, measurements can be made in high frequency range. Figure 2.8 (b).

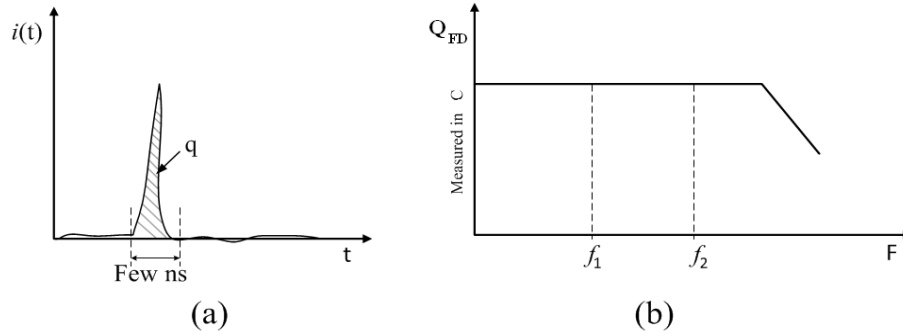


FIGURE 2.8: (a) PD pulse in time domain (b) PD pulse in frequency domain

Band pass filter is needed to limit the measurements bandwidth. The international standard IEC60270 [45] has determined the recommended values for wide band PD measurements as the following:

- $30\text{kHz} \leq f_1 \leq 100\text{kHz}$
- $f_2 \leq 500 \text{ kHz}$
- $\Delta f = f_2 - f_1$: where $100 \text{ kHz} \leq \Delta f \leq 400\text{kHz}$

The typical spectrum of unfiltered PWM converter is as shown in figure 2.9, where the highest magnitude is for the fundamental desired frequency followed by the switching frequency (carrier frequency), the side-band frequencies are appear as multipliers of the switching frequency, since the recommended switching frequency is 2 kHz to 20 kHz, the sided-band frequencies will appear in the range of (2 kHz to 1 MHz) depends on the amplitude and frequency ratios between the carrier and the desired signals(details are explained in clause 2.5.2.2). As a consequence to that an interference with PDs is predicted.

The PD-MI works at a high frequency range as mentioned before(f_1 and f_2) and the PD patterns are evaluated in parallel with time domain (phase angle) to identify the type of PDs[44,57,55]. Taking in account that the typical frequency converters synchronise the carrier with the sine signal(desired), therefore the PWM switching time points appear at constant phase angles, thus the PD-MI has no chance to discriminate the signal from PWM switching, neither in frequency nor in time domain.

The interference appear as background noise in PD-MI. The IEC standard[45] puts a limit that the background should be less that 50 % of a specified permissible PD magnitude. The allowed PD magnitude depends on the insulator materiel which ranges between (2 pC to 500 pC) [58]. In order to fulfil this requirements for various types of insulators, the background noise has to be less than 1 pC.

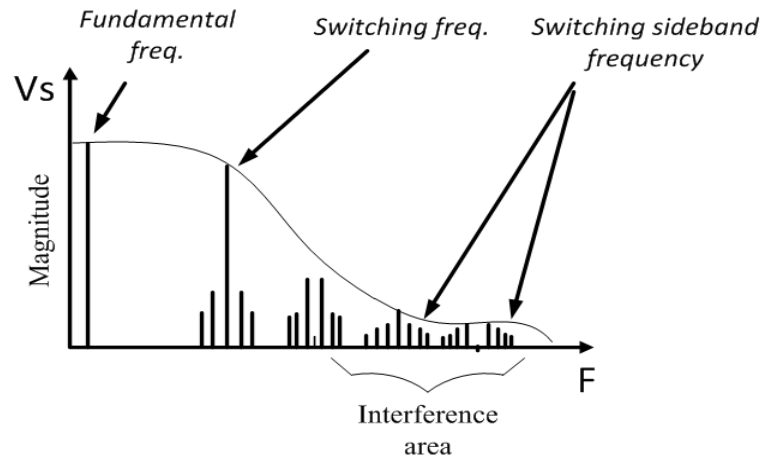


FIGURE 2.9: Typical spectrum of an unfiltered PWM frequency converter

In order to eliminate this interference the PWM output voltage has to be filtered with a proper attenuation ratio, especially for the bandwidth (100 kHz to 500 kHz). The PWM harmonics magnitude in the interference area as shown in figure 2.9 are measured in milli volts. The relation between the two units mV and pC can't have a general formula [56], while it depends on the impedance of coupling between the tested object and MI, but as it is clear from [56] and [61] in addition to lab work experience that the range of PD patterns can be expressed in volt starting from roughly 1 millivolt and less. According to experimental investigations, it is found that 1 pC would correspond to roughly 35 to 5 μ V (magnitude of the PWM harmonics in the interference area). That means, the key of a proper filter design is to attenuate the PWM spectrum in the range (100 kHz to 500 kHz) to be below roughly 5 μ V. Figure 2.10 shows a real PD measurements performed in the ETS lab in case of improper filtering of PWM converter, where the PWM switching side-band frequency interference with PD pattern is obviously clear.

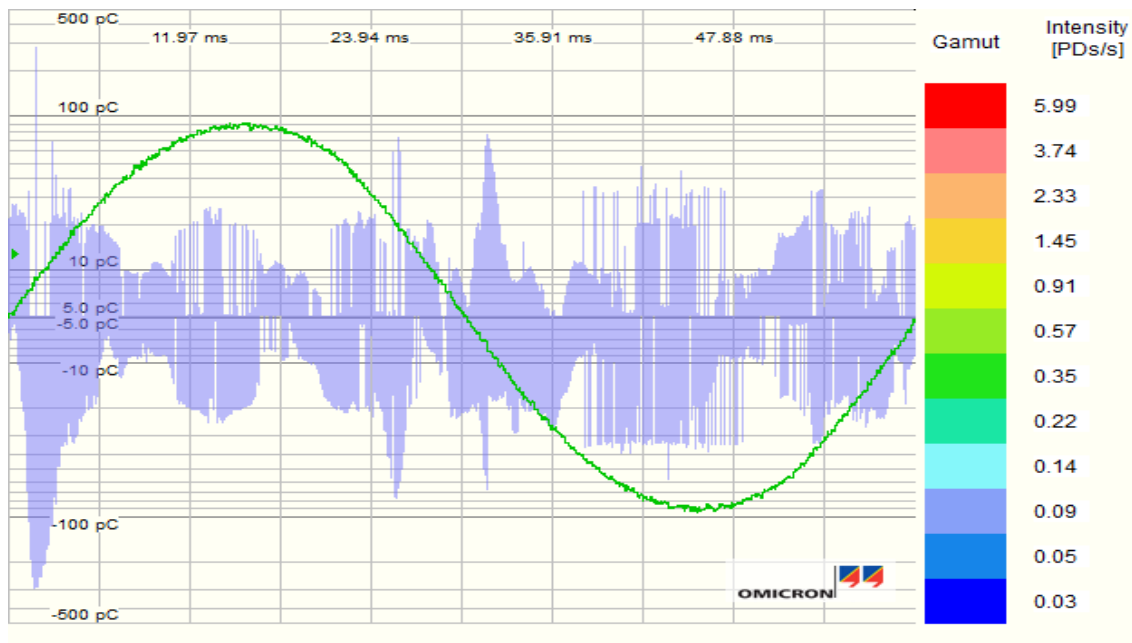


FIGURE 2.10: PD and PWM interference

2.4 HV Test Transformers and Harmonics disturbance

2.4.1 Harmonics

Harmonics in an electrical power systems are an integer multiplier frequencies of a fundamental voltage power frequency. Harmonics are distortions which are caused by nonlinear loads in the electrical power grid, such as switch mode power supplies, AC-DC rectifier, converters, inverters and transformers. In linear loads if the voltage is pure sinusoidal, the current must be sinusoidal as well with/without phase shift. Unfortunately the current is not sinusoidal in nonlinear loads, it is distorted. These current distortions will influence the voltage source due to the impedance of the mains by adding harmonics to it. Since the current is a symmetrical odd function, the expected harmonics is only odd. Figure 2.11 shows an example of 3rd and 5th harmonics with 40% of the fundamental (50 Hz) amplitude.

The total harmonic distortion factor is measured by calculating the square root of summation squares of harmonic amplitudes divided by fundamental frequency amplitude. as shown in equation 2.1 below.

$$\text{Total harmonic distortion THD} = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \dots V_{49}^2}}{V_1} \quad (2.1)$$

Where V_3, V_5, \dots is the harmonics amplitudes and V_1 is the fundamental frequency voltage amplitude.

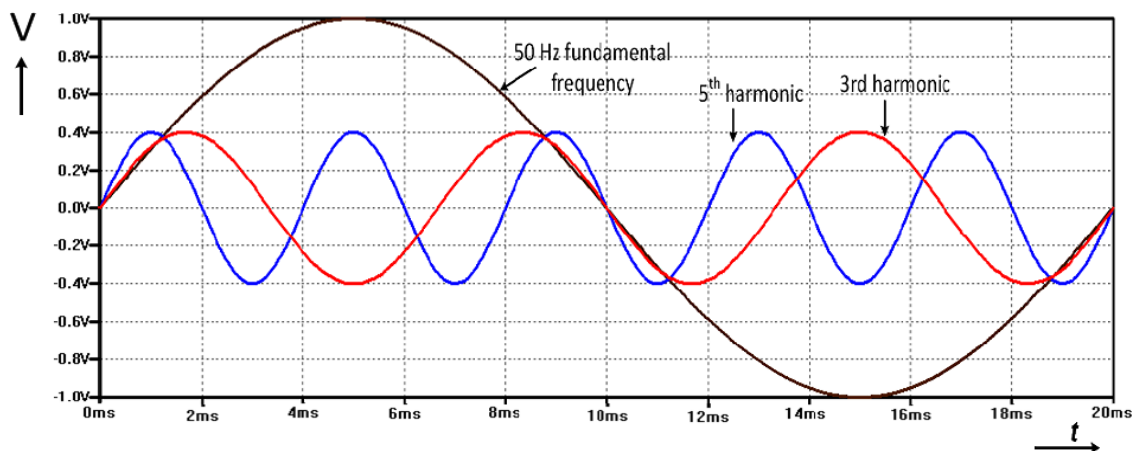


FIGURE 2.11: 3rd and 5th harmonics of 50 Hz power signal

Harmonics are extremely undesired in electrical network. They adversely influence on the electricity producers and customers as well. The elements and devices in electrical network are designed to work with a power frequency of 50 Hz or 60 Hz, higher frequencies current like harmonics will increase the conductor power losses (I^2R) due to the additional current frequency components (harmonics). Moreover they

change the load impedance(increasing in case of inductive load, or decreasing the in case of capacitive load). Thus harmonics have different effects depending on the device which is exposed to them, but in general harmonics (if not eliminated) can over heat the devices[58]. They must be mitigated, otherwise they may cause damage to the electrical system.

In AC high voltage tests such as dielectric Test and PD measurements, the international standard requirements (IEC 60060-1 2010) for the test-source voltage signal is to be sinusoidal, a small deviation from sinusoidal is accepted if ratio of peak to r.m.s. values equals $\sqrt{2}$ within $\pm 5\%$, and the THD has to be taken in account too. The IEEE standard for High-Voltage Testing Techniques[2] put a limit for the THD to be less than 5%.

In practice these requirements are difficult to fulfil in some cases and the standards limits values can be exceeded. That is due to the following :

- Harmonics are presence in the voltage test source whether it is from mains 50 Hz or conventional frequency converters.
- Test transformers are nonlinear devices, they will increase the THD while they produces extra harmonics in addition to amplifying the voltage source harmonics.(clause 2.4.2 presents the details)

Figure 2.12 shows an example of a real PD measurements, where the standard limits values are exceeded due to the mentioned reasons above.(the voltage source was from mains).

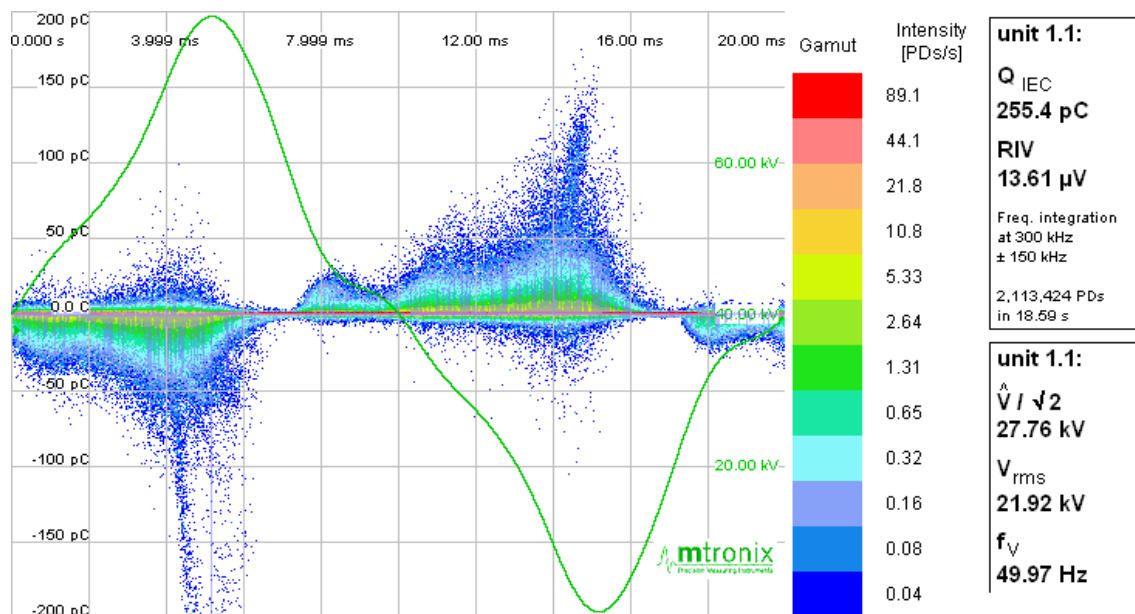


FIGURE 2.12: Highly distorted sinusoidal signal in real PD measurement

2.4.2 HV Test Transformers

Single phase transformer basically consists of two windings on an iron core as in figure 2.13. The physical concept is simple, if an applied voltage change during time (sinusoidal) at the primary winding, the magnetic flux in the core ϕ will be also changing during time. This will induce a current/voltage in the secondary winding.

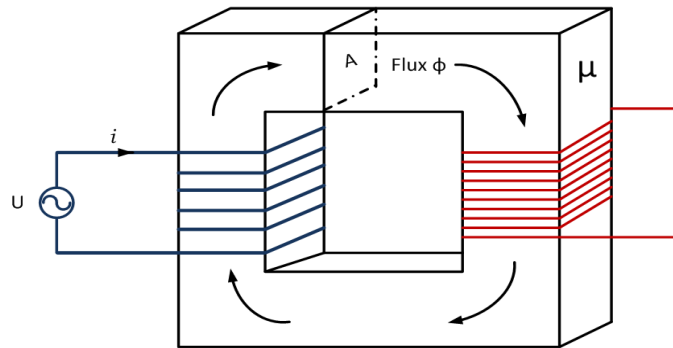


FIGURE 2.13: Single phase transformer

The flux ϕ will flow through the iron core. According to the Faraday's law the induced voltage will depend on the flux changing rate $\frac{d\phi}{dt}$ and number of the coil turns (N).

$$u_p = \frac{d\phi}{dt} \cdot N_p \text{ and for the secondary } u_{sec} = \frac{d\phi}{dt} \cdot N_{sec} \quad (2.2)$$

Figure 2.14 explains the nonlinear behaviour of an iron core. Assuming a sinusoidal voltage u is applied to a coil on an iron core transformer, the flux ϕ is 90 degree shifted. The flux ϕ will start to increase in approximately linear behaviour in time intervals (t_0 to t_1) and (t_1 to t_2) as well as the current i . When the core is nearly saturated (t_2 to t_3), the iron permeability μ is no longer linear as well as the current and the magnetic field H . The induced i is non sinusoidal, it contains harmonics. These current harmonics will go back to the voltage source, the amount of voltage distortion will depend on the source impedance. By applying Fourier series analysis, only odd harmonics will be seen in voltage, since the distorted current is a symmetry odd function.

In high voltage tests where a step up transformer is used to generate a high voltage, the tested objects or measurement instruments are almost have a high impedance, thus the secondary current is normally less than 100 mA. The main current loop is the primary current (few Amps or few 10s Amps) as shown in figure 2.15. This current I_p is a nonlinear due to the nonlinearity of the iron core and contains odd current harmonics which will appear as a voltage drop through the source impedance, thus $V_p = V_s + V_z$ will be induced to the secondary windings and will be amplified with the contained

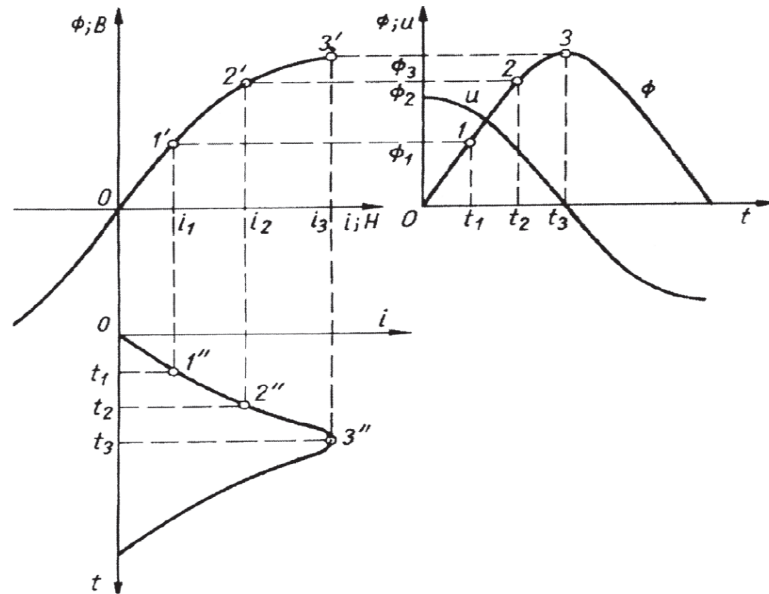


FIGURE 2.14: Non-linearity of iron core[46]

harmonics. This interprets the reasons for a distorted sinusoidal voltage signal in figure 2.12 (clause 2.4.1).

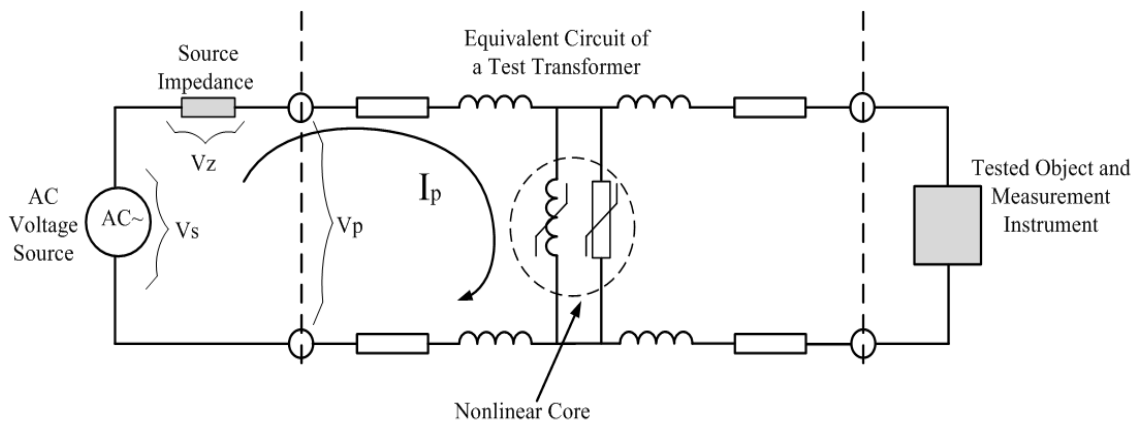


FIGURE 2.15: Nonlinearity-core's effect on the current loop in the Test Transformer

A measurement in lab was setup in a similar way of figure 2.15, where the voltage source is the Pec-HV and a harmonics network analyser is connected to measure the harmonics at V_p . This experiment shows that the 3rd and the 5th harmonics are the dominants. Figure 2.16 show the result of this experiments where the core non-linearity is clear since the THD is 7.1 %, which is more than 5 % in this case, thus a solution has to be found for this problem.

Figure 2.17 shows an examples of high voltage test transformers, where insulation issue is more significant and they should have less flux density within the core to avoid high order harmonics .[47,44].

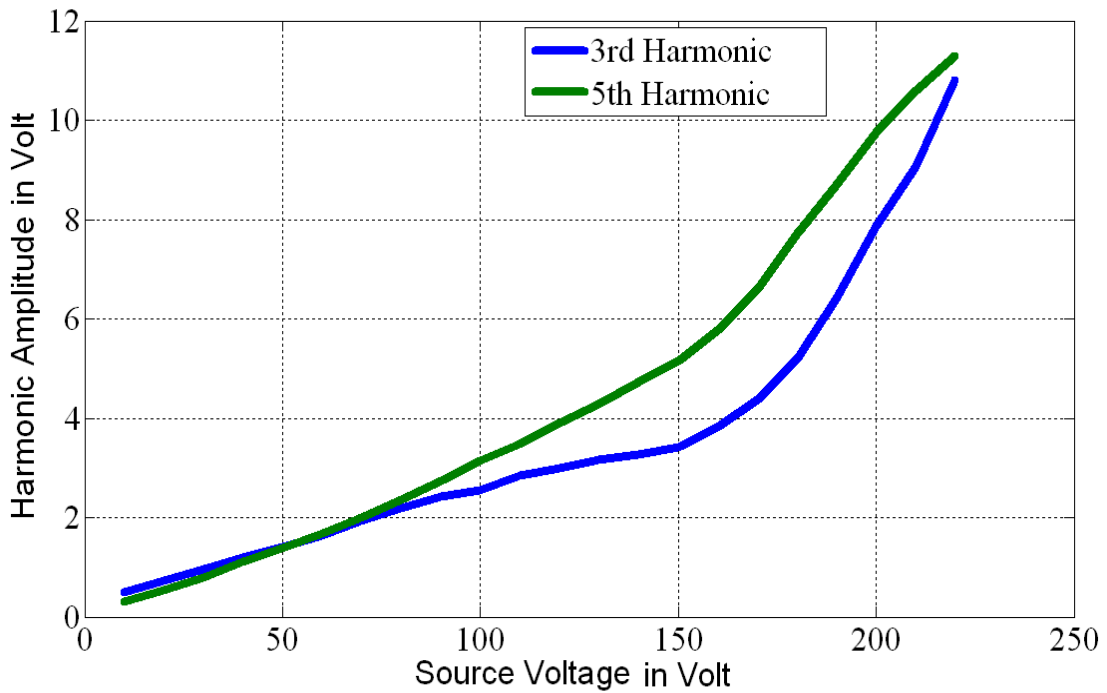


FIGURE 2.16: Measured 3rd and 5th harmonics which are generated due to core non-linearity

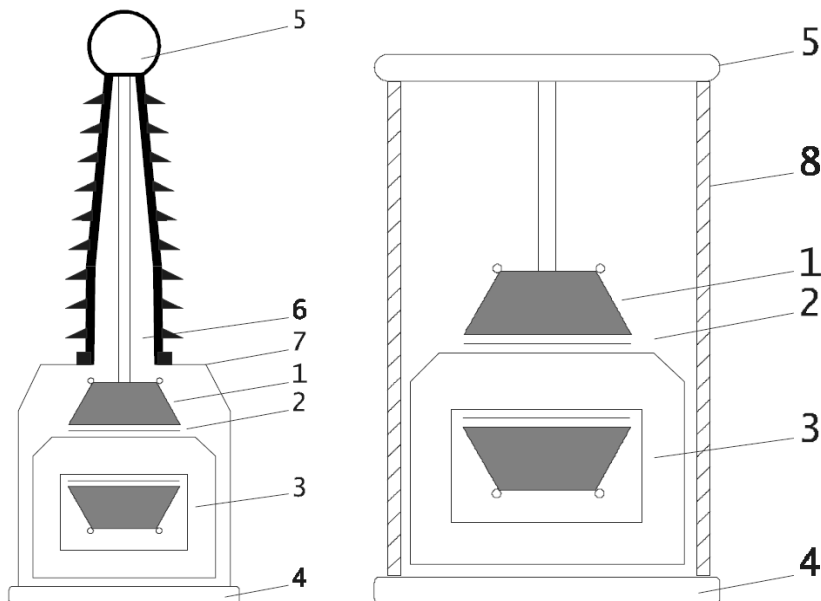


FIGURE 2.17: HV-test Transformers[44](1) Secondary HV winding. (2) Primary winding.(3) Iron core. (4) base. (5) HV electrode. (6) Bushing. (7) metal tank. (8)Insulating tank.

2.5 Single Phase DC-AC Inverter and Pulse width modulation

2.5.1 DC-AC Inverter topologies

The DC to AC inverter is the main part of a static frequency converters. Inverters are used in various applications such as interruptible power supply, AC motor drivers and recently as voltage source for high voltage tests. Figure 2.18 shows a typical block diagram of a one phase static frequency converter which mainly consists of :

- AC to DC rectifier and DC link capacitor.
- DC to AC inverter which reforming a DC voltage to AC through a switching scheme algorithm.
- Low pass filter to smooth the desired output voltage.

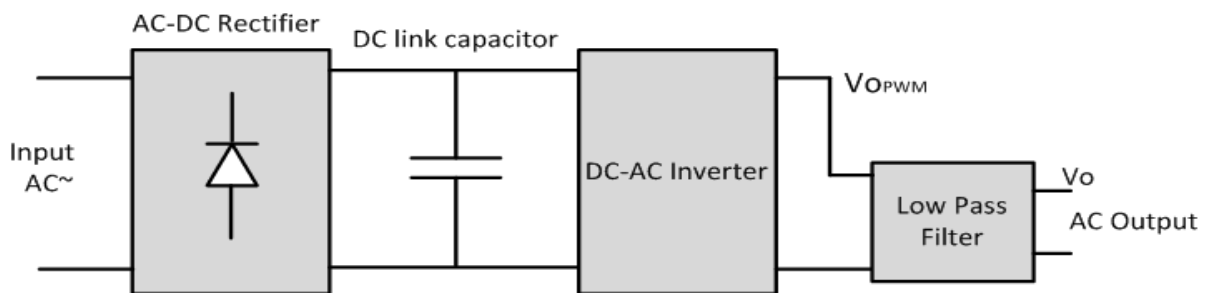


FIGURE 2.18: Block diagram of a frequency converter

The interesting point for this thesis is the inverter's switching algorithms, especially how it can be modified and implemented in order to get a pure clean signal or combined with intended harmonics output which can be efficiently used as a voltage source for HV tests.

The well known inverter topologies are half bridge and full bridge inverter as shown in figure 2.19. Since the full bridge topology is more efficient for real inverters design, it will be adopted in this thesis[10,11,12].

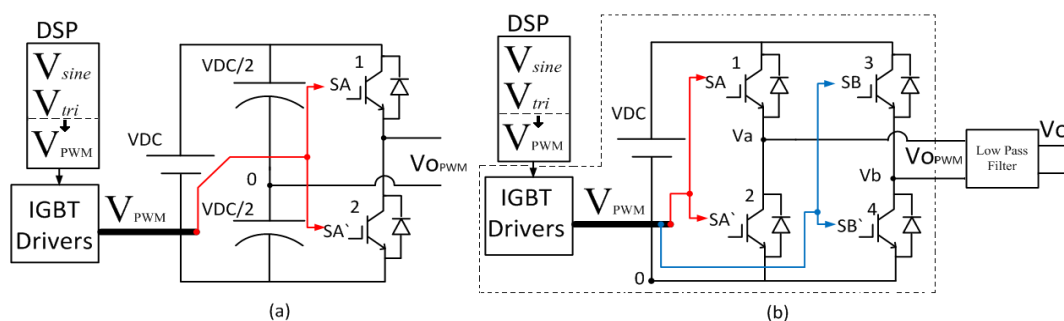


FIGURE 2.19: a) Half bridge inverter. (b) Full bridge inverter

As seen in figure 2.18, the main switching element is an IGBT, it is efficient reliable semiconductor and can be driven with a simple driver circuit. Full bridge IGBTs are available now in advanced complete design including the drivers and a protection circuits, they are well known as power modules (PM). A digital signal processor (DSP) is used to control the IGBTs switching process through an implemented switching algorithm, where a modulation of a desired signal (V_{sine}) and carrier signal (V_{tri}) is executed.

The PWM switching algorithms specifies the inverter's output signal quality and shape. There are many switching algorithms/bridge topologies that can be applied for a full bridge inverters design, some of them are too complex to be implemented for a high level of power (few 10s kW) such as multi stage inverters. Practically bipolar and unipolar PWM switching strategies are efficient, controllable and not complex to be implemented. In this thesis a Unipolar PWM strategy is developed and enhanced to achieve the goals. In the next parts of this clause one can find an explanation about the unipolar concept; starting from the general PWM concept and approaches, and then the half bridge topology with bipolar PWM switching strategy, then the full bridge bipolar PWM, and then the full bridge unipolar PWM .

2.5.2 Pulse width modulation (PWM)

2.5.2.1 Concept of PWM

PWM means a changeable width (Duty cycle) of pulses pattern according to a reference signal. That can be achieved by comparing a reference signal (desired output voltage V_{sine}) with a higher frequency triangle signal (carrier frequency V_{tri}). see figure 2.20.

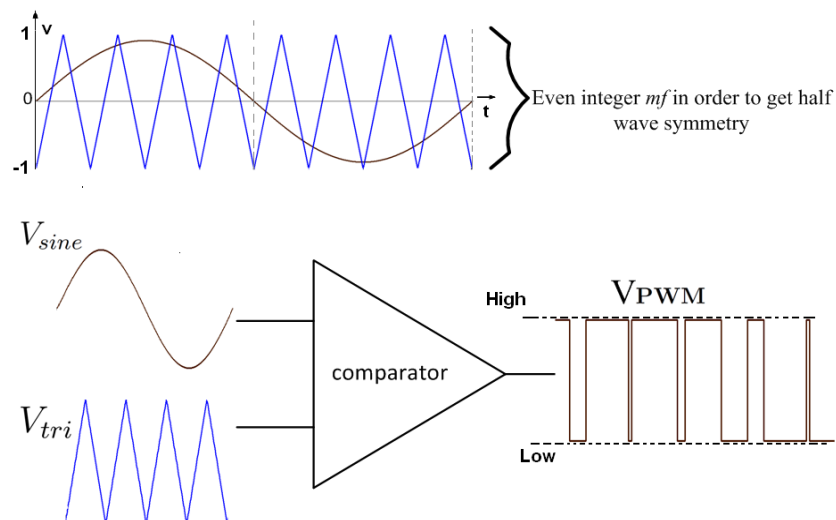


FIGURE 2.20: concept of PWM

The following describes the generation of PWM :

- If $V_{sine} > V_{tri}$ then V_{PWM} is high and when $V_{sine} < V_{tri}$ then V_{PWM} is low.

- The peak voltage of V_{sine} ($V_{p_{sine}}$) should be less or equal to the peak of the carrier signal $V_{p_{tri}}$

$$m_a = \frac{V_{p_{sine}}}{V_{p_{tri}}} \leq 1 \quad (2.3)$$

where m_a is the modulation index.

- m_f is the frequency ratio of the carrier frequency f_{tri} and desired frequency f_{sine} .

$$m_f = \frac{f_{tri}}{f_{sine}} \quad (2.4)$$

- m_f should be an even integer (in case of using Unipolar PWM scheme) in order to get half wave symmetry of the periodic desired output voltage, therefore less harmonics in the total output voltage (V_o) [11,12].
- For optimal system behaviour, in order to produce quality output with less harmonic distortions, V_{sine} & V_{tri} should be synchronised (m_f is an integer) and the modulation index m_a (figure 2.21) should be in the linear region [11,12].

The inverter system will have a linear behaviour if $m_a \leq 1$. Larger m_a values leads to over-modulation case [10,11,12]. As seen in figure 2.21, where $V_{po}(h)$ is the harmonics peaks value of the unfiltered PWM signal (see figure 2.23) and ($h=1,3,5,7,\dots$) is the harmonic order. In case of full bridge inverter; the fundamental frequency at $h=1$, $V_{po}(1)=m_a \cdot V_{DC}$, for the rest harmonics peaks the $V_{po}(h)=nhp \cdot V_{DC}$ where nhp is the normalised harmonic amplitude. More details are found in the next clause.

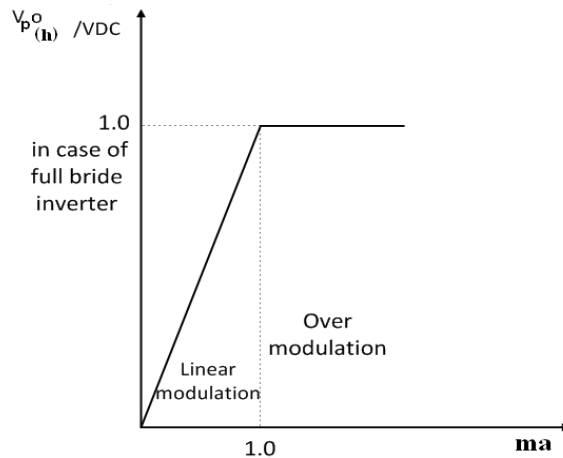


FIGURE 2.21: PWM linear modulation region

2.5.2.2 PWM spectral analysis

Assuming that the V_{PWM} signal (figure 2.20) is fed to the leg A of the full bridge in figure 2.19(b) where V_{PWM} is directly fed to SA and through an inverter to SA'. $V_a(t)$ will have the same characteristics of V_{PWM} but having the VDC value for the high value and 0 for the low value.

In such a system the output voltage $V_a(t)$ is a result of the modulation process of the two signals V_{sine} and V_{tri} , where :

- $V_{sine}(t) = V_{p_{sine}} \sin w_{sine} t$. where, w_{sine} is the angular frequency of the desired output voltage.
- and $V_{tri}(t) = \frac{2*V_{p_{tri}}}{\pi} \arcsin [\sin(w_{tri}t - \frac{\pi}{2})]$. where , w_{tri} is the angular frequency of the carrier triangle signal as shown in figure 2.20.

The well known method to analyse any signal to its frequency components is the Fourier Series, in such system where two periodic functions (V_{sine} and V_{tri}) determine the characteristics of $V_a(t)$, since there is no rotational relation between them, a single Fourier Series is not applicable, therefore a Double Fourier Series method will be applicable to calculate the system spectrum[10,50,51]. This method is used first by Bennett and Black in communication modulation theory[51,10].

Equation 2.5 [52,51,10] shows the general form of Double Fourier Series which has four main parts:

- The first part $\frac{A_{00}}{2}$ is a constant which represents the DC offset value.
- The second part (summation of n's) represents the fundamental frequency and it's baseband harmonics (see figure 2.23) where y is the desired signal frequency which is $w_{sine}t$.
- The 3rd part (summation of m's) represents the carrier harmonics where x is the carrier frequency $w_{tri}t$
- The last part (double summation) represents the sideband harmonics.

$$f(x, y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos ny + B_{0n} \sin ny] + \sum_{m=1}^{\infty} [A_{m0} \cos mx + B_{m0} \sin mx] \\ + \sum_{m=1}^{\infty} \sum_{n=-\infty, n \neq 0}^{\infty} [A_{mn} \cos(mx + ny) + B_{mn} \sin(mx + ny)] \quad (2.5)$$

where

$$A_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \cos(mx + ny) \, dx \, dy \quad (2.6)$$

$$B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \sin(mx + ny) \, dx \, dy \quad (2.7)$$

or

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) e^{j(mx+ny)} dx dy \quad (2.8)$$

In order to solve the Double Fourier Series, it is required to reformulate the system as two dimensional function, where $x = w_{tri}t$ and $y = w_{sine}t$ as in figure 2.22. This method is explained comprehensively in [52,51,10]. The first step is to solve equation 2.8 and to determine the integral limits. To simplify the double integral solving process, the period of the function y will be taken from $-\pi$ and $+\pi$ as well as for x, in this case the integral limits of x are the intersection points between the sinusoidal and triangle (top right-hand side of figure 2.22) which are $\frac{\pi}{2}(1 + ma \sin w_{sine}t)$ and $-\frac{\pi}{2}(1 + ma \sin w_{sine}t)$. In reference [10] the desired signal is taken as general sinusoidal form $ma \cos(w_{sine}t + \theta)$ and the double integral of equation 2.9 can be solved by Bessel function.

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\frac{\pi}{2}(1+ma \sin w_{sine}t)}^{\frac{\pi}{2}(1+ma \sin w_{sine}t)} VDC e^{j(mx+ny)} dx dy \quad (2.9)$$

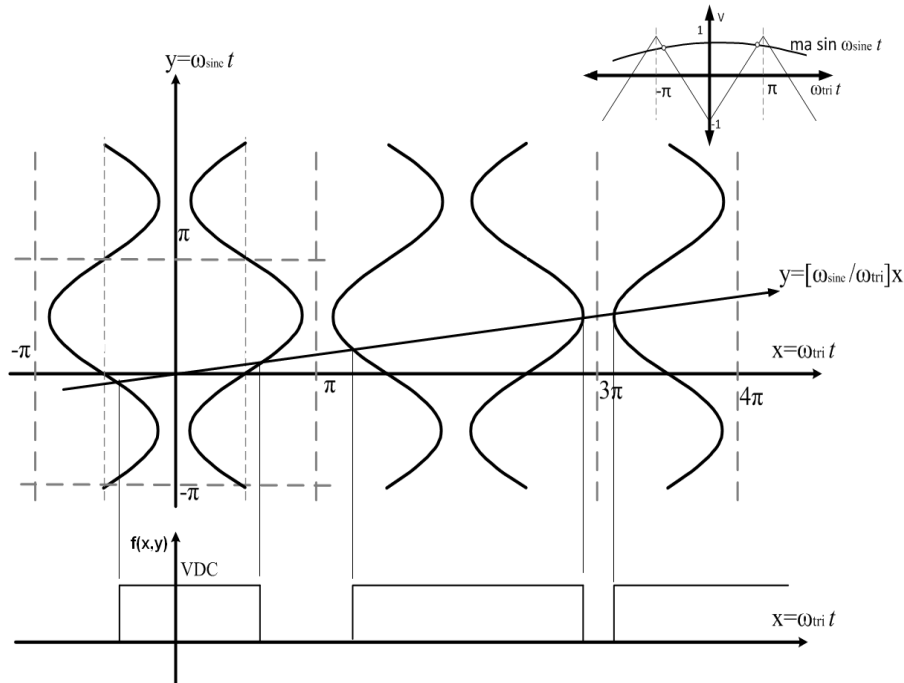


FIGURE 2.22: Reformulated sine-triangle PWM as two dimensional function

As a final result of applying the previous explained method for a full bridge inverter, the PWM spectrum of a sine-triangle function will be as in figure 2.23 [52,51,10]. A generalised spectrum harmonics amplitude values of both Unipolar and bipolar switching schemes are clearly presented in [11], table 2.1 contains a samples of these values.

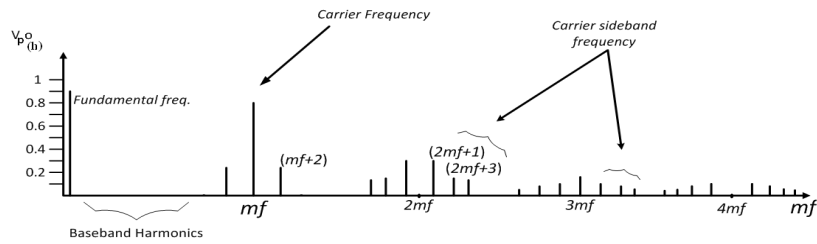


FIGURE 2.23: Spectrum of a full bridge sine-triangle PWM

Harmonic	Generalized amplitude at VDC=1V
<i>fundemantal</i>	0.8
m_f	0.818
$m_f \pm 2$	0.220
$2m_f \pm 1$	0.314
$2m_f \pm 3$	0.139
$2m_f \pm 5$	0.013
$3m_f$	0.171
$3m_f \pm 2$	0.176
$3m_f \pm 4$	0.104
$3m_f \pm 6$	0.016
$4m_f \pm 1$	0.105
$4m_f \pm 3$	0.115
$4m_f \pm 5$	0.084
$4m_f \pm 7$	0.017

TABLE 2.1: Normalised harmonics amplitudes for $m_f > 21$ and $ma=0.8$

From table 2.1 and figure 2.23 the harmonics always appear as the fundamental frequency $h1$, carrier frequency and its sideband frequencies which can be described as the following [52,51,10,11,12]:

$$h = im_f \pm j \quad (2.10)$$

where:

h is the odd harmonic order.

j is even for odd i and vice versa. (i.e $j=2,4,6\dots$ for $i=1,3,5\dots$ and $j=1,3,5\dots$ for $i=2,4,6\dots$)

For example if $m_f=250$, $i=2$ and $j=1$ so $h = 2*250 \pm 1 = 499$ and 501 , if the fundamental frequency is 50 Hz then the harmonic number 499 is at the frequency of $499*50 = 24.950$ kHz and has an amplitude of 0.314 V if $ma=0.8$ and $VDC=1$ V.

The task of the low pass filter in figure (2.19 b) is to filter out these high frequencies and to let the fundamental and the baseband harmonicas (called intended in this thesis) to pass.

In this thesis the desired sinusoidal output voltage will contain an intended 3rd and 5th harmonic. In such case the double integral of equation 2.9 cannot be simplified using the conventional method (Bessel function) [52]. Furthermore in case of exact integer carrier ratio m_f , simulation studies of PWM harmonic investigations using the well known Fast Fourier Transform(FFT) is effective[10]. From this point of view FFT will be used in this thesis to investigate the harmonic content of the Matlab model system which will be explained in clause 3.3 .

2.5.2.3 PWM approaches and implementation challenges

PWM approaches

- Naturally Sampled approach: This approach represent the ideal case(or the so-called naturally sampled PWM), where both signals the desired sine signal and the carrier signal are analogue. In such a case the V_{PWM} signal switching will occur simultaneously with the intersection points between the two signals (V_{sine} and V_{tri}) , see figure 2.24 (a). The analysed V_{PWM} signal in frequency domain will not contain any baseband harmonics[10,40], if a low pass filter is applied to the inverter's output in order to filter out the carrier and its sideband frequencies , then a zero voltage THD at the filter output is expected. Unfortunately that is not the case in real inverters design due to implementation challenges such regular sampled PWM and the dead time effect.
- Regular Sampled approach: In real inverters design a digital signal processor (DSP) is used to generate the PWM signal[31,34,35] , where both signals (V_{sine} and V_{tri}) are digital. The sine signal is stored in the DSP memory as samples, so it will held constant during each triangle cycle. The carrier signal in the DSP is represented by a counter which counts up and down in each carrier cycle, see figure 2.24 (b) . This will create a different switching times for V_{PWM} as if the naturally sampled approach were used. This deviation in time domain will generate baseband harmonics in the frequency domain.[11,10]

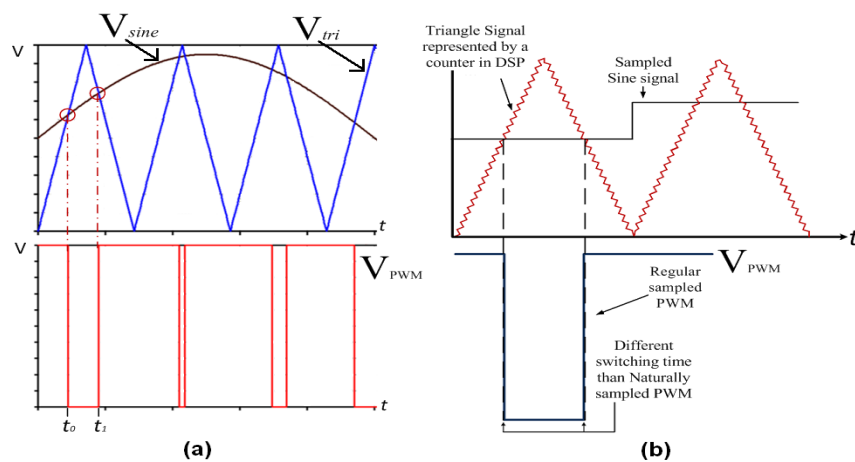


FIGURE 2.24: (a)Naturally sampled PWM , (b)Regular sampled PWM

- Alfa (α) approach: In this approach the corresponding angles of the switching times (i.e t_0 and t_1 of figure 2.24 (a)) of naturally sampled PWM will be calculated and stored in a DSP to generate a clean baseband PWM signal or intended harmonics in baseband area. This method is explained separately in clause 2.5.4.1.

Dead Time

Dead Time (d_t) means a delay time between switching the two IGBTs which are working inversely as seen in figure 2.25, where a delay time is generated at the raising edge of SA and SA'. This delay can be generated optionally by the DSP, the main point is to generate a waiting time until the switching process of an IGBT is completed, then to switch the complementary IGBT. That is important to avoid any high current through both IGBTs during switching, the delay time must be equal or larger to the IGBT switching on or off time (the typical value from data sheet is roughly $2 \mu s$).

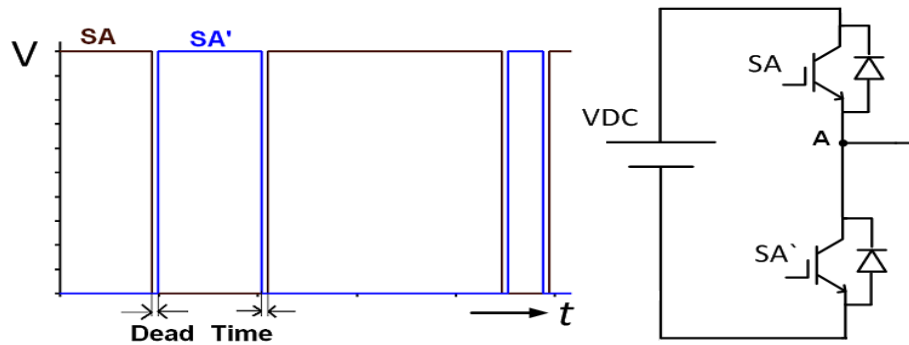


FIGURE 2.25: Dead Time between two complementary IGBTs

The voltage error due to the dead time distortions is proportional to the switching frequency f_{tri} , the dead time d_t and VDC [49]. In [49] the modulation index m_a whether it is ignored or accepted as 1, in addition to that it has been mentioned in [60,48] that the voltage error is inversely proportional to the modulation index m_a . Thus the complete description for the dead time voltage error is the following :

$$\text{Dead time voltage error} = \frac{f_{tri} * d_t * 2V_{DC}}{m_a} \quad (2.11)$$

The Matlab model which will be explained in chapter three is used to illustrate equation 2.11 by the following example :

Assuming a unipolar PWM switching scheme has the following parameters; $m_a=0.4$, $d_t=0$, $f_{tri} = 800 \text{ Hz}$, $V_{DC} = 300$, V_{sine} & $V_{sine}' = 50 \text{ Hz}$, in this case the fundamental output voltage V_{O_p} is 119.7 V . If the same system has a $2\mu s$ dead time, then the fundamental output voltage V_{O_p} is 117.4 V , that means the voltage error is 2.3V, which is in good agreement with the results (2.4 V) if equation 2.16 is used for the calculation.

Many solutions such as using extra hardware elements or applying the control theory to design a control loop are applied to eliminate/compensate the dead time distortions [32,48,49]. In this thesis it will be eliminated by the concept of intended harmonic generation, more details will be shown in the next chapter.

2.5.3 bipolar Pulse width modulation

As mentioned before half bridge with bipolar strategy inverter(refer to figure 2.19 a) is the simplest one. The aim is to get a sinusoidal output voltage with predetermined frequency. Figure 2.26 shows how to generate the V_{PWM} signals (SA and SA') by the DSP, to simplify the explanation the naturally sampled PWM approach is adopted. The desired sine signal V_{sine} is compared with the carrier V_{tri} , as a result the signal SA is generated, and then by inverting SA the signal SA' is generated. Feeding the signal SA through the IGBT driver to IGBT 1 and the signal SA' to IGBT 2 will let the output voltage V_{OPWM} to switches between $V_{DC}/2$ and $-V_{DC}/2$. Filtering the signal V_{OPWM} by a Low Pass Filter(LPF) will get out the desired signal V_o as seen in figure 2.27.

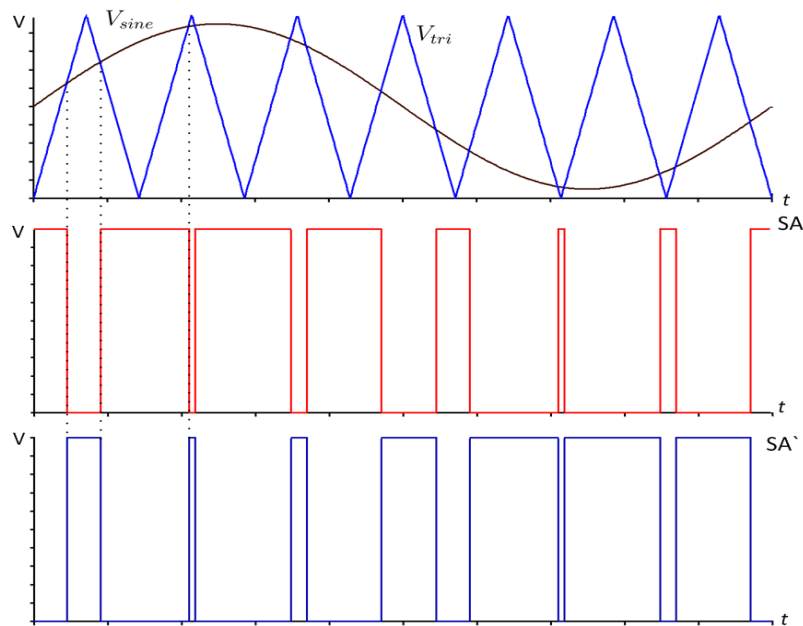


FIGURE 2.26: Half bridge switching scheme, $m_a = 0.9$ and $m_f = 7$.

In half bridge case the maximum peak voltage of the filtered V_{pwm} (V_{Op}) is half of the VDC at $m_a=1$. This is the main disadvantage of half bridge inverter.

$$V_{Op} = \frac{V_{DC}}{2} m_a \quad (2.12)$$

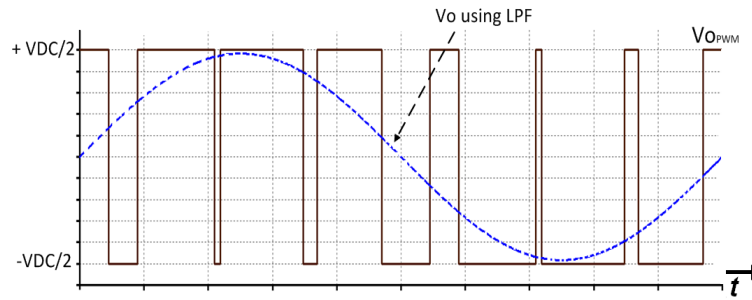


FIGURE 2.27: Half bridge voltage output

In order to increase the inverter output peak voltage, so it can reach the value of the input V_{DC} , another output stage is added to build a full bridge one phase inverter. As in figure 2.28, the bipolar full bridge switching scheme can be achieved if :

- SA is fed to IGBT 1 & 4 .
- SA` is fed to IGBT 2 & 3.

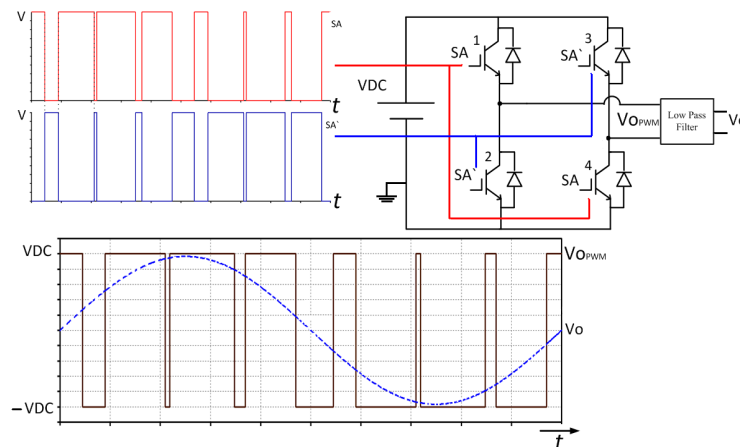


FIGURE 2.28: Bipolar PWM full bridge inverter

In this case the amplitude of the low pass filtered output voltage V_{o_p} is:

$$V_{o_p} = m_a * V_{DC} \quad (2.13)$$

2.5.4 Unipolar Pulse width modulation

Unipolar PWM strategy (only applicable for full bridge topology) can be achieved by comparing the carrier frequency V_{tri} with two sinusoidal signals which have 180° phase shift between them, these two signals represent the desired output frequency. The results from a simple LTspice simulation visualise this modulation scheme with $m_a=0.9$ and $m_f=8$ ($V_{sine}=50$ Hz) as an example. The naturally sampled PWM approach is adopted for simplicity (Figure 2.29).

Figure 2.29 consists of four parts:

1. Two signals of the desired output frequency are 180° out of phase (V_{sine} and V_{sine}') are compared with the triangle carrier frequency V_{tri} .
2. As a result of comparing V_{sine} with V_{tri} the SA signal is generated, and by comparing V_{sine}' with V_{tri} the SB signal is generated. SA is generated by inverting SA and as well SB by inverting SB. The four signals controls the switching process of the four IGBTs, where IGBT 1 fed by SA, IGBT 2 fed by SA', IGBT 3 fed by SB and IGBT 4 by SB'.
3. The outcome of the previous switching process is V_{OPWM} , which is actually VA-VB, this subtraction will eliminate some of the harmonics content and doubling the switching frequency [11,12]. The amplitude of the low pass filtered output signal V_o is V_{Op} where:

$$V_{Op} = ma * VDC. \quad (2.14)$$

4. Here one can see the frequency domain of the output voltage V_{PWM} using FFT. In order to be in a good agreement with naturally sampled PWM, the simulation time step is chosen to be 10ns and FFT is applied for 10 sine cycles.

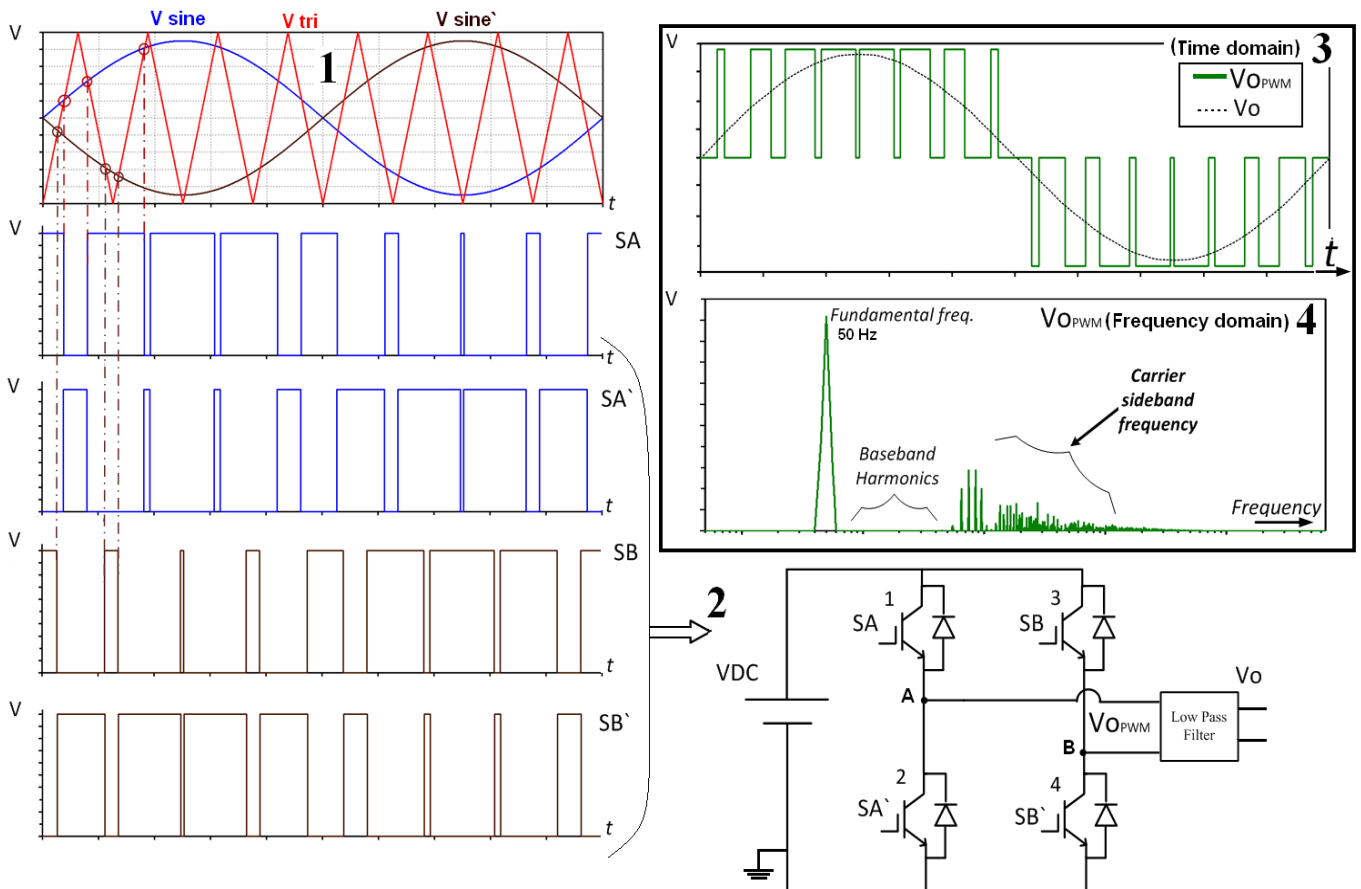


FIGURE 2.29: Unipolar PWM Full bridge inverter

As a Comparison to the previous explained full bridge Bipolar PWM, the full bridge Unipolar PWM has the following advantages over Bipolar PWM:

- Less harmonics content: Unipolar PWM has harmonics only at even multiplier of m_f . [11,12,32,33]
- More power efficiency : IGBT produce the most power losses during the transition on-off or vice versa. Therefore, the higher the switching frequencies the more loss power averaged over time. On the other hand higher switching frequency required to reduce the complexity and cost of the low pass filter . The unipolar PWM strategy doubling the switching frequency at the output V_{pwm} while keeping the switching frequency the same for each IGBT . That is a great advantage for the Unipolar PWM. [11,12,32,33]

That is why Unipolar PWM strategy is adopted in this thesis.

2.5.4.1 PWM Alfa (α) Approach

High quality inverter output voltage signal, free from baseband harmonics or with the generation of intended harmonics is an important issue for this thesis. In the Unipolar PWM, the timing of switching from high to low or vice versa is crucial process. It is the main key which links between the time domain and the frequency domain (harmonics), any deviation in the time of switching (from the ideal case) will yield to harmonics. On the other hand, justifying the timing process of the pulses (time of switching) according to a required frequency domain characteristics (with/without intended harmonics) of Unipolar PWM is the main concept of Alfa (α) Approach.

The following mathematical analysis is come out through an effort which has been put in order to employ the theoretical mathematics for practical solutions for the Unipolar PWM switching scheme [10,11,12,19,20]. To simplify the problem, a Unipolar PWM switching scheme is assumed which has $m_f=8$ and $ma=0.8$, in such a case (figure 2.30) the signal of Unipolar PWM (V_{OPWM}) is quarter-wave symmetry odd function.

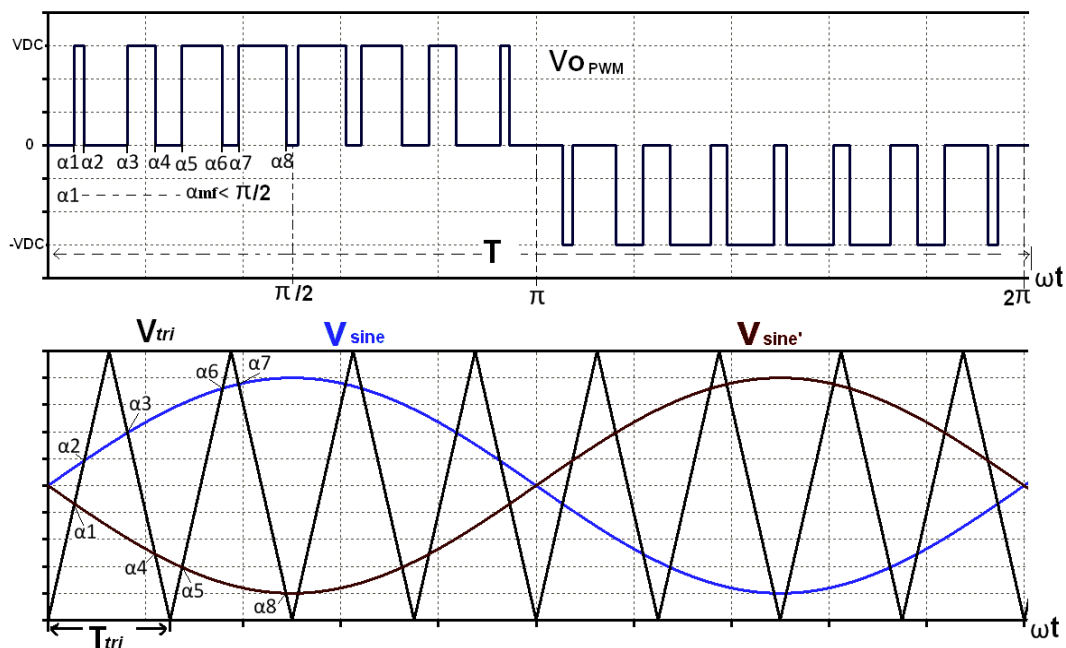


FIGURE 2.30: Analysis of Alfa approach for a Unipolar PWM

The switching angles (α_n or $n\omega_0 t$) are corresponding to the intersection points between the carrier V_{tri} and the desired signals V_{sine} and V_{sine}^* , where :

- $n= 1,2,3... m_f$
- $\alpha_1 < \alpha_2 < \alpha_3 < \dots \alpha_{m_f} < \frac{\pi}{2}$.
- T is one cycle of the V_{OPWM}

In this approach the signal V_{OPWM} will be analysed to its frequency domain components using the well known Fourier Series method, where the general form of Fourier Series is:

$$f(t) = av + \sum_{k=1}^{\infty} a_k \cos kw_0t + b_k \sin kw_0t \quad (2.15)$$

where :

- av is the average DC value $\frac{1}{T} \int_0^T f(t)dt$
- $w_o = \frac{2\pi}{T}$

According to Fourier Series properties, if $f(t)$ (which here $V_{OPWM}(t)$) is an odd quarter-symmetry function then $av=0$ and $a_k=0$, so the function $f(t)$ has to be solved for b_k , b_k is driven for such a function and equal to

$$b_k = \frac{8}{T} \int_0^{T/4} f(t) \sin kw_0t dt \quad (2.16)$$

where T again is the period of the function (figure 2.29) and $k=1,3,7,9...$

Now applying equation 2.16 for the $V_{OPWM}(t)$ where $\alpha_n = tn\omega_0$, and then substitute the result in the general form of Fourier series (equation 2.20), the result can be written like the following form :

$$hv_{(k)} = \frac{4 * V_{DC}}{k * \pi} [\cos k\alpha_1 - \cos k\alpha_2 + \cos k\alpha_3 - \cos k\alpha_4 + \cos k\alpha_5 - \cos k\alpha_6 + \cos k\alpha_7 - \cos k\alpha_8] \quad (2.17)$$

where

- $k=1,3,5,7 \dots 2*m_f-1$.

- hv represent the amplitude of the k_{th} harmonic where hv_1 is the fundamental frequency.
- V_{DC} is the amplitude of the DC voltage source in volt.

The general form of equation 2.17 is

$$hv_k = \frac{4 * V_{DC}}{k * \pi} - \sum_{n=1}^{2*m_f-1} (-1)^n \cos k\alpha n \quad (2.18)$$

where $n=1,2,3,4\dots m_f$

This method is used to eliminate the harmonics from the PWM signal [10,11,12,19,20], For this thesis the main idea is to employ it to determine the amplitudes of the intended harmonics.

From equation 2.18 it is possible to determine the required harmonics amplitudes (hv_1 , hv_3 , hv_5,\dots) by solving the outcome matrix equations in order to find the corresponding α values , where $\alpha_1 < \alpha_2 < \alpha_3 < \dots \alpha_{m_f} < \frac{\pi}{2}$. This condition makes the matrix equations solution only possible by a numerical iterative , therefore the cosine functions has to be rewritten to it's equivalent polynomial functions(nonlinear), the result is new system of nonlinear matrix equation which can be solved by a various methods.

In this Thesis, Levenberg-Marquardt method for solving non-linear equations is used[41]. The system was programmed using Matlab in order find out α values. The numerical iterative process (done by Matlab) takes along time, for example; solving the matrix equations for $m_f=50$ takes around one week. However, higher m_f values means higher carrier frequency, thus less low pass filter complexity and cost. The optimization process, which is important for choosing the optimal filter and switching frequency, required to solve the system for a varied values of m_f . This large consumption of the time makes this system impractical, for this reason this calculation method is excluded and the Naturally Sampled PWM approach is adopted for finding the proper α values . The next chapter presents how the Naturally Sampled PWM is enhanced and employed to serve the theist aims.

3. Pec-HV: switching Algorithm, modelling & simulation, system validation, protection unit and filter characterisation

3.1 Enhanced Unipolar PWM

En-Unipolar-PWM is a new driven switching algorithm which based on the Naturally Sampled PWM, it is enhanced to generate intended harmonics and to overcome the implementation challenges of the Naturally Sampled PWM. It allows the use of DC-AC inverter for HV-DI tests and PD measurements.

3.1.1 Entrance

Assuming that a general sinusoidal signal compared with a carrier triangle signal to generate PWM as in figure 3.1 , where $t_1 t_2 t_3 \dots t_{2m,f}$ are the intersection points of the triangle and sinusoidal functions and T_{tri} is the period of one triangle cycle.

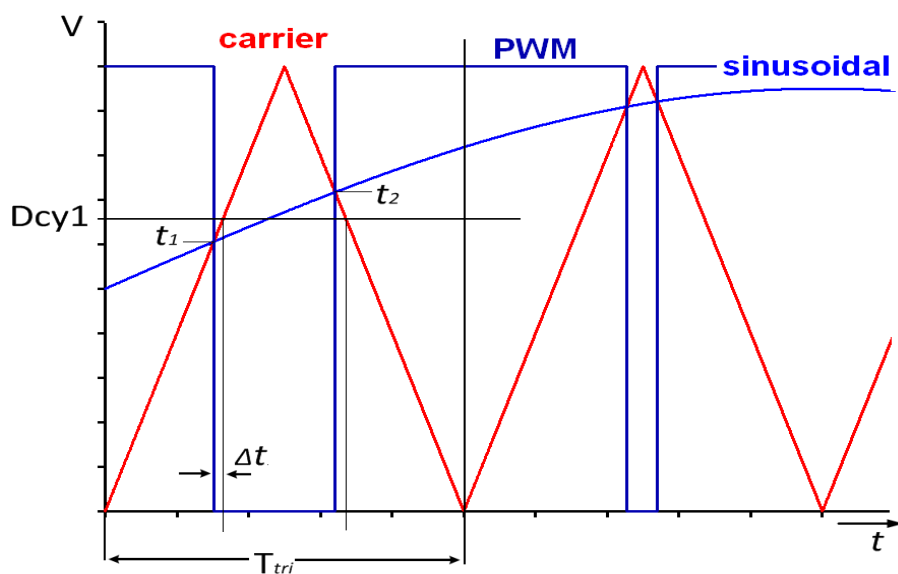


FIGURE 3.1: Concept of the En-Unipolar-PWM

If the intersection points are calculated($\text{Triangle}(t) - \text{sinusoidal}(t) = 0$), then the corresponding PWM duty cycles can be expressed by the following equation :

$$\text{Dcy}(n) = \frac{t_{(2n-1)} + (T_{tri} - t_{(2n)})}{T_{tri}} \quad (3.1)$$

where $\text{Dcy}(n)$ is the PWM duty cycles matrix [$\text{Dcy}(1) \text{Dcy}(2) \text{Dcy}(3) \dots \text{Dcy}(m_f)$] and $n=1,2,3,4 \dots m_f$.

At the implementation level, if the $\text{Dcy}(n)$ is stored in the DSP instead of a sampled sinusoidal, and if a proper DSP with high resolution counter for the triangle signal is chosen(> 1.9 ns in this thesis) , then such a switching scheme can be considered as Naturally Sampled PWM. In this switching scheme, the DSP counter starts counting from zero until its value equals to the corresponding stored $\text{Dcy}(n)$ value and simultaneously switching on/off the PWM signal as seen in figure 3.1. Actually that will lead to a small deviation in the switching time Δt compared with the original t_1 and t_2 , but since both times(t_1 and t_2) are shifted by the same amount (because the carrier is a equal two sides triangle), the duty cycle in the total triangle cycle (T_{tri}) remains exactly the same. If m_f is large enough (roughly $m_f > 30$) the Δt is very small thus this timing deviation can be neglected, therefore the spectrum of this method is in agreement with Naturally sampled PWM. (System validation in clause 3.4.2)

As a backward solution, if the $\text{Dcy}(n)$ values are known and for simplification the values of Δt are neglected, then the corresponding switching time $t_1, t_2, t_3 \dots 2m_f$ can be calculated using the following equations:

$$t_{(2n-1)} = (\text{Dcy}(n) * \frac{T_{tri}}{2}) + (T_{tri} * (n - 1)) \quad (3.2)$$

$$t_{(2n)} = (-\text{Dcy}(n) * \frac{T_{tri}}{2}) + (n * T_{tri}) \quad (3.3)$$

where $n=1,2,3, \dots m_f$

3.1.2 En-Uniplar-PWM Algorithm

En-Unipolar-PWM is an alternative approach for calculating α values, which is overcoming the disadvantages of α approach, especially the time consumption during the solution of the computerized equations. The aim again, is to generate a high quality output signal with exact amplitude of the intended harmonics as well as zero amplitudes, which means zero THD.

The desired signal V_{sine} in this switching algorithm (as seen in figure 3.2) consist of the fundamental frequency V_{sineh1} and a 3rd harmonic V_{sineh3} (as an example, adding more harmonics are possible), since the switching strategy is based on the Unipolar

PWM the signal V_{sine} is required which is also consist of V_{sineh1} and V_{sineh3} , where all of the signals are compared to one carrier frequency V_{tri} .

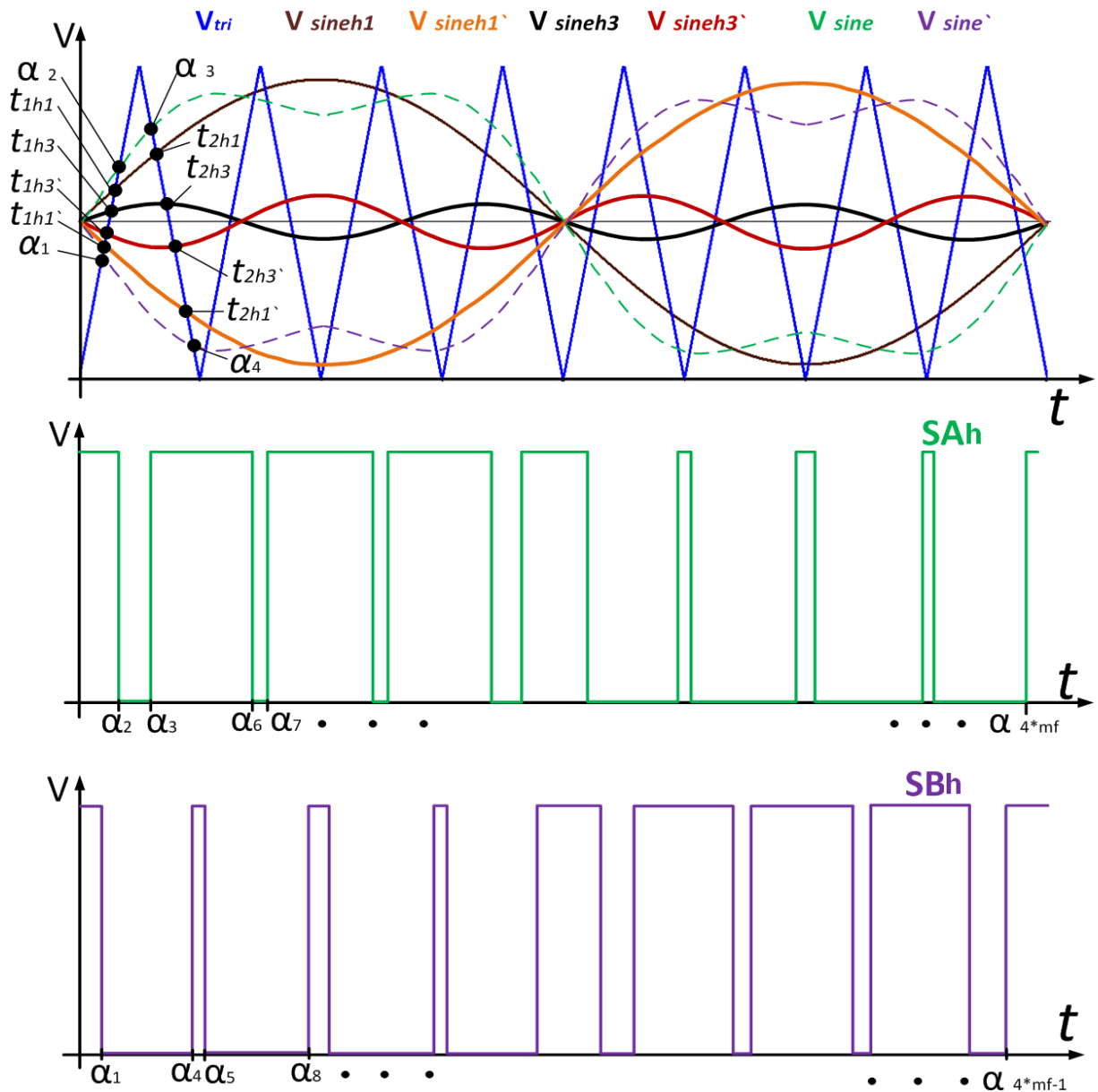


FIGURE 3.2: En-Unipolar-PWM principle

The concept based on the calculation of the intersection points between each of the fundamental frequency and its harmonic signals(V_{sineh1} , V_{sineh1} , V_{sineh3} , V_{sineh3}) and the carrier frequency, then to calculate the PWM duty cycles values according to the calculated intersection points, and then adding the duty cycle values of the fundamental frequency and the 3rd harmonic (again, adding more harmonics is possible) in order to find out α values for the desired signal one has to perform calculation steps as the following :

- Finding the intersection points(t_{1h_1} , $t_{2h_1} \dots t_{2mf_{h_1}}$) of the signals V_{sineh_1} and V_{tri} , and then calculating the duty cycle values Dcyh1(n) using equation 3.1 substituting $t(n)_{h_1}$ instead of $t(n)$.
- Finding the intersection points(t_{1h_3} , $t_{2h_3} \dots t_{2mf_{h_3}}$) of the signals V_{sineh_3} and V_{tri} , and then calculating the duty cycle values Dcyh3(n) using equation 3.1 substituting $t(n)_{h_3}$ instead of $t(n)$.
- Adding the matrices Dcyh1 and Dcyh3, considering that it is not allowed to have duty cycle more than 1 (100%), thus a subtraction of 0.5 (50%) from each duty cycle value of the harmonics is required except for the fundamental frequency. So the total duty cycle is $Dcyh1h3 = Dcyh1 + (Dcyh3 - 0.5)$. As a general Form :

$$Dcyh1h3h5..hi = Dcyh1 + (Dcyh3 - 0.5) + (Dcyh5 - 0.5) + \dots(Dcyhi - 0.5) \quad (3.4)$$

where $i=1,3,5,7..$ the intended harmonic order. The value 0.5 denote to a matrix which has the same length of Dcyhi and all of the elements are having the value 0.5 .

- Substitute the elements of Dcyh1h3(n) in the equations 3.2 and 3.3 in order to find the switching times corresponding to the duty cycles of Dcyh1h3 , the result matrix is $t(n)=[t_1 , t_2 ,t_3 \dots t_{2mf}]$. Amusing that t_k is the odd values of t_n and w_o is the angular frequency of the desired signal V_{sine} then the corresponding α values of the signal SAh are

$$\alpha(4n - 2) = t_{(k)}w_0 \text{ and } \alpha(4n - 1) = t_{(k+1)}w_0 \quad (3.5)$$

where $n=1,2,3,4 \dots \frac{m_f}{2}$ and $k=1,3,5, \dots m_f - 1$

and

$$\alpha(4n - 3) = t_{(k)}w_0 \text{ and } \alpha(4n) = t_{(k+1)}w_0 \quad (3.6)$$

where $n= \frac{m_f}{2} , \frac{m_f}{2} + 1 , \frac{m_f}{2} + 2 \dots m_f$ and $k=m_f + 1 , m_f+3, m_f+5, \dots 2^*m_f-1$.

For example if $m_f=8$, then $t(n)=[t_1 , t_2,t_3 \dots t_{16}]$ and the corresponding $\alpha(n)$ values for SAh are $[\alpha_2 , \alpha_3 , \alpha_6 , \alpha_7, \dots, \alpha_{20} , \alpha_{21} , \alpha_{24} , \alpha_{25} , \alpha_{28} , \alpha_{29} , \alpha_{32}]$

- Applying the explained above bullets for the signals V_{sineh_1} ` V_{sineh_3} ` in order to find out Dcyh1h3 ` and then the signal SBh. The result from substituting Dcyh1h3 ` in the equations 3.2 and 3.3 is $t'(n) = [t'_1 , t'_2 ,t'_3 \dots t'_{2mf}]$. Amusing that t'_k is the odd values of t'_n and w_o is the angular frequency of the desired signal V_{sine} then the corresponding α values of the signal SBh are

$$\alpha(4n - 3) = t_k w_0 \text{ and } \alpha(4n) = t_{k+1} w_0 \quad (3.7)$$

where $n=1,2,3,4 \dots \frac{m_f}{2}$ and $k=1,3,5, \dots m_f - 1$

and

$$\alpha(4n - 2) = t_k w_0 \text{ and } \alpha(4n - 1) = t_{k+1} w_0 \quad (3.8)$$

where $n = \frac{mf}{2}, \frac{mf}{2} + 1, \frac{mf}{2} + 2, \dots, mf$ and $k = mf + 1, mf + 3, mf + 5, \dots, 2 * mf - 1$.

For example if $m_f = 8$, then $t'(n) = [t'_1, t'_2, t'_3, \dots, t'_{16}]$ and the corresponding $\alpha(n)$ values for SBh are $[\alpha_1, \alpha_4, \alpha_5, \alpha_8, \dots, \alpha_{19}, \alpha_{22}, \alpha_{23}, \alpha_{26}, \alpha_{27}, \alpha_{30}, \alpha_{31}]$

- Using the signals SAh and SBh instead of SA and SB (figure 2.29) respectively in order to generate V_{OPWM} as explained in clause 2.5.4, where V_{OPWM} in this case contains the intended harmonics amplitudes, thus it is renamed to V_{ohPWM} . The α values of the signal ($V_{ohPWM} = SAh - SBh$) are in agreement with equation 2.18, as the En-Unipolar-PWM is validated in clause 3.4.

3.2 En-Unipolar-PWM Modelling and simulation

The En-Unipolar-PWM algorithm is modelled by Matlab for the fundamental frequency, 3rd and 5th harmonic. The model (MEn-Unipolar-PWM V 1.0) allows fast calculation for the intersection points as well as the corresponding duty cycles and α values. This Matlab model is used to find-out the duty cycles table which will be used in the implementation process instead of a sine samples table as presented in clause 3.3. This model as well helps to find the optimal system parameters especially m_f and to analyse the system in frequency domain.

The inputs for the Matlab model are the signal's parameters of figure 3.2 ($V_{tri}, V_{sineh1}, V_{sineh1}', V_{sineh3}, V_{sineh3}'$) and in addition to the 5th harmonic parameter. The system signals equations are:

- $$V_{tri}(t) = \frac{2 * V_{p_{tri}}}{\pi} \arcsin \left[\sin \left(w_{tri} t - \frac{\pi}{2} \right) \right] \quad (3.9)$$

where, w_{tri} is the angular frequency ($2\pi f_{tri}$) of the carrier triangle signal and $V_{p_{tri}}$ is the peak amplitude (in Volt) of the triangle signal.

- $$V_{sineh1}(t) = V_{p_{sineh1}} \sin w_0 t \quad (3.10)$$

where, w_0 is the angular frequency ($2\pi f_{sineh1}$) of the desired output voltage.

- $$V_{sineh1}'(t) = -V_{p_{sineh1}} \sin w_0 t \quad (3.11)$$

- $$V_{sineh3}(t) = V_{p_{sineh3}} \sin(3w_0 t + \phi_{h3}) \quad (3.12)$$

where ϕ_{h3} is the phase shift between the fundamental frequency V_{sineh1} and the 3rd harmonic V_{sineh3}

- $$V_{sineh3}'(t) = -V_{p_{sineh3}} \sin(3w_0 t + \phi_{h3}) \quad (3.13)$$

•

$$V_{sineh5}(t) = Vp_{sineh5} \sin(5\omega_0 t + \phi h5) \tag{3.14}$$

where $\phi h5$ is the phase shift between the fundamental frequency V_{sineh1} and the 5th harmonic V_{sineh5}

•

$$V_{sineh5}(t) = -Vp_{sineh5} \sin(5\omega_0 t + \phi h5) \tag{3.15}$$

The block diagram in figure 3.3 presents the Matlab model.

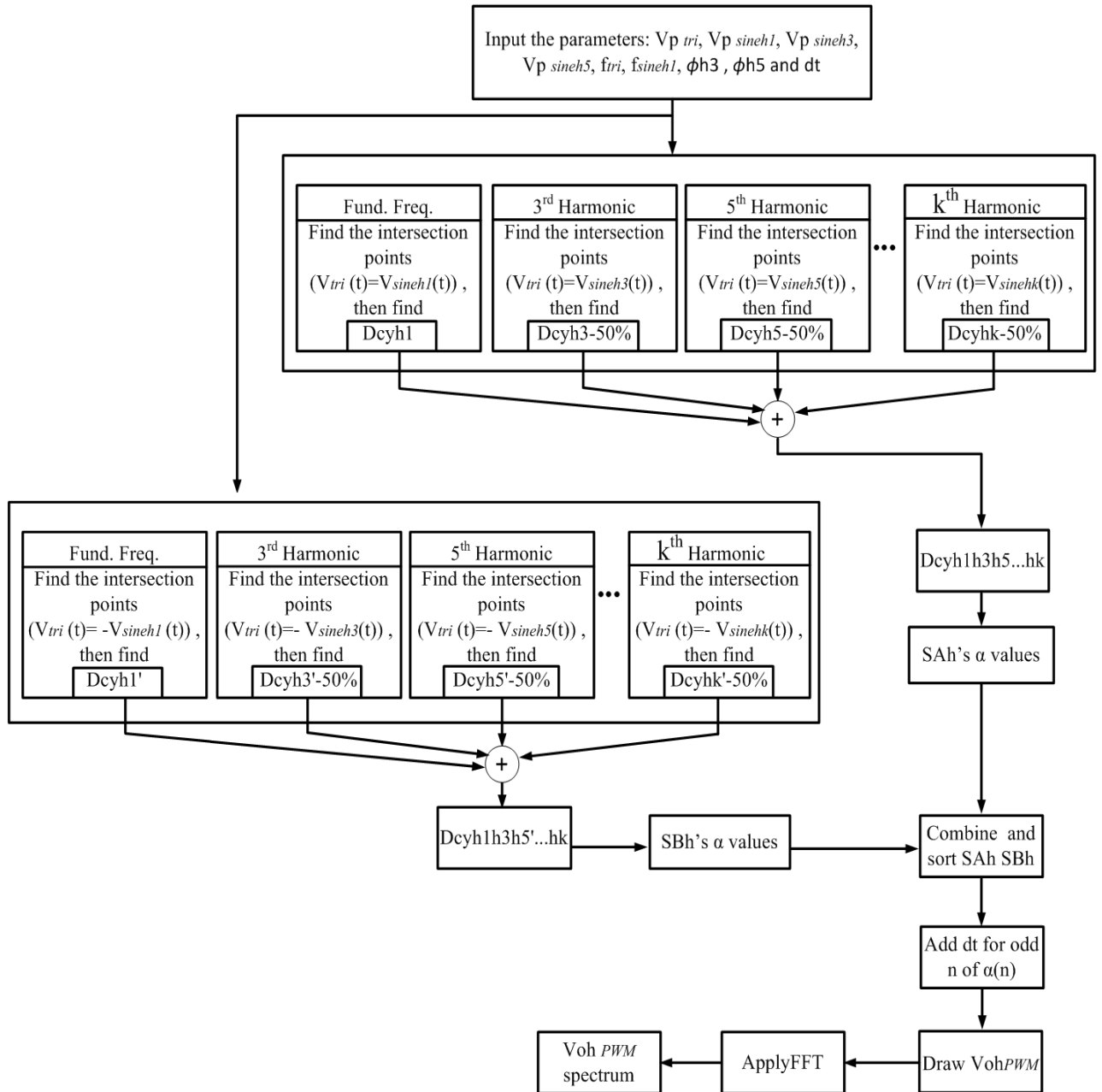


FIGURE 3.3: En-Unipolar-PWM Modelling

The model is based on programming the previous equations (3.9 to 3.15) in order to execute the steps explained in clause 3.1.2.

As seen in figure 3.3, the first step is to determine ($V_{p_{tri}}$ and $V_{p_{sineh1}}$) where these values are used to calculate m_a , and then the desired signal frequency (f_{sineh1}) and the carrier frequency (f_{tri}) where they used to calculate m_f . The intended harmonic amplitudes ($V_{p_{sineh3}}$ and $V_{p_{sineh5}}$) in addition to $V_{p_{sineh1}}$ must not exceed $V_{p_{tri}}$. Phase shift (ϕ_{h3} and ϕ_{h5}) can be added as well as the dead time dt which can be determined according to the switching element (IGBT) manufacturer datasheet.

The next step is to use the input parameters to find out the intersection points(see figures 3.2 and 3.3) and then duty cycle values: D_{cyh1} , $D_{cyh3-0.5}$, $D_{cyh5-0.5}$ and then add them together in order to calculate $D_{cyh1h3h5}$ which is used to find SAh α values. Applying the same concept to find out $D_{cyh1h3h5}$ and the corresponding SBh α values.

Instead of using the equations 3.5, 3.6, 3.7 and 3.8 to find out $V_{oh_{PWM}}$ α values one can simply combine and sort the two matrices α 's of SAh and α 's of SBh. The result up to this step is a matrix which contains the $V_{oh_{PWM}}$ α values.

Dead time as explained before is a waiting time during the switching on/off between each pair of the H-bridge IGBTs , for the Unipolar PWM strategy it is considered as a positive time shift for the odd α values of $V_{oh_{PWM}}$. In this model dt is denote to the dead time.

If a substitution of the α values in a set of equations as explained in the equation 2.18 is performed, that will give an information up to the harmonic $h\nu_{2m_f-1}$, which is not enough for the low pass filter investigations(PD measurements up to 500 kHz), thus FFT method is used for $V_{oh_{PWM}}$ spectrum calculation, keeping in mind that FFT is an effective method in case of synchronized triangle carrier frequency with the desired sinusoidal signal and with even m_f values(clause 2.5.2.2).

Performing a loop to draw the signal $V_{oh_{PWM}}$ as a function of time depending on the found α values and the desired DC voltage system, the result is a time domain signal similar in shape to the presented one in figure 2.29(3). Applying FFT for the function ($V_{oh_{PWM}}(t)$) will calculate the signal spectrum. In clause 3.4 the system validation is presented as well as the results.

3.3 Implementation of En-Unipolar-PWM

This PWM switching scheme was developed to allow the use of PWM for PD measurement and dielectric tests, it can be implemented in any 16-bit DSP which includes PWM modules.

The new switching scheme En-Unipolar-PWM is capable to generate a controllable low order harmonics, in this work 3rd and 5th harmonics can be generated and a user can online control the voltage amplitude as well as the harmonic phase shift with reference to the fundamental selected frequency. The generated harmonic voltage amplitude in addition to the fundamental amplitude must not exceed V_{tri} signal

amplitude, otherwise the switching scheme is programmed to be interrupted in such case.

The block diagram in figure 3.4 summarises the algorithm's implementation. After determining a suitable m_f , the Matlab model (clause 3.2) will be used to generate a table of duty cycles as result of solving the two functions ($V_{tri}(t)$ and $V_{sineh1}(t)$) for the intersection points at $ma=0.99$. Processing the duty cycle values from left to the right (forward) is used to generate SAh and from the right to the left (backward) to generate SBh. Three synchronised timers Interrupt Service Routines (ISR) are utilized to generate the fundamental frequency in addition to the 3rd and 5th harmonics.

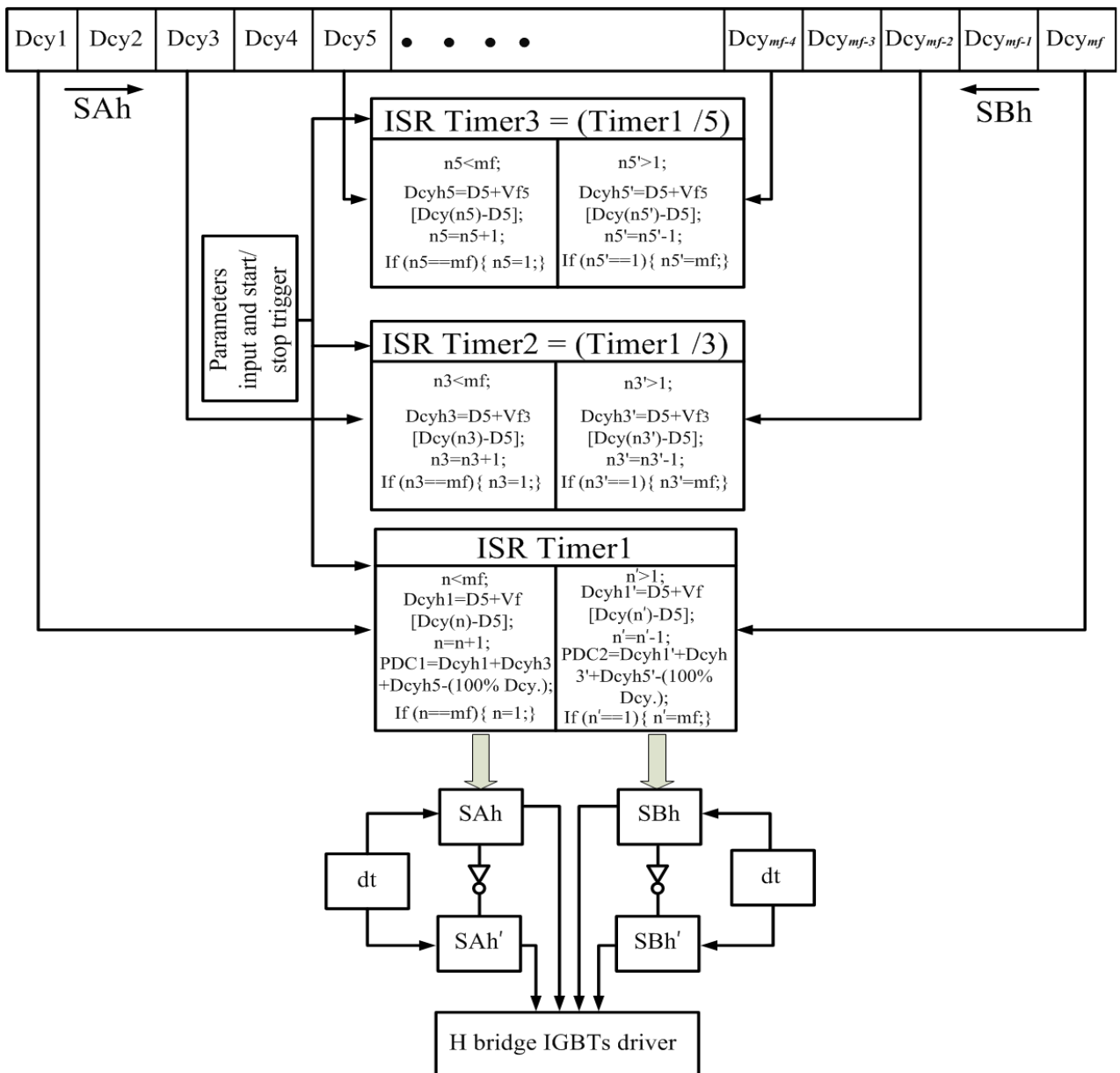


FIGURE 3.4: Implementation of En-Unipolar-PWM

The time of timer1 will determine the fundamental signal frequency where $\text{timer1} * m_f$ is the time of a complete desired sine cycle. Timer2 is 3 times faster than timer1, therefore it is able to process 3 complete sine cycles compared with timer1 to generate the 3rd harmonic. Timer3 is 5 times faster than timer1 where it is able to process 5 complete sine cycles compared with timer1, thus it generates the 5th harmonic.

Two counters are programmed inside each ISR, one to count forward for the generation of SAh and the another in backward for the generation of SBh. Multiplying the Duty cycle value by a factor from 0.1 to 0.99 will determine the amplitude where selecting the starting point (n, n3 ,n5 and n` , n3` , n5`) in each counter will determine the phase shift. As an example if $m_f=250$ and 90° phase shift between the desired sine and the 3rd harmonic is required, then the algorithm has to wait until zero crossing (normally at one complete cycle of the fundamental desired frequency) and then to update the values of n3 and n3` according to the following :

- $\frac{360^\circ}{250} = 1.44^\circ$ which the resolution of phase shift.
- $\frac{90^\circ}{1.44} = 62.5$ will be rounded to 63 , so $n3=63$ and $n3` = 250-63 = 187$

The voltage amplitude factor (Vf in Timer1) can have a value from 0.0001 to 0.9999 which will determine the modulation index m_a , as well as Vf3 and Vf5 in Timer2 and Timer3 respectively can have a value from 0.001 to 0.999 will determine the amplitude of the 3rd and 5th using the shown equations in each timer where D5 denote to 50% duty cycle.

While Timer1 just pass its $\frac{4}{5}$ period, the duty cycle registers PDC1 and PDC2 of the DSP PWM module will update their values according to shown equations in Timer1 (figure 3.4), where more details regarding a programming options in the DSP PWM module are taken in account in order to avoid any timing errors, so each time PDC1 and PDC2 were updated their values at the exact required values of Dcyh5, Dcyh5` as well as Dcyh3 and Dcyh3`.

Practically SAh and SBh` are generated automatically by inverting the value of SAh and SBh respectively. The dead time (dt) is added (according to the used DSP) at the rising pulse edge, this type of dead time is called a positive dead time, then the four signals (SAh, SAh` , SBh and SBh`) are fed to the IGBTs driver to produce the desired sine signal frequency with the intended 3rd and 5th harmonics amplitudes.

3.4 System Validation

3.4.1 The validation tests: overview and requirements

The previous explained Matlab model (MEn-Unipolar-PWM V 1.0) and the real system Pec-HV have to be validated to prove that the results are precise. The validation test performed first on the Matlab model in case of zero dead time and zero amplitudes of the intended harmonics and then the results are compared with the theoretical calculated data of table 2.1 (clause 2.5.2.1). Secondly to prove that the Matlab model MEn-Unipolar-PWM is valid in all possible cases, such as intended harmonic generation with/without dead time by comparing the simulated results with real measured data from the device (Pec-HV). The spectrum of the experimental measured data is calculated by applying the Matlab function FFT which is carefully processed to fulfil the requirements of measuring the Electromagnetic Interference in Time Domain (details are in the next paragraph). Further more a test is performed to measure the THD with/without intended harmonics using a measurements devices with respect to the standard IEC61000-4-7, and then to compare the measured data with a simulated one for the three fundamental frequencies (16.7 Hz , 50 Hz and 60 Hz).

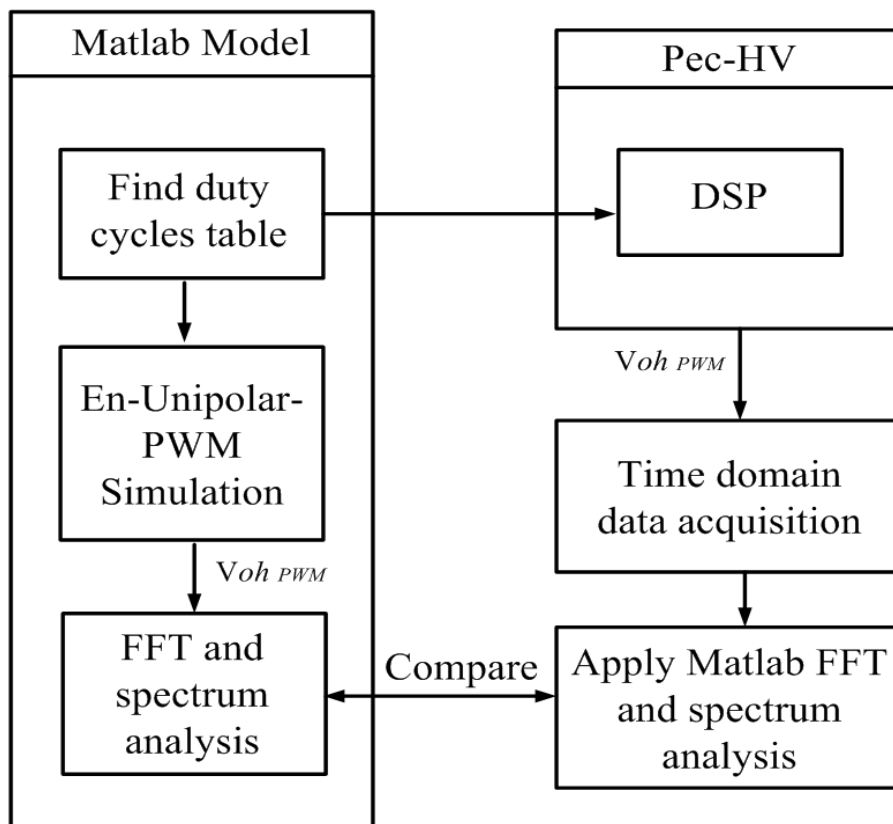


FIGURE 3.5: System Validation Test

As seen in figure 3.5, the duty cycles table stored in the DSP which controls the switching process of the En-Unipolar-PWM. Since the main target of En-Unipolar-PWM is to allow the usage of PD measurements as well as HV-DI tests with a specific amplitudes of intended harmonics, the analysis of the output signal $V_{oh_{PWM}}$ in frequency domain (up to 500 kHz) is required for the validation test and for the low pass filter investigation (clause 3.5).

Time domain EMI measurements are alternatives for the methods working in frequency domain which can be performed with a measurement receiver. The usually possible bandwidth with a measurement receiver is the $B=200$ Hz, in order to have a frequency resolution other than the 200 Hz (e.g. 34 to 120 Hz), the time domain EMI measurements method is applied in this research work.

Time domain EMI measurements must be performed in a certain conditions in order to have a proper measurements results [62,63,64,65,66]. Especially the dynamic range and sampling rate. In reference [63] Kurg from the University of Munich says that the sampling rate has to be 5 times of the interest highest frequency. The Signal to noise ration SNR (dynamic range in dB) of a stationary single has to be between 60dB and 70 dB[66]. A comparison study between time domain EMI measurements and frequency domain measurements in reference [65], where the final calculation states that with 60 dB (dynamic range) the time domain EMI peak measurements shows excellent results compared with frequency domain method.

An equation to calculate the SNR is presented in [71] as the following:

$$SNR_{dB} = 6.02N + 1.763 \quad (3.16)$$

where: N is the resolution in bits of the used Analogue to Digital Converter (ADC), and according to [71] this equation is valid over the DC to f_s as bandwidth, where f_s is the sampling frequency.

In order to meet the previous conditions, an oscilloscope with 12 bit ADC and high memory capacity is used as acquisition unit for the test, the chosen sampling frequency is 10 MHz, thus according to equation 3.16 the dynamic range is 74 dB which is fulfilled the previous explained conditions. The measured data is analysed then using Matlab FFT function.

3.4.2 The Validation Test

The system parameters (clause 3.2) has to be determined before performing the test, the most crucial parameter is m_f or in other word the switching frequency SWF. According to the explained information in clause 2.5.2 the SWF has to be high enough to simplify the design and to reduce the cost of the low pass filter as well as to keep a good power efficiency for the system. The chosen m_f value is experimentally adjusted to be 250, thus the SWF will be as the following :

- 12.47 kHz ($1/f_{tri} = 80.1875$ us) for the fundamental of about 50 Hz.

- 15 kHz ($1/f_{tri} = 66.659 \mu s$) for about 60 Hz.
- 12.47 kHz for the 16.7 Hz , that can be achieved by repeating each duty cycle value for 3 times . i.e the duty cycle value will be updated once each 3 triangle cycles ($3 * 80.1875 \mu s$) .

The dead time is according to the IGBTs data sheet is chosen to be $1.57 \mu s$, but due to a deference propagation delay time between the raising edges and falling edges of the used optocouplers in the IGBTs drivers (according to data sheet information)in addition to another issues, the real effective dead time is reduced to much lower values (explained in the discussion at the end of this clause).

A- Matlab Model validation test at zero dead time and zero amplitudes of intended harmonics

The following parameters values were determined to perform the test:

- $m_a = 0.8$, $m_f = 250$, $dt = 0$, $V_{p_{sineh3}} = V_{p_{sineh5}} = 0$ and $VDC = 1 V$.
- $1/f_{tri} = 80.1875 \mu s$ so the fundamental freq. is 49.882 Hz (these numbers are chosen in order to have integer values in the DSP duty cycle registers).
- The signal $V_{oh_{PWM}}$ has a steps time resolution of 100 ns and was simulated for one complete cycle of the fundamental frequency (20.047 ms).

Figure 3.6 shows the spectrum of simulated $V_{oh_{PWM}}$. It is obvious that the results are in agreement with the explained Naturally Sampled(NS) PWM especially the baseband harmonics are not present, further more the carrier sidebanded frequency has a similar peak amplitude compared with the presented data in table 2.1 as well as reference [11](see table 3.1), since the baseband area is harmonics free , it is obviously clear that the calculated α values by the EN-Unipolar PWM are in agreements with previous explained α approach, in other words if a set of equations are founded according to equation 2.18 and α values of this simulated exempld are substituted , the result which is the amplitudes of h_{v_k} will equal approximately zeros for the ks from $k=3$ until $k=499$.

According to the theoretical information which explained in clause 2.5, in NS-PWM only harmonics around even multipliers of m_f ($2m_f, 4m_f, 6m_f \dots$) appears in the spectrum , but in the EN-Unipolar-PWM (as seen in figure 3.6) the odd multipliers of m_f ($m_f, 3m_f, 5m_f \dots$) also appears in very small amplitudes which is fixed to roughly 0.0038 in case of $VDC=1$. That is due the 1 us deviation (100 ns time resolution) between the signals V_{sineh1} and V_{sineh1} , this can be ignored because it has no effect on the quality of the produced signals neither THD or the background noise in case of PD measurements.

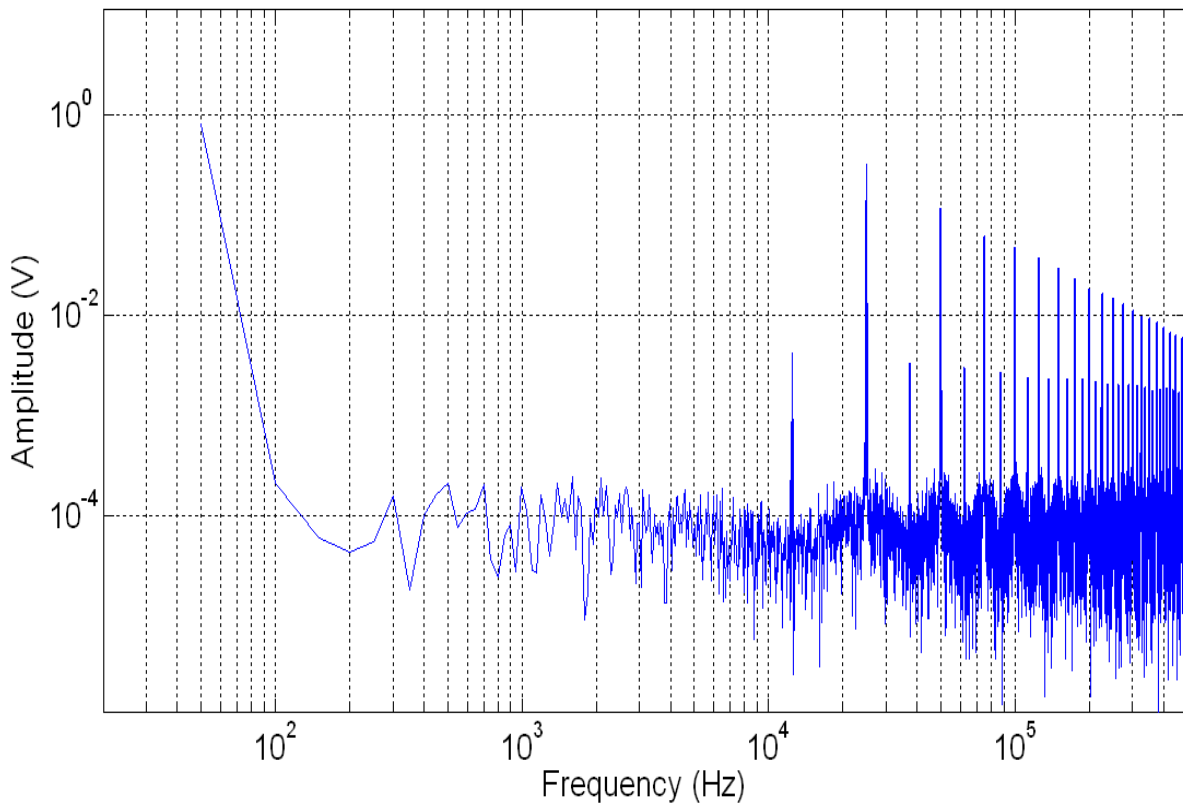


FIGURE 3.6: Spectrum of En-Unipolar-PWM for zero d_t and without intended harmonics

Table 3.1 shows the compared sidebanded harmonics peak values of the simulated En-Unipolar PWM with the previously mentioned parameters with the calculated values from reference [11]. The first column is the harmonic order which is always a multiple of m_f (equation 2.15) and by multiplying its values by the fundamental frequency (49.88 Hz) will give the exact frequency of the harmonic order (the second column). The numbers in the 3rd and 4th column are almost the same, the small differences is due to calculation round off error. That is clearly proofs that En-Unipolar-PWM algorithm passes the first validation test.

Harmonic Order	At the frequency ± 1 Hz in kHz	NS-PWM amplitudes @ VDC=1 in V	Matlab Model @ VDC=1 in V
$2m_f-7$	24.592		0.00053
$2m_f-5$	24.692	0.013	0.01255
$2m_f-3$	24.791	0.139	0.13860
$2m_f-1$	24.891	0.314	0.31490
$2m_f+1$	24.991	0.314	0.31380
$2m_f+3$	25.091	0.139	0.14020
$2m_f+5$	25.190	0.013	0.01288
$2m_f+7$	25.290		0.00040
$4m_f-7$	49.533	0.017	0.01729
$4m_f-5$	49.633	0.084	0.08361
$4m_f-3$	49.733	0.115	0.11520
$4m_f-1$	49.832	0.105	0.10560
$4m_f+1$	49.933	0.105	0.10480
$4m_f+3$	50.032	0.115	0.11410
$4m_f+5$	50.132	0.084	0.08469
$4m_f+7$	50.232	0.017	0.01769

TABLE 3.1: Comparison between the simulated results and the theoretical calculated from[11]

B- En-Unipolar PWM complete spectrum validation test, with dead time and in addition to generated intended harmonics

This test was performed with the following parameters:

- $m_a = 0.8$, $m_f=250$, $dt= 1.57 \mu s$ for the measured data and $d_t=0.3$ us for the simulated data , $V_{psineh3}=V_{psineh5} = 12.5\%$ of $V_{psineh1}$ which is 0.1 V at VDC=1V (for the simulation) and 10 V for the measurements of $V_{oh_{PWM}}$ which is produced by the device Pec-HV, so the expected harmonics amplitudes are 1 V in this case for the 3rd and 5th.
- $1/f_{tri} = 80.1875us$ so the fundamental freq. is 49.882 Hz.
- The simulated signal $V_{oh_{PWM}}$ has a steps time resolution of 100 ns and it's spectrum was calculated for one time domain cycle of the fundamental frequency.
- The measured signal $V_{oh_{PWM}}$ has a sampling time of 100 ns and recorded for two complete cycles of the fundamental frequency.

The model MEn-Unipolar-PWM is used to simulate this test results for the following two cases; (1) with zero dead time. and (2) with 0.3 us dead time. The

spectrum of the simulated signal for both cases are compared to the measured $V_{oh_{PWM}}$ (3rd case) from the device Pec-HV. The measurements are performed more than once to assure that the signal is stationary.

Figures 3.7, 3.8 and 3.9 are present the results of this test for the three taken cases, where table 3.2 presents a selected harmonics peaks values in volt of the 3 cases up to roughly 500 kHz.

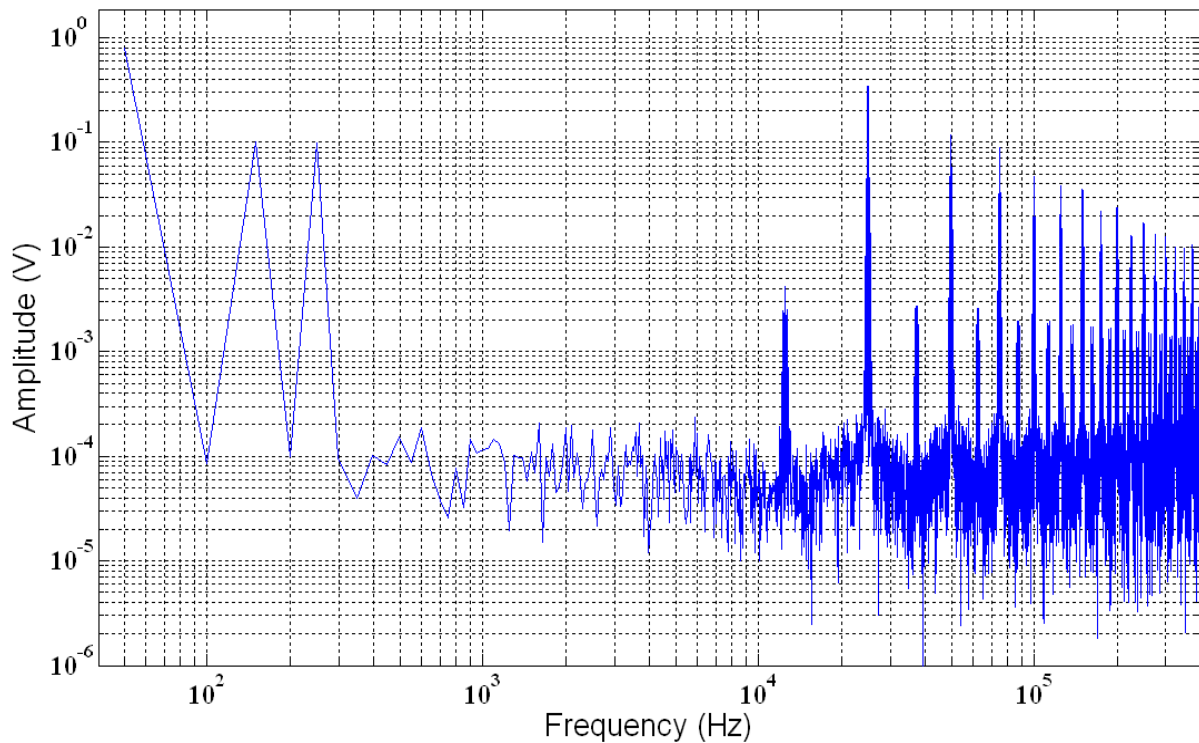


FIGURE 3.7: 1st case, Simulated spectrum of $V_{oh_{PWM}}$ at $dt=0$ with generated 3rd and 5th harmonics at 50 Hz

As seen in the figure 3.7, the 1st case results shows that the spectrum contains the expected 3rd and 5th harmonics with the amplitudes of 0.0999 V and 0.0998 V respectively, that is so closed from the desired amplitude (0.1 V), it is also clear that the baseband area is free from any other harmonics rather than the intended ones.

In the second case (figure 3.8) where the dead time is taken into account, the baseband area contains some undesired harmonics, that is due to the dead time effect. This result is matched with the briefly explained in [11,12] about the dead time effects.

In the 3rd case(figure 3.9), which is the experimentally measured, the signal $V_{oh_{PWM}}$ spectrum shows a very good desired results, the shape is close to the desired one. The amplitudes of the intended harmonics almost match the expected (0.9116 and 0.9234 V) of the 3rd and 5th harmonics respectively, as well as the amplitude of the fundamental frequency(7.349 V) which is not far from the desired one(8 V). Further more the baseband area is free from undesired harmonics(one of the targets). In spite of this satisfying results, a clear interpretation is needed to explain the differences between the selected dead time values(1.57 us in 3rd case and 0.3 us in the second case). Before answering this question a clear reading of the three cases is presented as numerical values in table 3.2 .

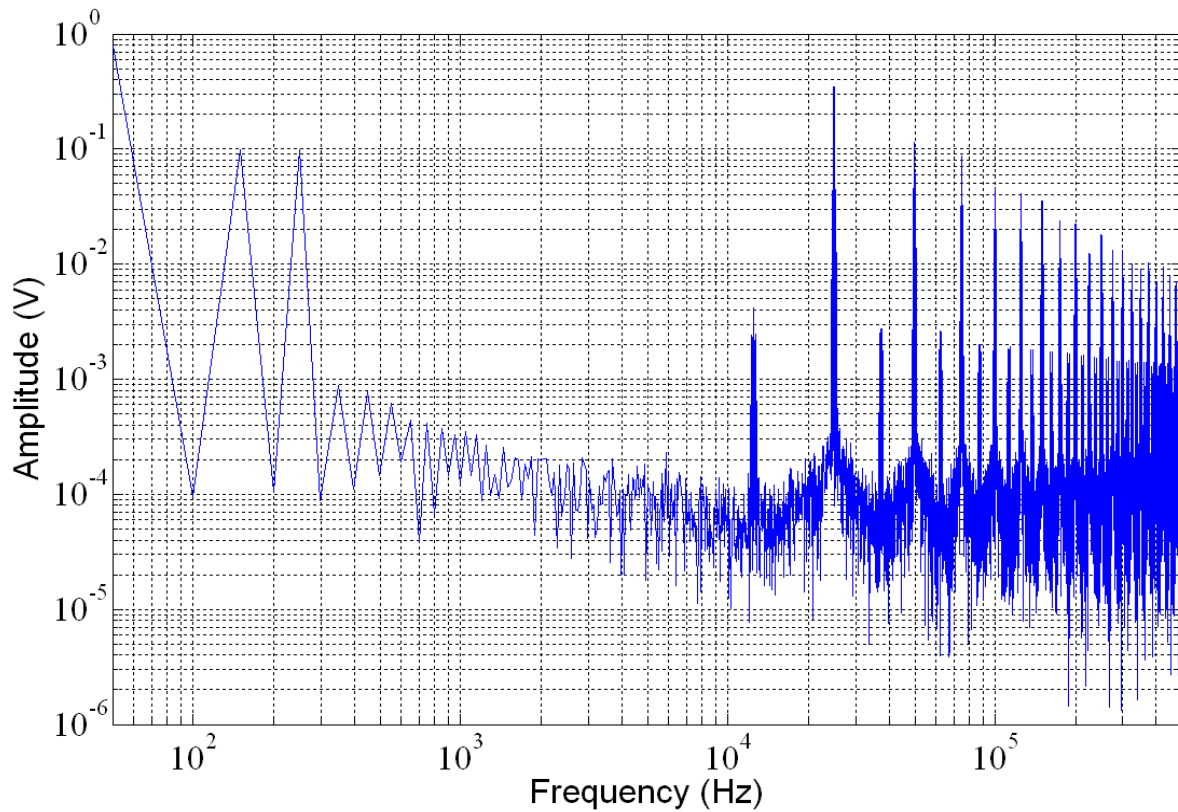


FIGURE 3.8: 2nd case, Simulated spectrum of V_{oh_PWM} at $dt=0.3$ μ s with generated 3rd and 5th harmonics at 50 Hz

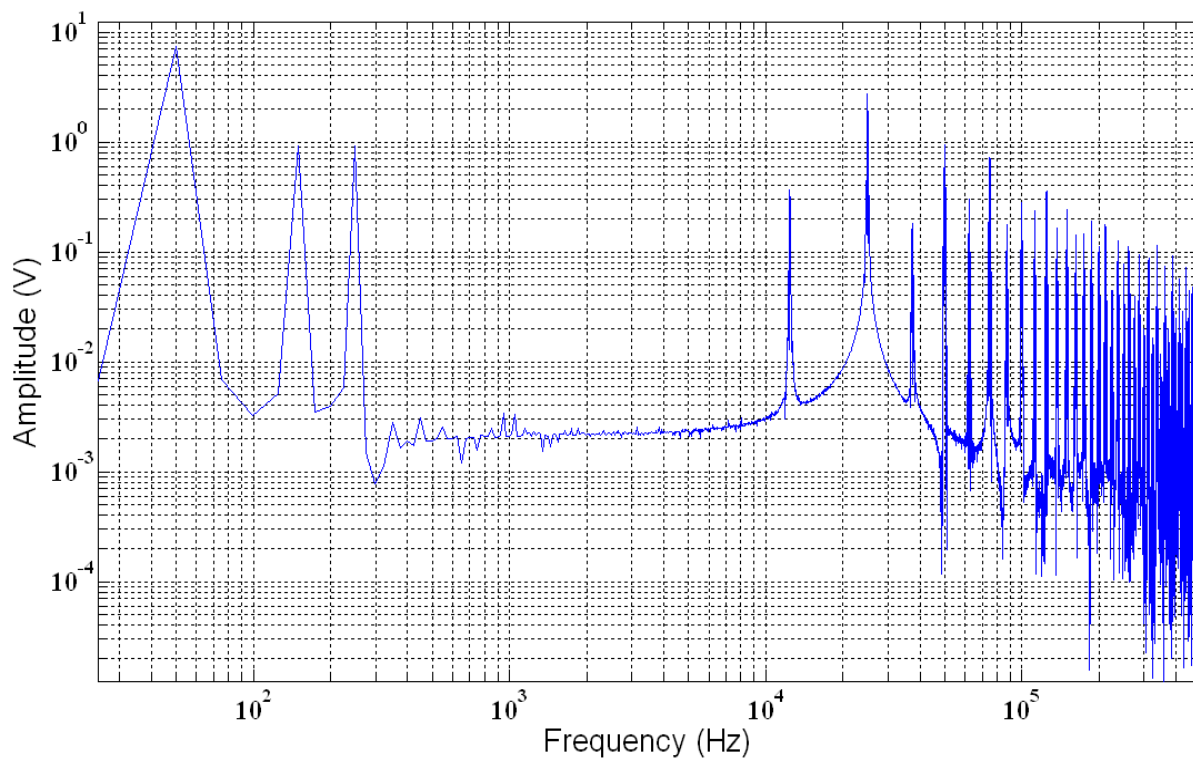


FIGURE 3.9: 3rd case, Measured spectrum of V_{oh_PWM} at $dt=1.57$ μ s with generated 3rd and 5th harmonics at 50 Hz

Harmonic Order	At the frequency ± 1 Hz in kHz	(1) Matlab Model dt=0, 12.5 % 3rd and 5th @ VDC=1 in V	(2) Matlab Model dt=0.3 us, 12.5% 3rd and 5th @ VDC=1 in V	(3) Measured dt=1.57 us, 12.5% 3rd and 5th @VDC=10 in V
1	0.04988	0.7999	0.793	7.349
3	0.14965	0.0999	0.098	0.9116
5	0.24941	0.0998	0.099	0.9234
7	0.34918	0.00004	0.0008	0.0028
9	0.44895	0.00008	0.0007	0.0031
$2m_f-7$	24.592	0.0447	0.04	0.3715
$2m_f-5$	24.692	0.0396	0.039	0.4483
$2m_f-3$	24.791	0.1594	0.157	1.280
$2m_f-1$	24.891	0.3469	0.349	2.290
$2m_f+1$	24.991	0.3462	0.348	2.732
$2m_f+3$	25.091	0.1598	0.158	0.8987
$2m_f+5$	25.190	0.0379	0.0347	0.3417
$2m_f+7$	25.290	0.0459	0.0446	0.3222
$4m_f-7$	49.533	0.0466	0.0468	0.3948
$4m_f-5$	49.633	0.0338	0.0329	0.2582
$4m_f-3$	49.733	0.0589	0.0622	0.5766
$4m_f-1$	49.832	0.1177	0.114	0.9463
$4m_f+1$	49.933	0.1178	0.1145	0.8792
$4m_f+3$	50.032	0.0575	0.061	0.5110
$4m_f+5$	50.132	0.0352	0.034	0.2772
$4m_f+7$	50.232	0.0457	0.0459	0.3851
$6m_f+1$	74.874	0.0197	0.023	0.2805
$6m_f+3$	74.973	0.0879	0.087	0.7016
$6m_f+5$	75.073	0.0367	0.0386	0.3594
$6m_f+7$	75.173	0.0065	0.0071	0.0563
$8m_f \pm 5$	100 ± 0.25	0.0474	0.0382	0.2458
$10m_f \pm 5$	124.8 ± 0.25	0.0373	0.0416	0.3529
$12m_f \pm 5$	149.8 ± 0.25	0.0341	0.0321	0.245
$14m_f \pm 5$	174.2 ± 0.25	0.0221	0.03	0.1473
$16m_f \pm 5$	199.8 ± 0.25	0.0240	0.0191	0.1121
$40m_f \pm 5$	498.8 ± 0.25	0.0060	0.0054	0.0351

TABLE 3.2: Compare the harmonics of $V_{oh_{PWM}}$ spectrum in three cases: (1) simulation with dt=0.(2)simulation with dt=0.3 us (3) measured data from Pec-HV

Before starting the expatiations of table 3.2 one has to take in account that: in order to compare the simulation results of (case 1 and 2) of the harmonics amplitudes with the measured one, the simulated values have to be multiplied by 10, since the relation between VDC and the amplitudes of the harmonics is linear (clause 2.5.21).

The table (3.2) is divided vertically to five parts according to the frequency range, the following is briefly reading and analysis of the table's data:

1. Baseband area : the harmonics order from the first (fundamental) to the ninth are selected because they have the highest amplitudes among the baseband harmonics. The third part of the system validation test(clause 3.4.2-C) is focused only on this range of frequency for the three fundamentals (16.7 Hz 50 Hz and 60 Hz)
2. Carrier sideband frequencies around $2*m_f$: here all the harmonics peaks are considered, the number of peaks and their shapes are almost identical in the three cases, the differences are in the amplitudes. The measured harmonics amplitudes mostly are less than the simulated, that is due to the difference of dv/dt of the signal Voh_{PWM} in time domain, where the measured pulse (will be explained later) shows larger dv/dt and thus less harmonics amplitudes in frequency domain.
3. Carrier sideband frequencies around $4*m_f$: here also all the peaks are considered, the same as the previous point the signal shape in the three cases are almost identical but with roughly +20 Hz shifted(case 3 shifted from case 1 and 2) , the measured harmonics amplitudes are slightly less than the both simulated case except for the harmonics $4*m_f \pm 1$ for is between the fist case and the second.
4. Carrier sideband frequencies around $6*m_f$: here just some of the sideband frequencies are considered, the measured harmonics amplitudes(case 3) are more closed to the first case, the measured amplitudes are also shifted by roughly +26 Hz from the simulated harmonics. This shift is due to the slightly difference between the simulation SWF and the measured one.
5. 100 - 500 Khz: here only the highest peaks are selected,while this frequency range is important for the low pass filter investigations. Also the measured peaks shows less amplitudes than the case 1 and 2 .

Test's Data analysis

According to the shown results above, one can notes the following :

1. The dead time in case 2 is 0.3 us where it is 1.57 us in the 3rd case.
2. The baseband area of the measured data are more closed to case 1 , where no dead time is considered in the simulation.

- Most of the measured carrier sideband harmonics amplitudes are slightly less than the simulated ones (when the simulated are multiplied by 10).

Regarding the first and second points:

In order to find out the reason behind that, the time domain signal of $V_{oh_{PWM}}$ is examined for case 1 and 3 of table 3.2. Figure 3.10 shows the 7th cycle (as an example) pulse for the 1st and 3rd cases. Actually most of the pulses are examined, as result it is found that the measured pulses are having a real dead time value ranges from 0.1 us to 0.87 us where most of them has a real dead time value of roughly 0.3 us (the selected for case 2), while the real programmed dead time value is 1.57 us. That can be understood by analysing the hardware prorogation delay behaviour, starting from the DSP PWM signal outputs pins, then going through the optocoupler of the IGBT's driver and ending by the IGBT switching on/off process. The used optocoupler (according to datasheet) has more propagation delay by roughly 600 ns for the falling edges of pulses than for the raising edge, where the programmed dead time is creating a delay for the raising edge, in other words it reduces the dead time effect by roughly 600 ns by means of delaying the falling edges.

Another cause which reduces the effect of dead time is the dv/dt of the IGBTs switching on/off characteristics, where larger raising/falling time reduced the pulse width (measured at 80% of the pulse amplitudes) since the switching on/off ranges from 0.3 to 1.8 us. With respect to the explained above, the dead time of 0.3 us is adopted in MEn-Unipolar-PWM for the simulations.

Regarding the third point:

Since the measured pulses of $V_{oh_{PWM}}$ has a larger dv/dt than the simulated ,thus it will have less harmonics amplitudes for the carrier sideband frequencies . On the other hand, the simulation has to be performed at high time resolution (100 ns) in order to keep the accuracy of switching at α values, as well as to use to same number of data points for the FFT function.

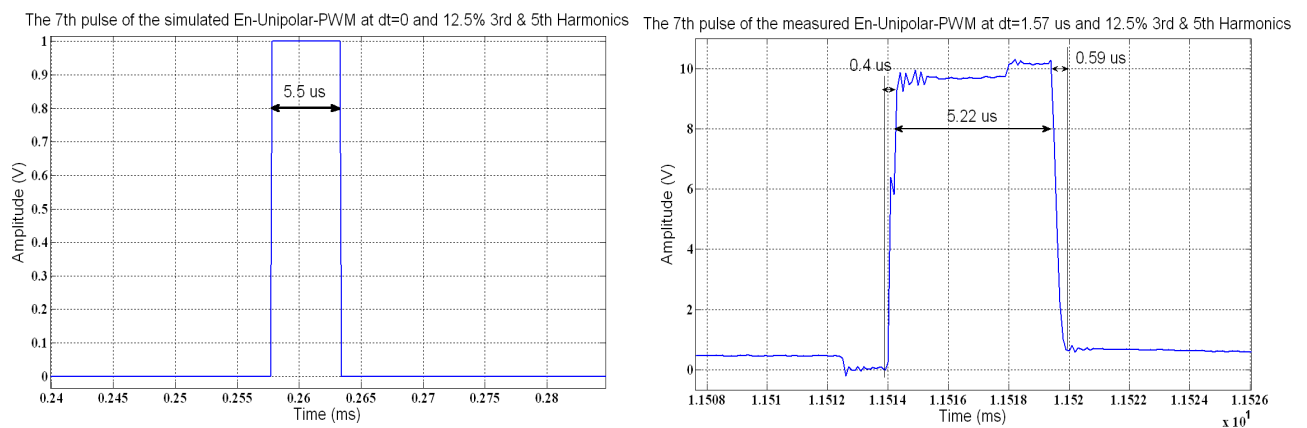


FIGURE 3.10: A comparison between simulated and measured Pulse

C- THD validation Test

One of the main goals of this thesis is to have a high quality output voltage signal from the Pec-HV. In this test the THD will be evaluated for the three fundamental frequencies (16.7 Hz, 50 Hz and 60 Hz) for both; the modelled system (MEn-Unipolar-PWM) and for the device Pec-HV. The measurements are performed according to the standard IEC61000-4-7 (Testing and measurement techniques General guide on harmonics and inter-harmonics measurements and instrumentation, for power supply systems and equipment connected thereto). The signal $V_{oh_{PWM}}$ from Pec-HV is filtered by a low pass filter, where the filter is needed here to keep the measurement device save from high frequency disturbances.

The following parameter where selected for the test :

- The VDC value is chosen to be 125 V for the simulation and 180 V for the experimental measurement of Pec-HV(the VDC values are selected to simplify result's reading).
- The modulation index $m_a=0.8$ for both. The dead time is modified to $0.3 \mu s$ for simulations.

This test is performed in two parts, the first with zero amplitudes of the intended harmonics and the second with 12.5 % of the 3rd and 5th harmonics. The ideal THD for the fist test part is 0% , where it 17.68% for the second test part.

First Part:

Table 3.3 shows the results of using the Matlab model MEn-Unipolar-PWM to find out the spectrum of $V_{oh_{PWM}}$ for each fundamental frequency(16.7 Hz 50 Hz and 60 Hz), and then to calculate the THD up to the harmonic order 63 using equation 2.1 . It is clear that all the results are so closed from the ideal case (THD= 0%) as well as the amplitudes of the fundamental frequencies (ideally $0.8*125= 100$ V). The three fundamental frequencies has slightly different from the ideal values (16.63 Hz 49.883 Hz and 60.01 Hz), because the model MEn-Unipolar-PWM is built in an accurate way to simulate the implemented En-Unipolar-PWM where an integer numbers has to be filled in registers to perform the required PWM switching process. Having zero dead time means zero THD up to harmonic order 63 as proofed in clause 3.4.21, according to various performed simulations, the THD amount depend on the dead time value (direct proportional), but the THD in case of fixed dead time is inversely proportion to the SWF (the carrier triangle period) , that is why the 16.63 Hz has the lowest THD where 60.01 has the highest one.

Harmonic Order	16.7 Hz(16.63) V _p	50 Hz (49.883) V _p	60 Hz (60.01) V _p
1	99.6	98.8	98.56
3	0.127	0.394	0.474
5	0.082	0.245	0.287
7	0.057	0.1709	0.205
9	0.045	0.143	0.162
Up to 63	THD 0.19%	THD 0.57%	THD 0.69%

TABLE 3.3: THD evaluation by system simulation at $dt=0.3\mu s$ and zero intended harmonics

Table 3.4 and the figures 3.11, 3.12, 3.13 shows the measured THD of the three fundamental frequencies. The harmonics are measured by the power quality analyser (janitza UMG511) which is directly connected at the output terminals of the device Pec-HV, where the measured signal here is V_o . The results are so closed from the simulated data in table 3.2, In other words the system Matlab model as well as the device Pec-HV are achieved what is required until this point(high quality output voltage signal).

Harmonic Order	16.7 Hz(16.63) V rms	50 Hz (49.9) V rms	60 Hz (60.1) V rms
1	99.945	101.67	102.895
3	0.122	0.513	1.097
5	0.080	0.0300	0.021
7	0.060	0.167	0.145
9	0.120	0.0900	0.090
Up to 63	THD 0.3%	THD 0.65%	THD 1.09%

TABLE 3.4: Measured THD for the three fundamental frequencies at zero intended harmonics

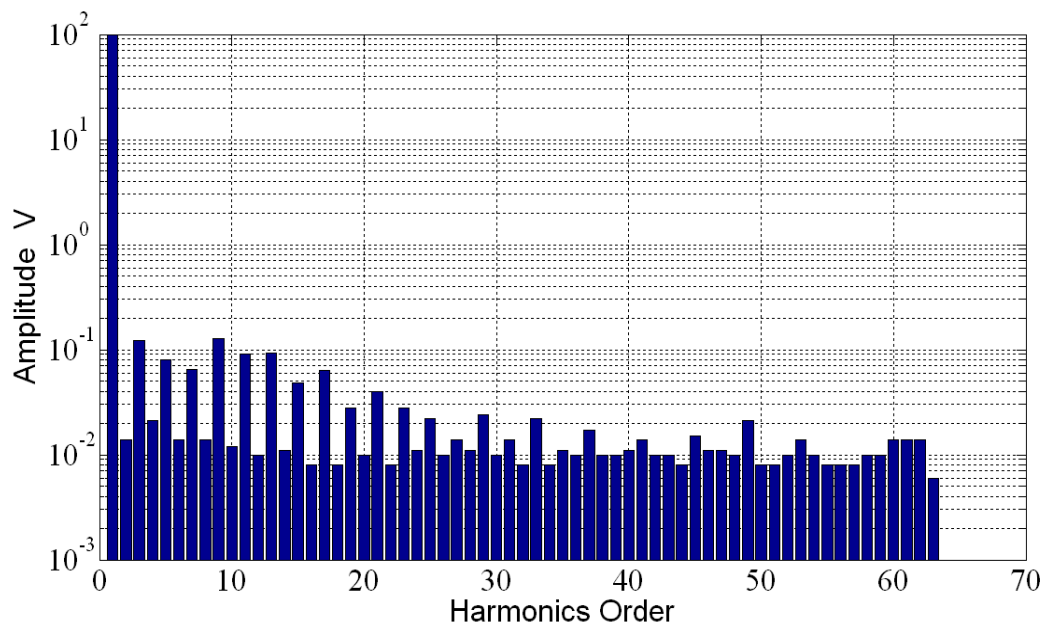


FIGURE 3.11: Measured THD for the 16.7 Hz at zero intended harmonics

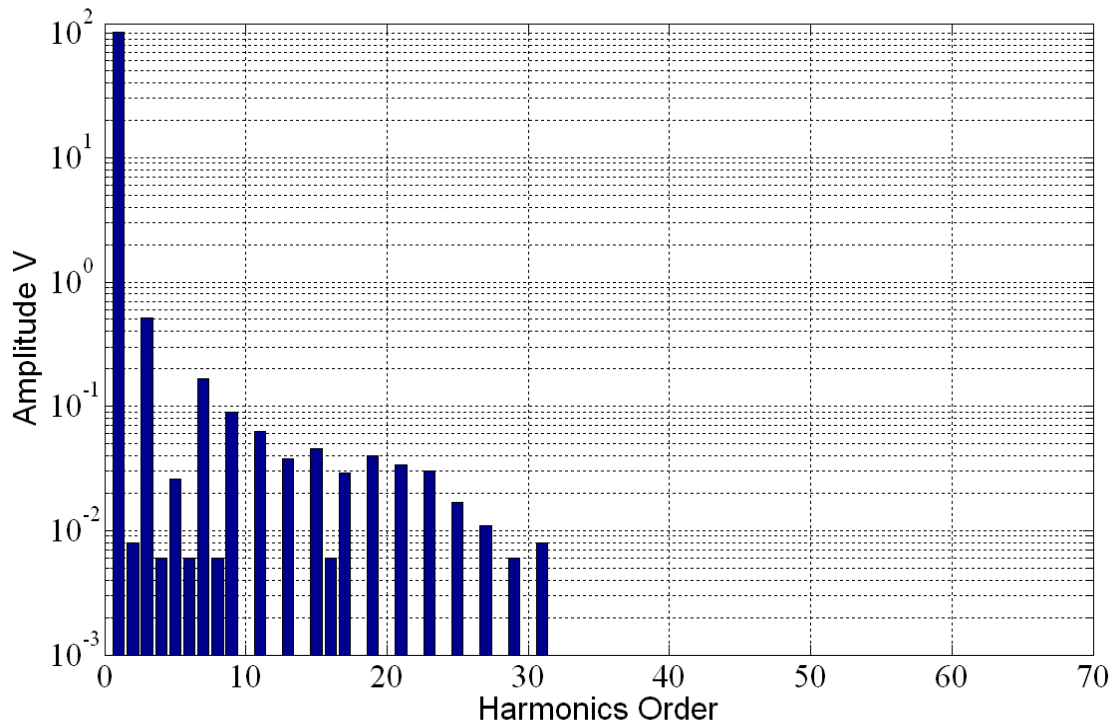


FIGURE 3.12: Measured THD for the 50 Hz at zero intended harmonics

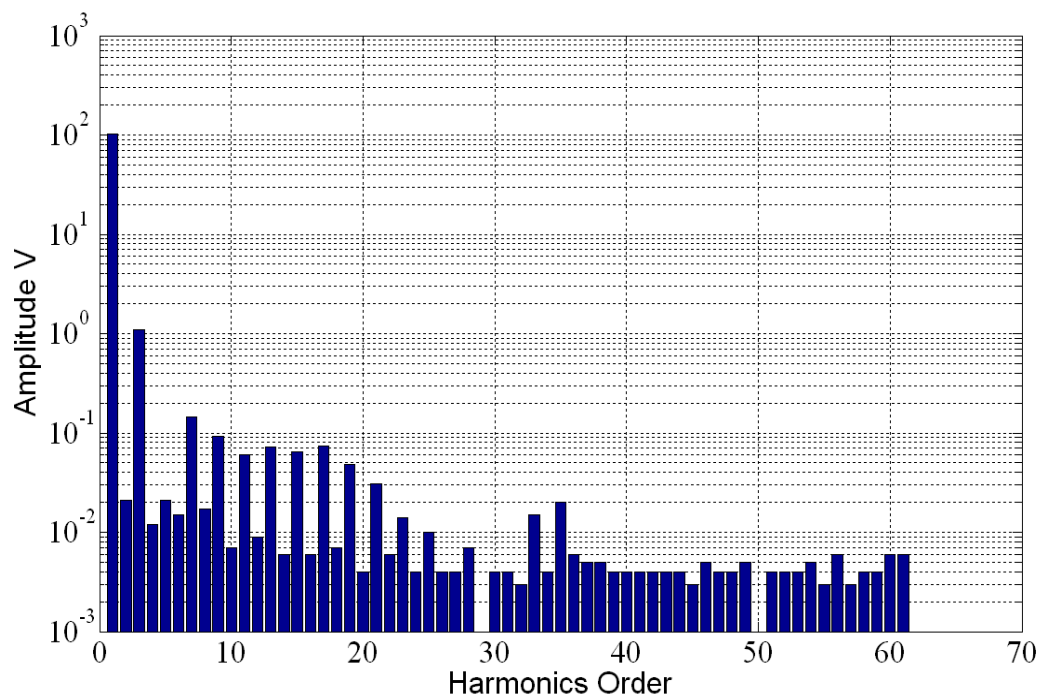


FIGURE 3.13: Measured THD for the 60 Hz at zero intended harmonics

Second Part :

This test is performed with the same parameters of the first part but a 12.5% of 3rd and 5th harmonics were added. High accuracy (theoretical THD must be so closed from measured/simulated) is required for generating an intended harmonic in order to achieve one of the main goals of this thesis.

Table 3.5 shows the simulated THD with the generation of 12.5% 3rd and 5th harmonics, the expected THD in this case is 17.68%. The simulated data for the three fundamental are so closed from the expected THD, the maximum difference is acceptable as well (0.3% at 60 Hz).

Harmonic Order	16.7 Hz(16.63) V _p	50 Hz (49.883) V _p	60 Hz (60.01) V _p
1	99.6	98.8	98.56
3	12.36	12.1	12.02
5	12.4	12.23	12.2
7	0.054	0.167	0.204
9	0.048	0.1422	0.157
Up to 63	THD 17.58%	THD 17.42%	THD 17.38%

TABLE 3.5: Simulated THD of the three fundamental frequencies with intended harmonics

The measured data which presented in the figures 3.14, 3.15, 3.16 and table 3.6 are in agreement with the simulated as well as the expected THD, also the maximum deviation between simulated and measured (0.79% at 60 Hz) is within an acceptable range.

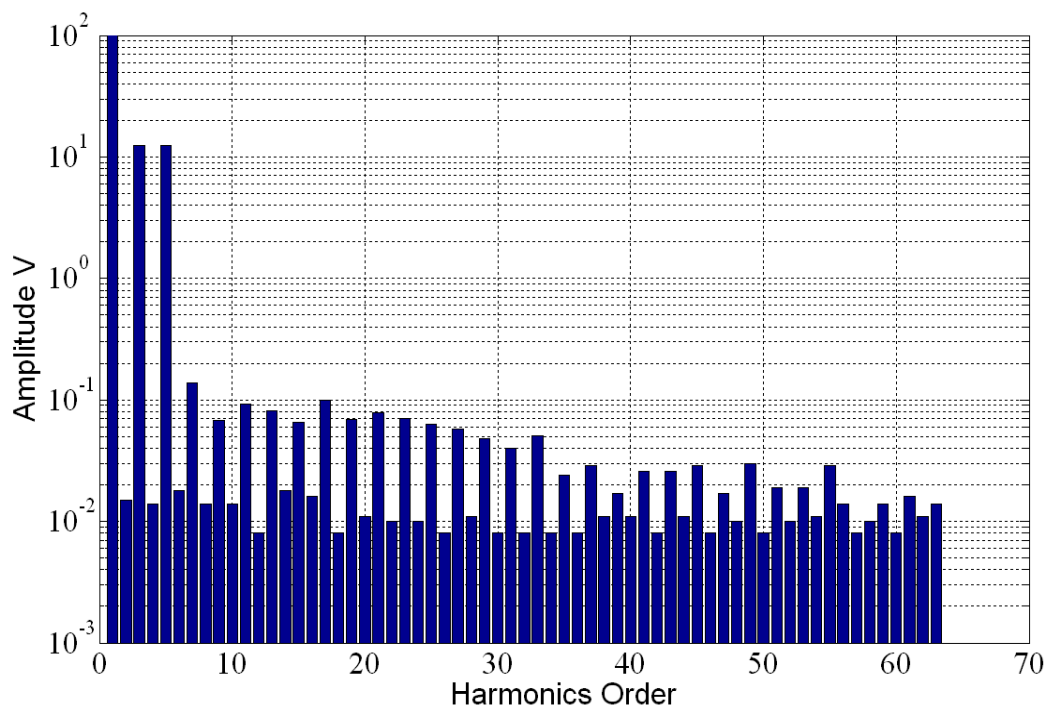


FIGURE 3.14: Measured THD for the 16.7 Hz with intended harmonics

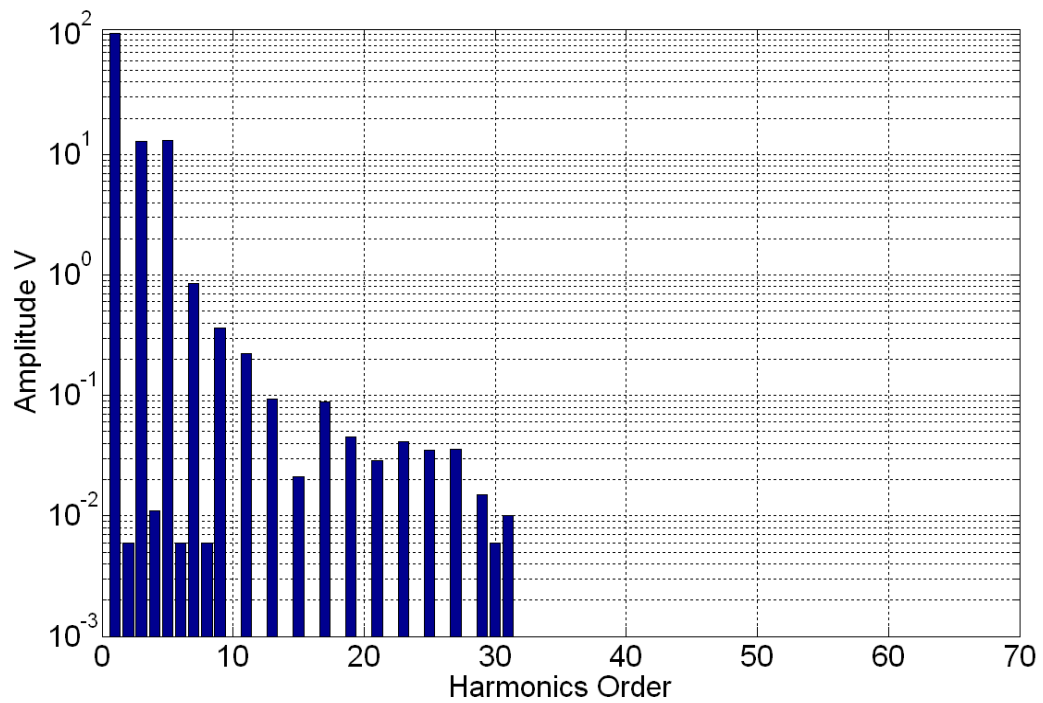


FIGURE 3.15: Measured THD for the 50 Hz with intended harmonics

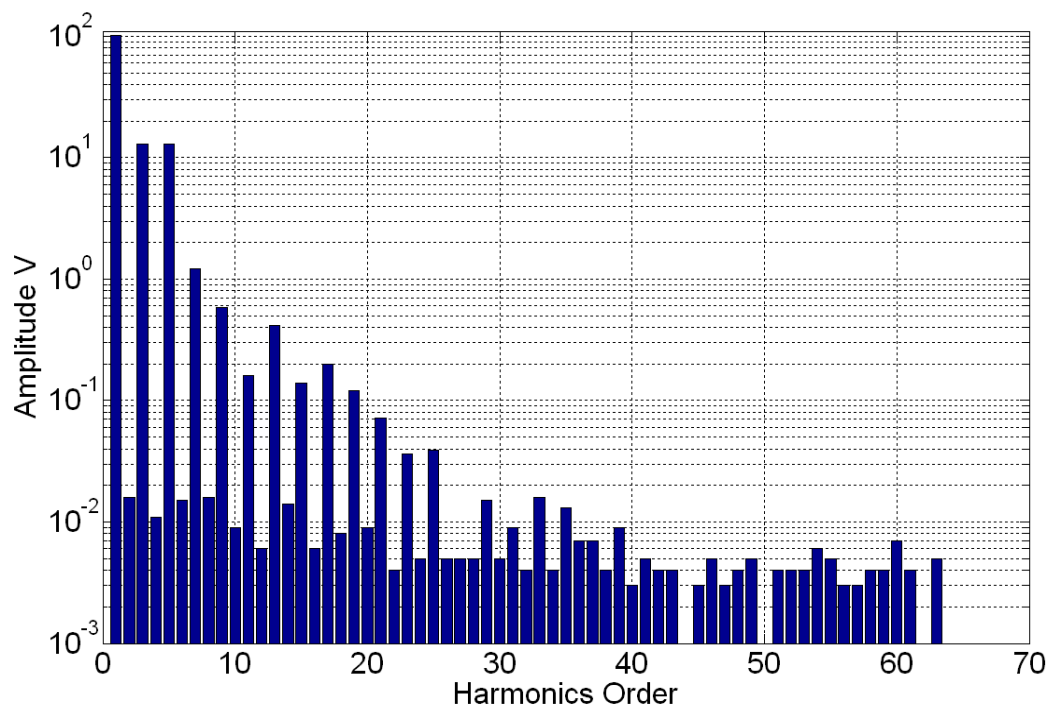


FIGURE 3.16: Measured THD for the 60 Hz with intended harmonics

Harmonic Order	16.7 Hz(16.63) V rms	50 Hz (49.9) V rms	60 Hz (60.1) V rms
1	100.11	101.62	101.22
3	12.47	12.886	12.957
5	12.498	13.025	12.971
7	0.139	0.8520	1.206
9	0.068	0.3660	0.583
Up to 63	THD 17.6%	THD 18.09%	THD 18.17%

TABLE 3.6: Measured THD for the three fundamental frequencies with intended harmonics

The results of the three validation tests (clause 3.4.2- A,B and C) are leads to the conclusion that the system Pec-HV and MEn-Unipolar-PWM are fulfils their requirements and both are valid.

3.5 Extrapolation phase

The device Pec-HV has a various dynamic output signal behaviour where the voltage amplitude, frequency and the amplitudes/phase-shift of the generated intended harmonics are controllable within a wide range of digitised steps. (for example ma of the fundamental 50 Hz can have a value from 0.0790 to 0.9999 within a step resolution of 0.0005).

Table 3.7 shows a simulated THD up to the harmonic order 63 at different modulation index (m_a) without a generation of intended harmonics. Through performing this simulation, it has been noticed that the amplitudes of the 3rd, 5th, 7th and 9th harmonics are roughly fixed around (0.4%, 0.3%, 0.2% and 0.1 %) respectively of the maximum fundamental frequency (at $m_a=1$, $m_f=250$ and $dt=0.3\mu s$) regardless of changing m_a value later, that means if m_a is decreased then the fundamental amplitude will decrease too, thus the THD will increase and vice versa. These undesired harmonics are produced due to the dead time effect and they are roughly fixed since the dead time has a fixed value. i.e if $ma=1$ at $VDC=1$ V then the amplitudes of the 3rd, 5th, 7th and 9th are 0.004 V, 0.003 V, 0.002 V and 0.001 V respectively, even if ma value is changed, these harmonics amplitudes remains almost the same.

m_a	THD[%]
0.2	2.2
0.3	1.51
0.4	1.41
0.5	0.91
0.6	0.77
0.7	0.66
0.8	0.57
0.9	0.51
0.99	0.47

TABLE 3.7: System dynamic behaviour at various m_a

Since the system is able to generate intended 3rd and 5th harmonics (various amplitudes and phase-shifts), therefore it is possible to compensate the undesired 3rd and 5th (generated due dead time) by generating intended ones with an adequate amplitude/phase-shift to reduce the THD, thus having a high quality output with an THD less than 0.4%. Figure 3.17 shows a measured 50 Hz at ($m_a=0.8$) where the 3rd and 5th are eliminated by the generation of intended 3rd and 5th having the same amplitudes of the undesired one but with 180° as phase shift .

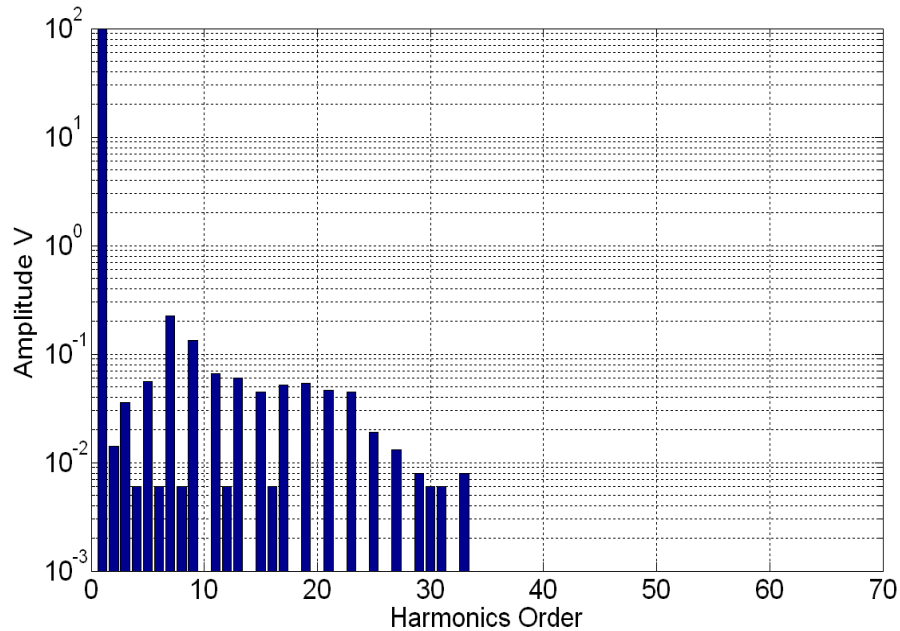


FIGURE 3.17: Eliminate the effect of dead time at the output voltage of Pec-HV

From the previous presented simulated and measured results, one can expect the system behaviour for all of the possible output voltage signal shape of the fundamental frequencies (16.7 Hz, 50 Hz and 60 Hz) with the exact desired THD, where difference between the desired THD and the produced by Pec-HV is roughly 1% at the worst case.

3.6 Characterisation of Low Pass Filter

As explained in clause 2.3, a proper attenuation ratio of the low pass filter has to be determined in order to attenuate the carrier sideband harmonics of the signal $V_{oh_{PWM}}$ in the frequency range of (100 kHz to 500 kHz), thus eliminating the background noise interference in the PD measurements. According to an experimental investigations, the attenuation has to be enough to keep any harmonic amplitude roughly in the range of 35 μ V to 5 μ V at the high voltage terminal of the tested object for the PD (back to figure 2.7).

To measure the sideband harmonics of the signal $V_{oh_{PWM}}$ in pC as seen by the PD MI an experiments in ETS lab is performed as the following:

1. Adjust the Pec-HV parameters and then measuring the signal $V_{oh_{PWM}}$ in the frequency domain using a measurement receiver according to CISPR-16-1-1. (figure 3.18)
2. Keeping the same setting of the Pec-HV and connect the device to a coupling capacitor and PD MI as seen in figure 3.18.
3. Measuring the PD in the frequency domain at different selected bandwidth.

The result of this experiments shows that the sideband harmonics have the value of roughly 1 pC if its amplitude is ranges from 5 to 35 uV within a selected measurement bandwidth from 9 kHz to 300 kHz.

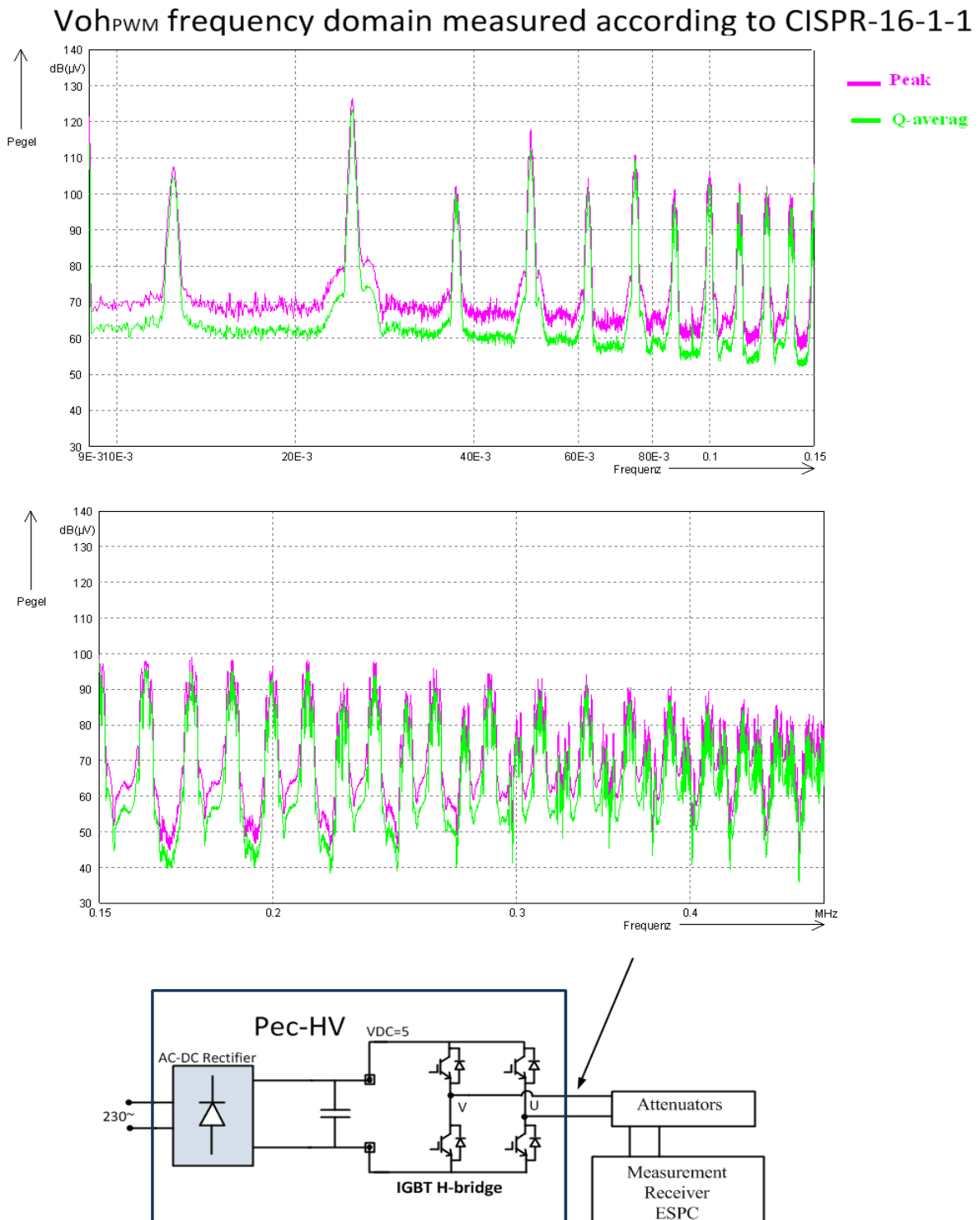


FIGURE 3.18: measuring the Pec-HV PD interference

From the presented results in clause 3.4.2-B, the highest harmonic amplitude appears around the harmonic order of $2*m_f$, and then start decreasing at higher frequencies. For the filter investigation, it is important to know the highest harmonic amplitude in the range (100 kHz to 500 kHz), which is expected around 100 kHz. The highest peak has to be determined at a various values of ma or with/without intended harmonics for the 3 fundamental frequencies.

Fundamental Frequency	without intended harmonics in V	With intended harmonics in V
16.7 Hz	0.3682	0.3527
50 Hz	0.2931	0.3529
60 Hz	0.3805	0.3658

TABLE 3.8: Highest voltage harmonics of the measured $V_{oh_{PWM}}$ in frequency range 99.8 kHz to 500 kHz

Table 3.8 shows the measured highest harmonic amplitude for the three fundamental frequencies using the same measurements parameters (ma=0.8 at VDC=10) and method which are mentioned in clause 3.4.2-B. As seen in the table the highest peak is 0.3805 V, since the relation is linear between VDC and the harmonics amplitudes (clause 2.5.2.1) so the maximum is $(320/10)*0.3805=12.176$ V, where 320 is the maximum VDC. The complete measured spectrum of the presented results shows that adding an intended harmonics will slightly influence on the amplitude of carrier sidebanded frequencies.

In order to observe the influence of ma at the harmonics amplitudes in the range (100 kHz to 500 kHz) a simulation is performed for the fundamental 50 Hz considering $dt=0.3$ us and VDC=1 V. The results are shown in table 3.9, keeping in mind that due to higher dv/dt of the simulated pulses than measured, the harmonics (carrier sidebanded frequencies) amplitudes are higher as well. Through reading the results in table 3.2 (clause 3.4.2-B) the amplitude difference between normalised measured and simulated carrier sidebanded harmonics is roughly 0.01 V. Therefore the value of 0.0546 V (0.0646-0.01) is adopted for the filter design as the highest harmonics amplitude. Since the maximum VDC=320 then the highest harmonic amplitude = $320*0.0546 = 17.472$ V. That means the low pass filter curve in addition to the test transformer must have a transfer function voltage attenuation of roughly -130 dB at 100 kHz to 500 kHz.

ma	highest peak V
0.2	0.030
0.3	0.0646
0.4	0.039
0.5	0.0594
0.6	0.0478
0.7	0.0543
0.8	0.0462
0.9	0.0485
0.99	0.0457

TABLE 3.9: Highest voltage harmonics peaks of the simulated (50 Hz) $V_{oh_{PWM}}$ in frequency range 99.8 kHz to 500 kHz at various ma

Frequency Response of the Test Transformer :

In order to design a proper Low Pass Filter, the test transformer's transfer function has to be known, especially for the frequency range from 100 kHz to 500 kHz. That can be achieved by building up a complete model for the transformer such presented in the references [67, 68] or by lab measurements investigations. Since the modelling methods are complex, the measurements investigations is chosen for this thesis.

For an accurate transformer transfer function measurements, the following have to be considered :

- Input impedance : The input in such usage for the transformer is the LPF and a low impedance voltage source (less than 50 Ω) whether it is the Pec-HV or the mains.
- The output impedance: Normally in the PD measurements the load at the transformer secondary is a capacitive voltage divider in addition to the PD coupling capacitor and the PD coupling device which is actually a high pass filter with 50 Ω .
- Transformer's Non-linearity: The transformer's irons core has a non-linear behaviour with respect to the primary voltage (for example 50 Hz), for that reason it is recommended to perform the measurements of the frequency response with presence of the mains voltage (50 Hz).

To perform a proper frequency response measurement and taking in account the previous bullets, the method of conducted immunity EMC test (IEC 61000-4-6) is simplified as seen in figure 3.19, where :

- A variable transformer is used to control the mains voltage amplitude at the primary and the LPF to separate the high frequency component from the mains in

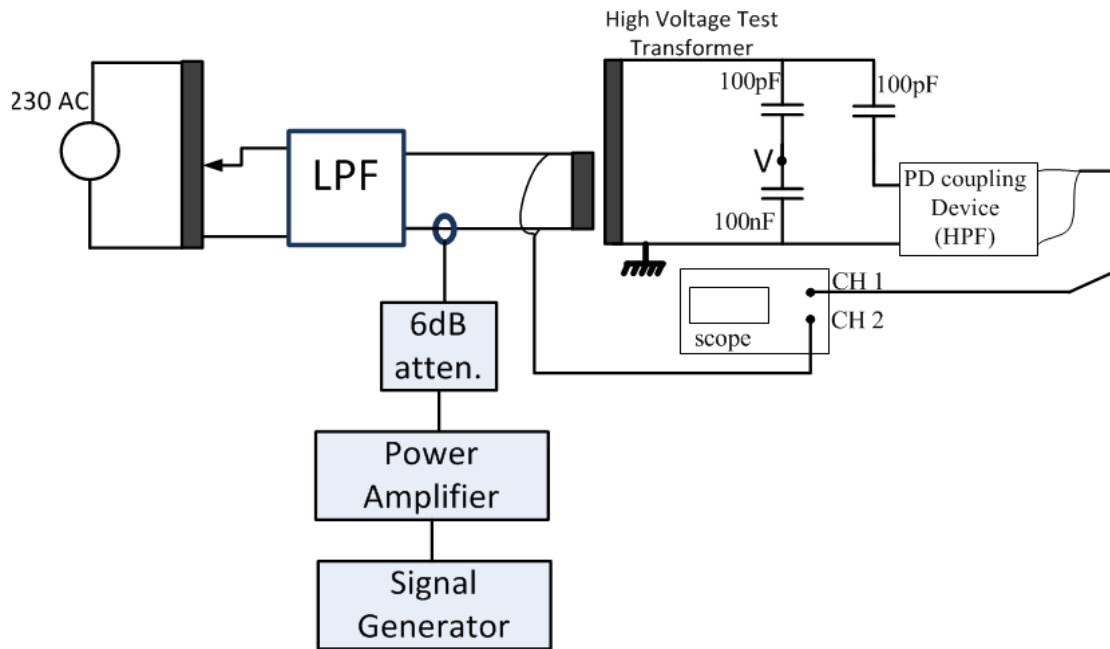


FIGURE 3.19: Measurement setup of the test transformer transfer function

addition to represent the real circumstances where a LPF is connected normally with the machine Pec-HV.

- A signal generator, a power amplifier and a current clamp are used to inject a sinusoidal signal in the frequency range of 100 kHz to 500 KHz.
- At the secondary of the transformer, a voltage divider of 1:1000 is connected in addition to a conventional (in pF) PD coupling capacitor and a HPF .
- An oscilloscope is connected to measure the primary voltage and the secondary to calculate the voltage transfer function.

To investigate the effect of the core non-linearity, the first measurements are performed as seen in figure 3.19 but without the PD coupling device and coupling capacitors, where the secondary voltage was measured through the capacitor voltage divider. The measurements are performed at selected frequency values from 10 kHz to 1.4 MHz where the mains voltage is 10 V_{rms} and then raised up to 190 V_{rms}. The results of this measurements are as seen in figure 3.20 which shows that the core non-literary is increasing the attenuations.

where:

- The red points are the selected frequency values among the interested range.
- V_{in} is the primary voltage.
- v_{out} is the secondary voltage.

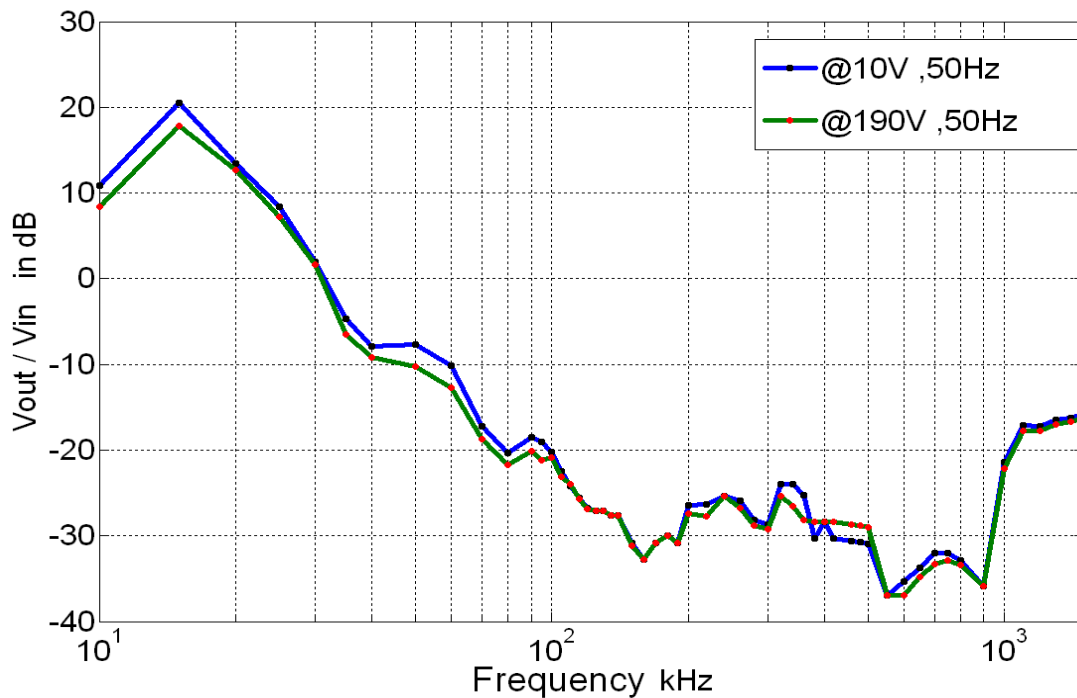


FIGURE 3.20: Core non-linearity influence on the transfer function

The measurement are performed again at the worst attenuation case (10 Vrms of the mains voltage) with connected the PD coupling device and capacitor as shown in figure 3.19. The results are shown in figure 3.21.

The curve in the figure 3.21 shows an attenuation of roughly -65 dB in frequency range of 100 kHz to 180 kHz then the attenuation is reduced to - 43 dB at roughly 300 kHz. The shown curve is measured at 10 Vrms of the mains 50 Hz voltage. Increasing the 50 Hz voltage will increase the attentions as measured before. The curve is different from figure 3.20 due to a different output impedance at the secondary of the test transformer (50 Ω of the PD coupling device). This result would be a positive point for the filter design complexity and cost.

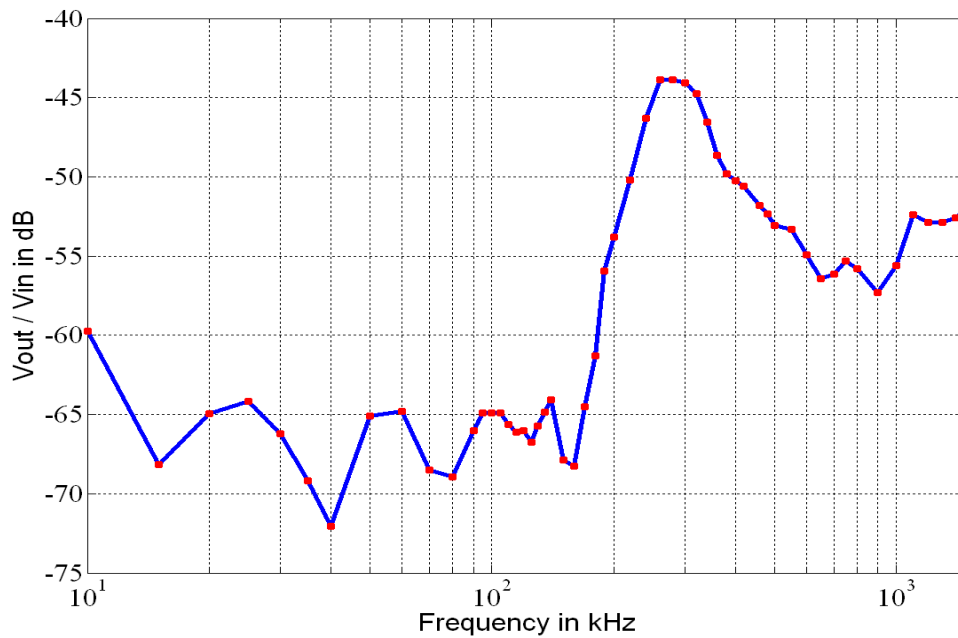


FIGURE 3.21: Frequency response of the test transformer

Low Pass Filter investigations :

According to the presented information in the clauses 2.3 and in this clause, a LPF as seen in figure 3.22 is selected to allow the usage of En-Unipolar-PWM for PD measurements. The filter consists of a sine-filter followed by multiple stages of low pass filters in order to achieve the required attenuations, that is in addition to transformer's attenuation in order to reduce or eliminate the $V_{oh_{PWM}}$ signal's harmonics interference with the PD measurements.

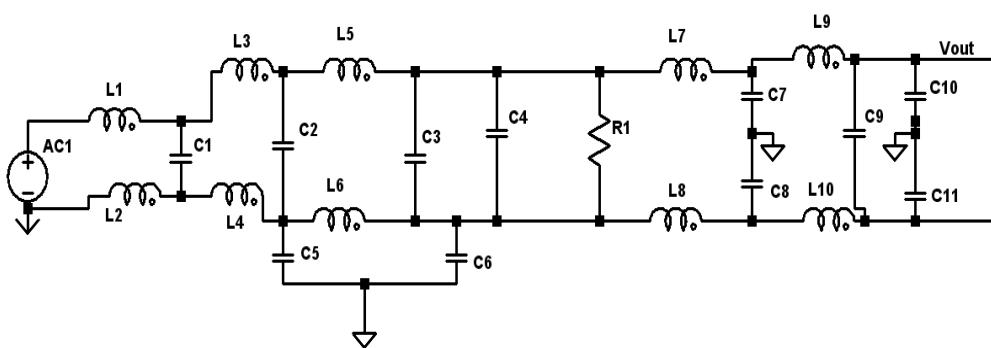


FIGURE 3.22: LPF Schematic diagram

Figure 3.23 shows the measured voltage-frequency response of the selected LPF, the frequency response curve were measured at the mains (low impedance) as input impedance and $1\text{ M}\Omega$ as output impedance. High output impedance is selected because it is more close to the real usage of the filter where it is normally connected to the test

transformer where it is used in the HV test investigations with an approximately open circuit secondary.

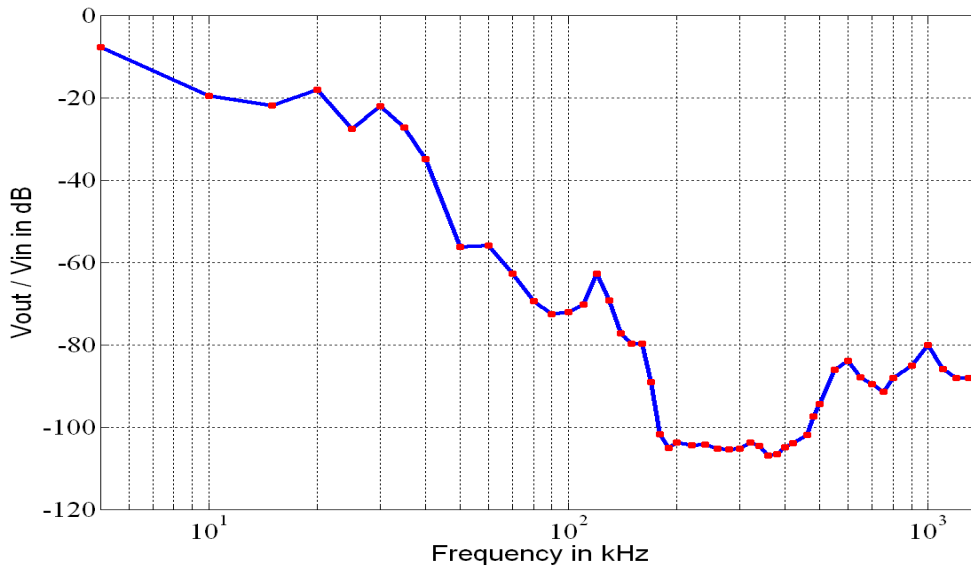


FIGURE 3.23: LPF, measured frequency response

Adding the two curves (figure 3.21 and 3.23) shows a satisfying voltage attenuation for the frequency range of 100 kHz to 500 kHz as seen in figure 3.24.

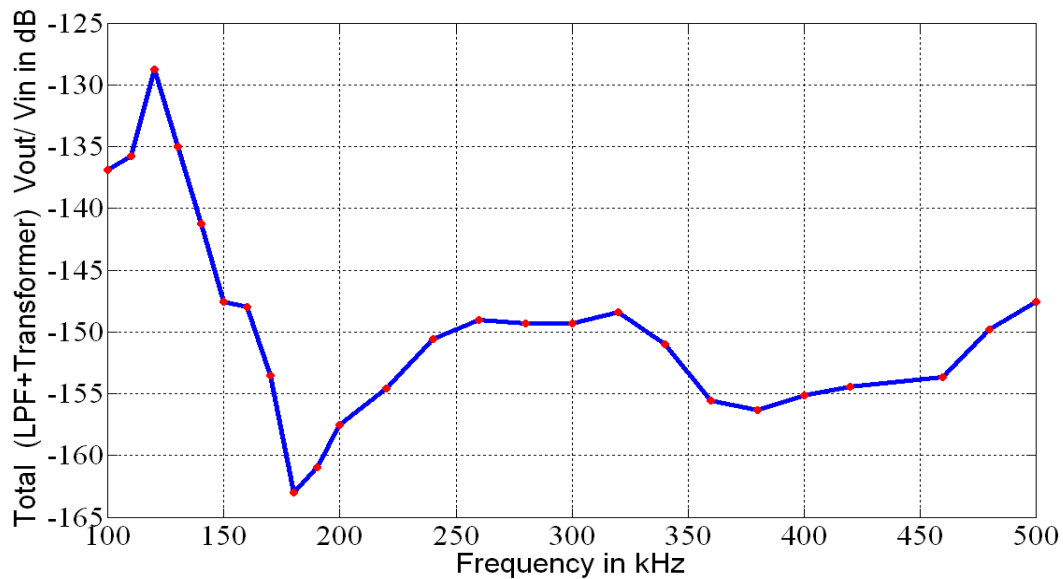


FIGURE 3.24: The total transfer function V_{out}/V_{in} of the LPF and the transformer

The harmonics amplitudes of the signal $V_{oh_{PWM}}$ are getting smaller with the respect to increasing the frequency, i.e the highest harmonic amplitude in the interesting range (100 kHz - 500 kHz) is at roughly 100 kHz, then higher frequency harmonics amplitudes are getting decrease (figure 3.9), while the attenuation due to both (LPF and transformer) are increasing with respect to the frequency as seen in the figure

above, that is an adequate attenuation to eliminate the background noise interference in PD measurements.

The filter is tested for all the expected dynamic singles output which the Pec-HV can produce. Figure 3.25 shows one of this results where the background noise is less than 1 pC.

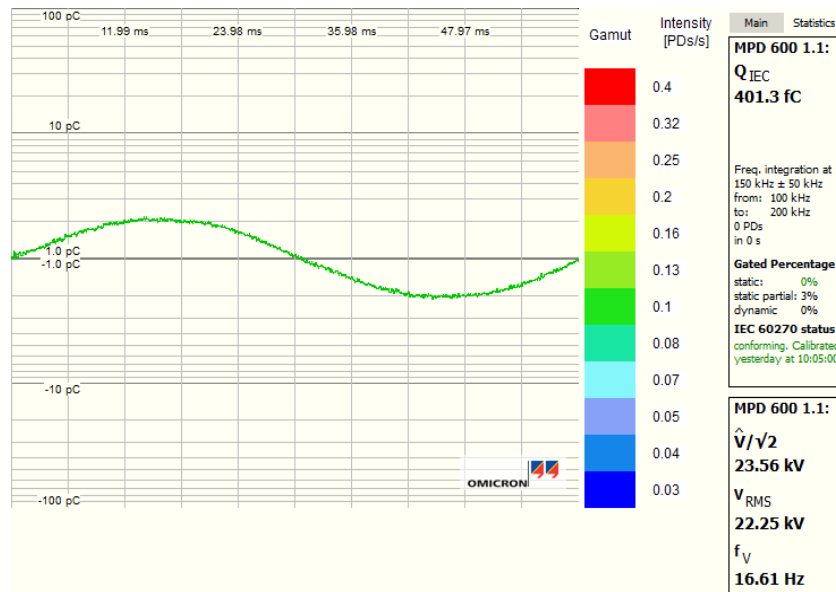


FIGURE 3.25: Elimination of the Background noise in PD measurements

3.7 Pec-HV Protection unit

As mentioned in clause 1.1.2 and 2.2, the voltage breakdown is an expected result of the DI-HV test, where the current could raise up to a destructive values especially if the test voltage source has not been interrupted very fast (within few 10's of us). To avoid any kind of damage in the test system, a protection unit based of the current raise up time (di/dt) at the primary side of the test transformer and on the voltage fall time (dv/dt) at the secondary. Figure 3.26 shows how the protection unit is integrated with the Pec-HV. A special algorithm is programmed and implemented in the DSP of the protection unit(PU-DSP) ,the PU-DSP will interrupt the IGBTs switching process in a case of voltage breakdown and/or if the current exceeds a certain limit. An operational amplifier circuit is designed to match between the current(I) measuring point at the primary part and the ADC of the PU-DSP circuit.Also Another operational amplifier circuit is designed to match between the divided voltage (V) at the secondary and the ADC of the PU-DSP.

The Algorithm is programmed to detect the voltage breakdown according to a comparison between the read samples (figure 3.27). The idea briefly is to find out the sum of the first three sampled values together, then to find out the sum of the next three samples and then to find the difference absolute value between the two summations(step). The number three (3 samples) is experimentally determined, where

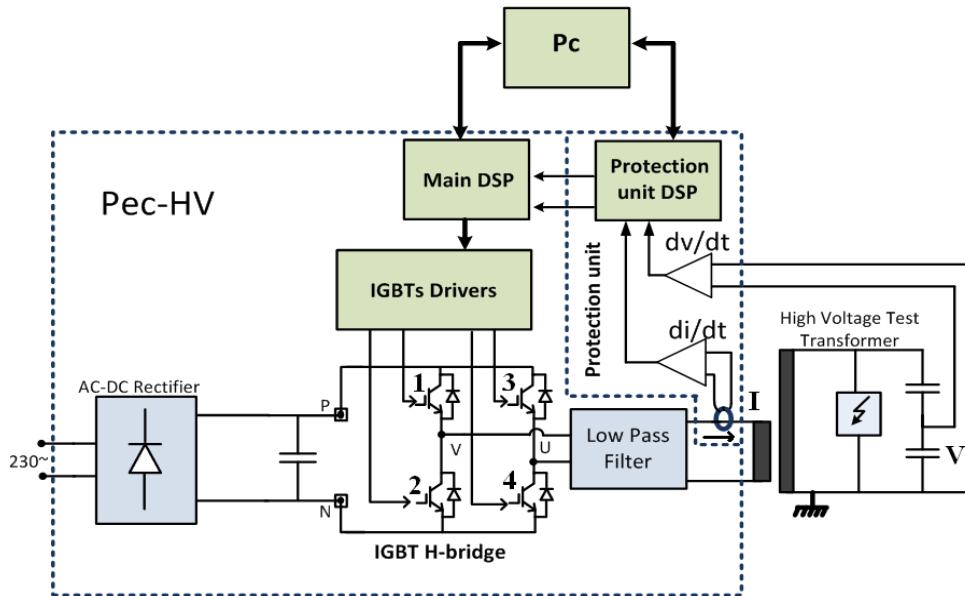


FIGURE 3.26: Overview schematic of the Pec-HV and the Protection Unit

taking more than three samples consume more calculation time and less than three will increase the detection error. If the calculated step is less than a dynamic pre-calculated threshold, the process will be repeated again, and if the step is higher than the threshold, a breakdown is detected and a trigger signal will be sent to the main DSP (figure 3.26) in order to stop the IGBT's switching process. If the main DSP receives the trigger signal from the protection unit, then IGBTs 1 and 3 will be opened and 2 and 4 will be closed, thus reducing the injected energy in the breakdown channel.

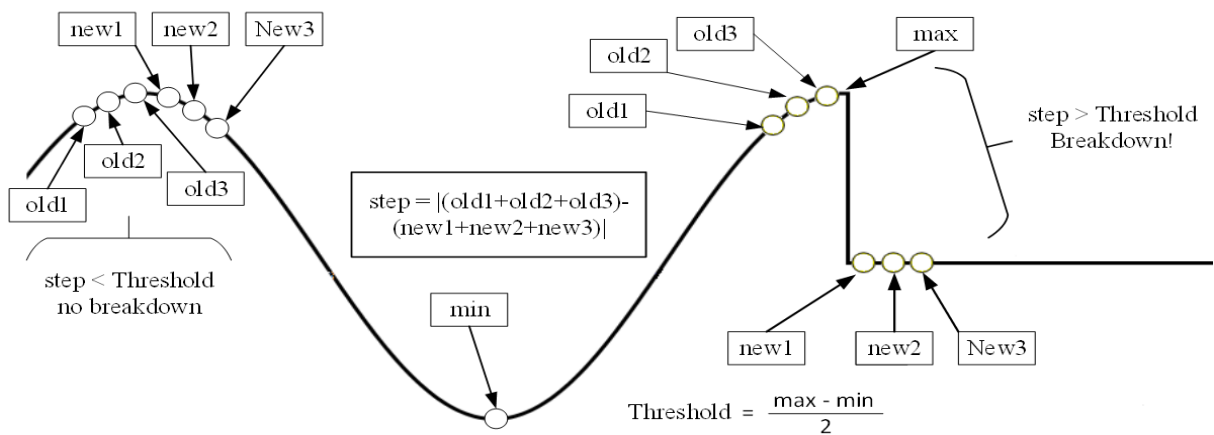


FIGURE 3.27: Breakdown detection algorithm

The time of the detection process and thus the total switching off/interrupting the test voltage source is depending on the sampling time of the ADC and a propagation delay of the trigger signal as well as the IGBTs gate signals to close/open the desired IGBTs as explained before. The sampling time is experimentally adjusted to be 10us where faster time gives more detection error, as well as the consumed time of calculating

the step value must be less than the sampling rate, in other words no samples will be missed. The overall measured switching off time of the H-bridge in case of a detected breakdown is roughly 50 μ s.

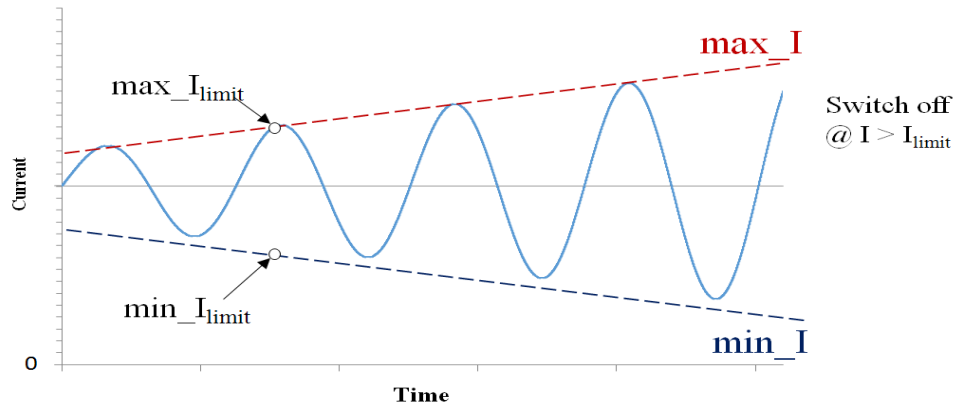


FIGURE 3.28: Protection against destructive current

The protection against any high raise up current is required, not only at the case of breakdown, but as a general protection from any unexpected cases. The device Pec-HV can be used to accomplish the HV-DI test and PD measurements where a step up transformer is installed to generate the high AC voltage. The maximum current of the primary's transformer coil could be less than the capable one of the Pec-HV, that is in addition to the destructive current value which can raise up rapidly in case of voltage Breakdown. Therefore a programmable limit (max_Ilimit and min_Ilimit) as seen in figure 3.28 has to be determined, where max_I is the maximum current positive peak value of the H-bridge module which is (50 A) and min_I is the negative peak. Interpreting the switching process will executed in case of exceeding the value of max_Ilimit or beneath the value of min_Ilimit . The interruption is executed in the same way as explained for the voltage-breakdown case.

4. Experimental Procedures and results

4.1 HV Test-source signal preconditioning

The previous presented THD measurements in the figures 3.11 to 3.17 were performed at the output terminals of the Pec-HV (no load was connected). In this clause as well as the following clauses, all measurements/test were accomplished while a high voltage step up transformer is connected to the Pec-HV.

Figure 4.1 shows the Pec-HV test's setup in the high voltage lab at the University of Duisburg Essen. Pec-HV is connected to the 100 kV, 5 kVA transformer, the Network Harmonic Analyser (NWA) is connected in parallel to Pec-HV to measure the voltage THD of the test's signal, the same THD will transferred to the secondary windings, since the secondary can be approximately considered as an open circuit. For the PD measurements the Omicron device MPD600 was connected through a fiber-optic, quadripole as a coupling device and 100 pF as a coupling capacitor to the HV transformer. The system is calibrated for the proper PD measurements.

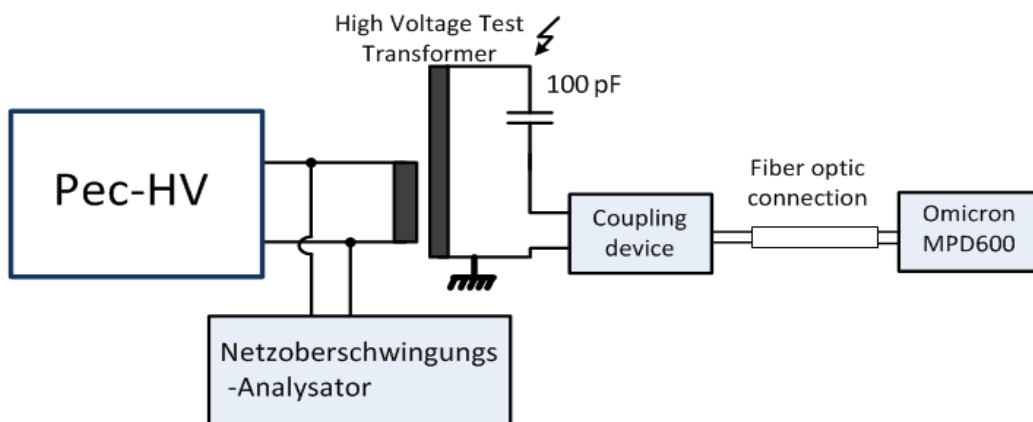


FIGURE 4.1: PD measurements setup in high voltage lab

The Pec-HV was started up to work in free harmonic mode (without intended harmonics) at the fundamental 50 Hz, nevertheless a THD of roughly 4% is measured by the NWA as seen in figure 4.2. These undesired harmonics are produced due to the iron core nonlinearity of the transformer (clause 2.4.2).

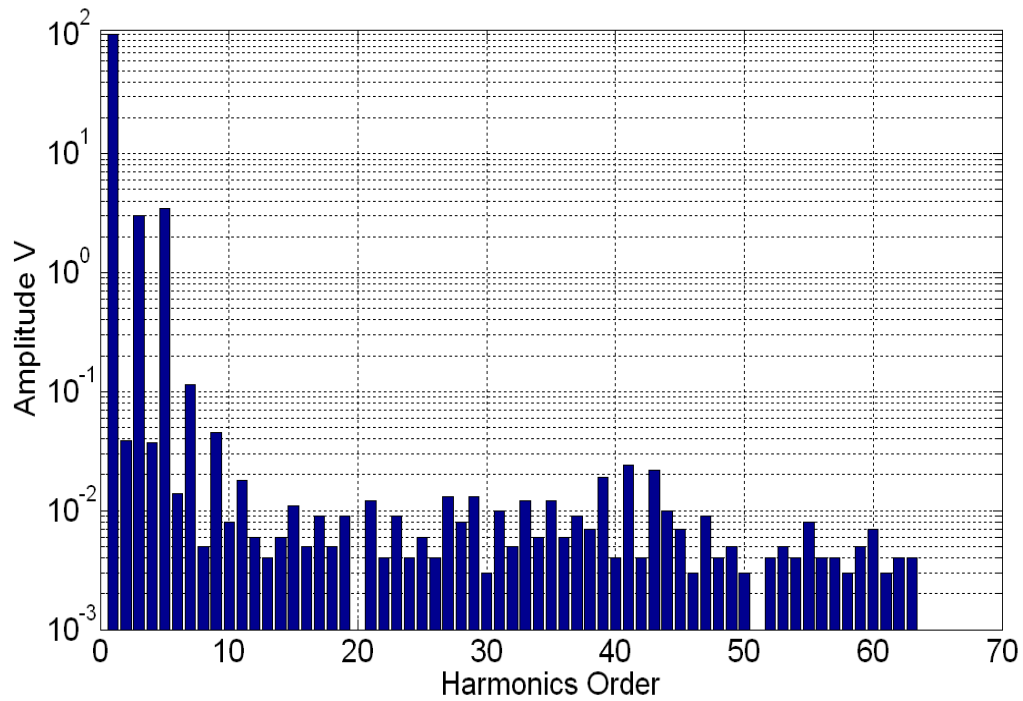


FIGURE 4.2: Undesired harmonics produced by the non-linear core of the test transformer

Since the Pec-HV is able to generate intended 3rd and 5th harmonics, it is possible to compensate the undesired generated ones and thus preconditioning the test's signal quality by reducing the THD to roughly 0.5% (Figure 4.3). The compensation can be done by generating the same undesired harmonics amplitudes, but with 180° phase shift

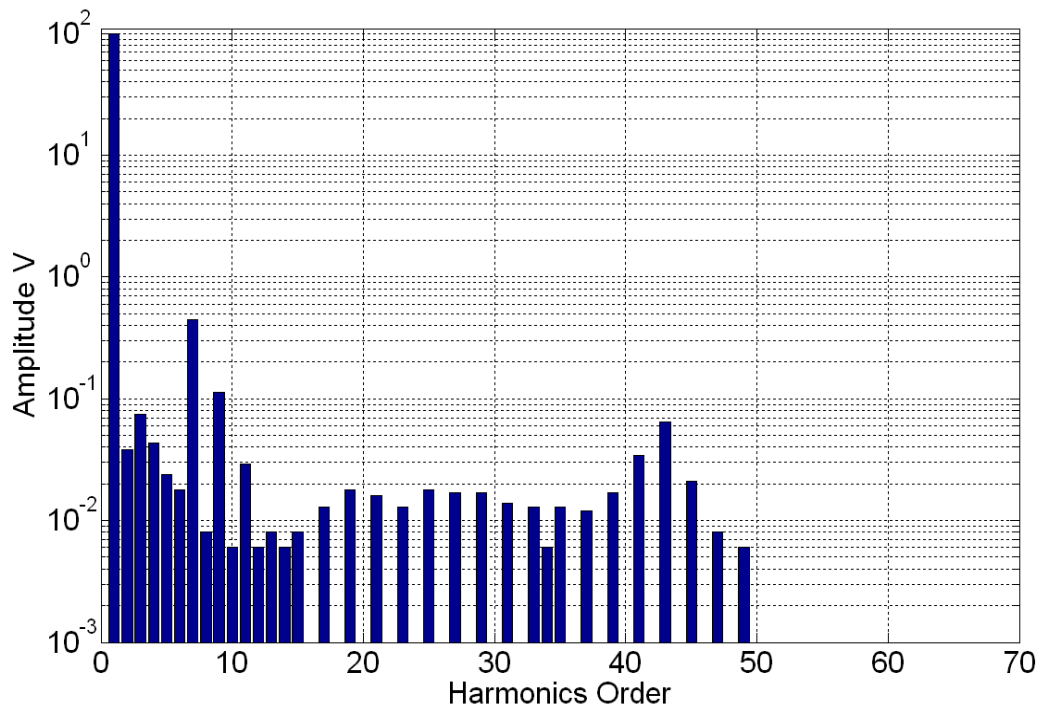
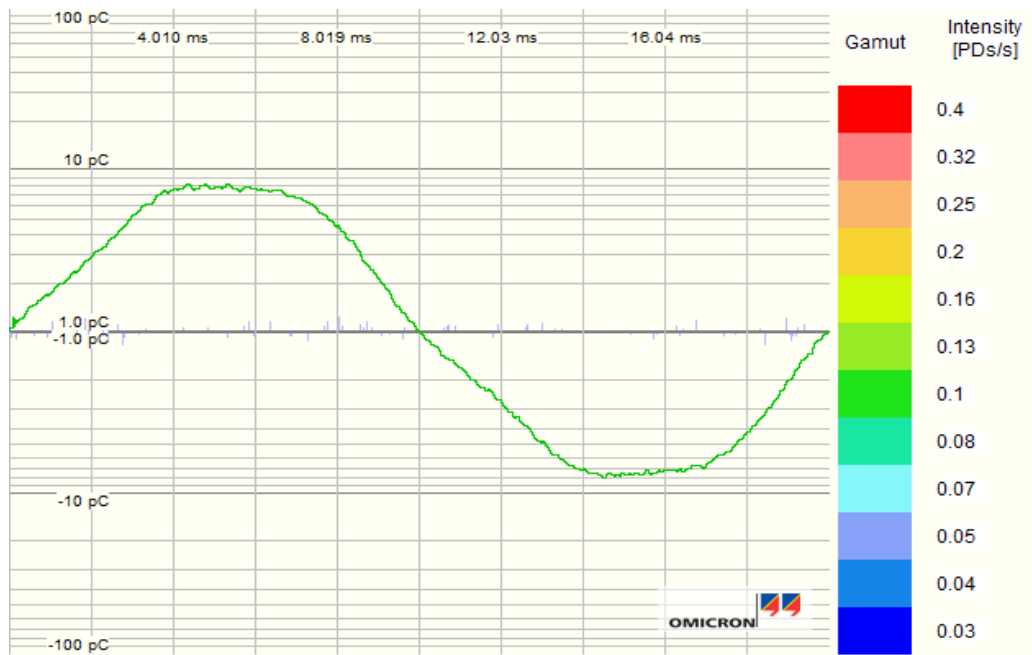
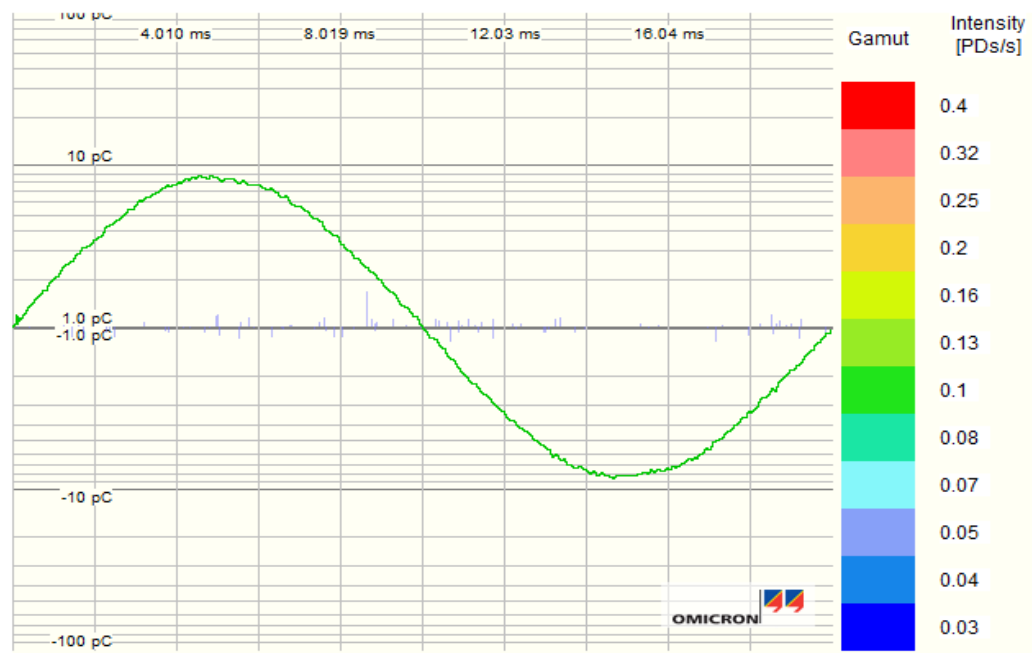


FIGURE 4.3: Test source signal preconditioning-compensation of the undesired harmonics

Figure 4.4 shows how the signal preconditioning improves the test's signal quality as seen by the PD measurements device, where 4.3 (a) shows the THD due the iron core and (b) shows the test signal after the compensation of the undesired harmonics.



(a) Without undesired harmonics compensation



(b) With undesired harmonics compensation

FIGURE 4.4: Test source signal preconditioning-compensation as seen by PD MI

4.2 Fast switch off and Voltage Breakdown test

The second aim of this thesis is a reliable fast interrupting of the test voltage source in case of breakdown during the DI-HV tests. Figure 4.5 shows the experiment test setup in HV-lab, where the primary current I is observed through a current probe by CH2 of an oscilloscope and the secondary divided voltage V by CH1. The point V is connected as well to the dv/dt input of the Pec-HV's protection unit. Two spheres was connected to the secondary to simulate a breakdown in the air as dielectric material. The experiment was performed at various distances between the spheres as range of (5 mm to 40 mm), the machine Pec-HV was started up and voltage was increased gradually, depending on the adjusted distance the breakdown was detected at nearly 24 kV peak up to nearly 100 kV peak. This range of breakdown is tested at the fundamental frequencies of 50 Hz and 60 Hz, while at 16.7 Hz the maximum possible voltage to apply is $\frac{1}{3}$ of the nominal transformer's primary voltage (220/3) V , thus the maximum HV at the secondary is roughly 34 kV RMS.

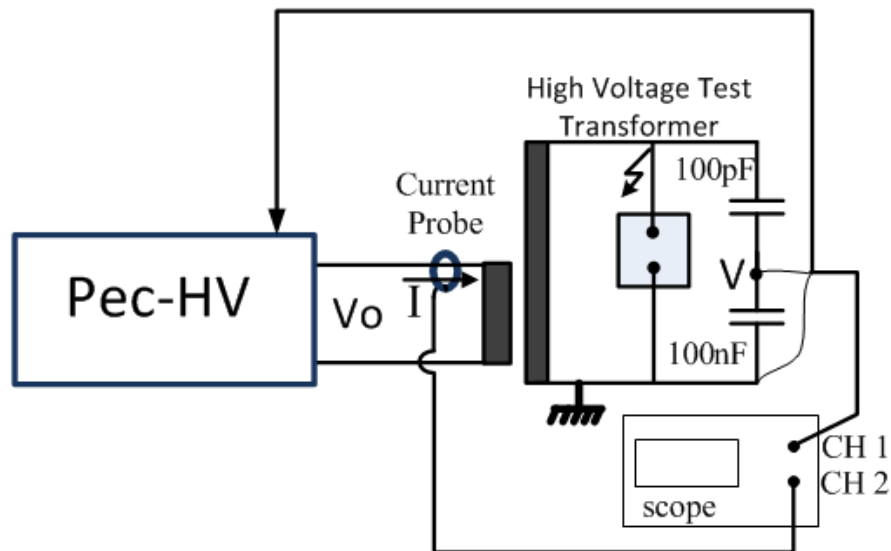


FIGURE 4.5: DI-HV Test setup in high voltage lab

Figure 4.6 presents one of the performed tests at 50 Hz where the distance between spheres was 5 mm. Both figures are for the same experiment but at different time scale. The voltage breakdown occurs at 24 KV peak, due to that the current raised up rapidly. Simultaneously the protection unit detected the breakdown voltage and current. At the moment of detecting the breakdown, the protection unit will send a trigger in order to interrupt the H-Bridge switching process. The detection and interrupting process as seen in figure 4.6 takes roughly $50\mu s$. The voltage signal oscillated rapidly at the moment of breakdown, that is due to the capacitive voltage divider (figure 4.5). since the voltage has to sink to zero value within nano seconds, the capacitors are not able to be discharged in this fast time, thus the voltage will oscillate within few micro seconds unit the capacitors are completely discharged.

Regarding the time $50\ \mu\text{s}$:as explained in 3.7 , the dv/dt algorithm has a sampling time of $10\ \mu\text{s}$, that means the programmed algorithm takes $30\ \mu\text{s}$ after the breakdown to read another 3 samples, another nearly $10\ \mu\text{s}$ to calculate the difference absolute value, where the rest $10\ \mu\text{s}$ is trigger propagation delay and switching off/on the IGBTs of the H-bridge.

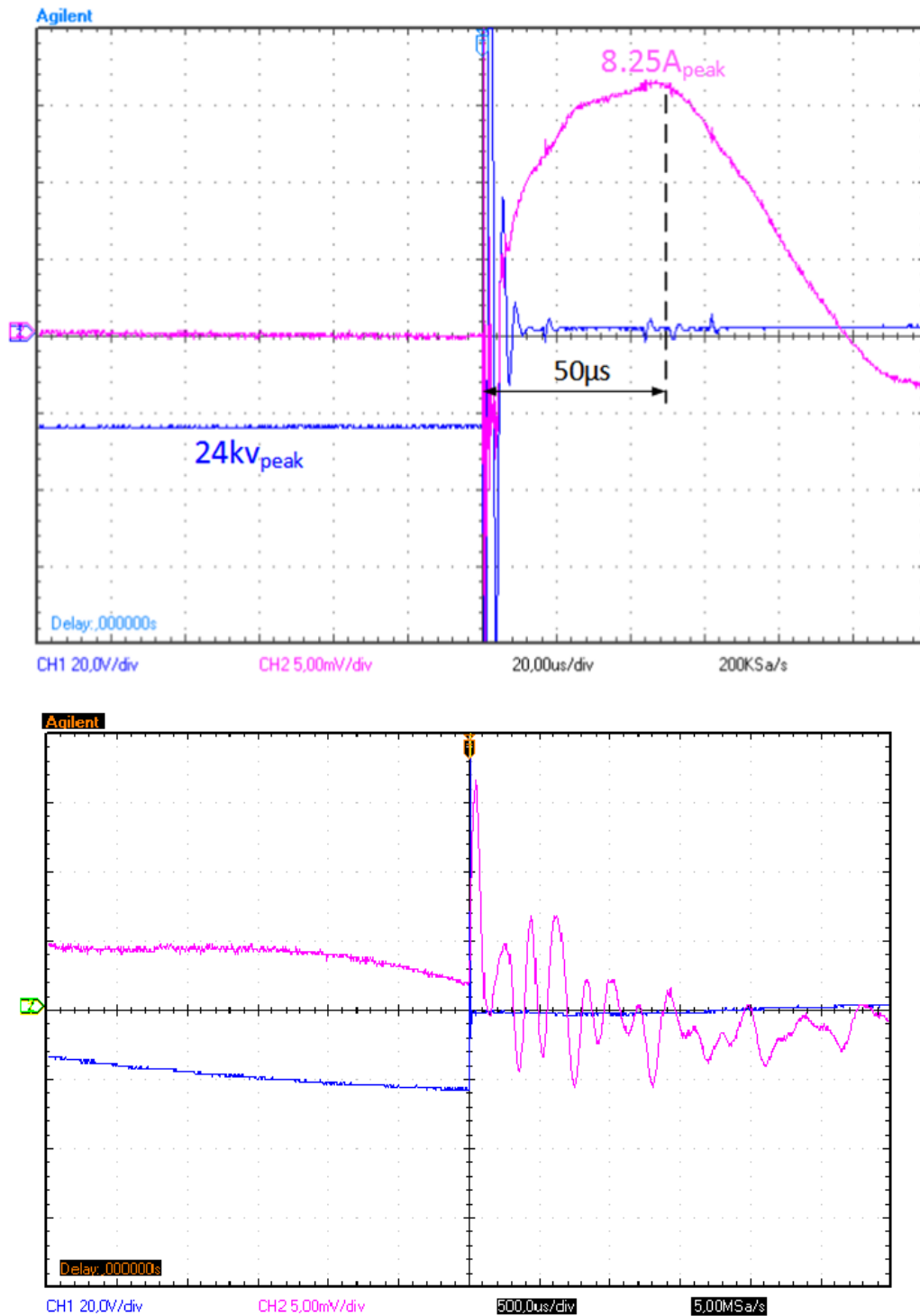


FIGURE 4.6: Interrupting the H-bridge switching when a breakdown is detected

4.3 Partial discharge measurements test

The third aim is to reduce the PD measurements background noise when the measurements are fed by the Pec-HV as a power source. The test was setup in the same way as in clause 4.1 (figure 4.1). The background noise has to be evaluated for the three selectable frequencies (50 Hz, 60 Hz, 16.7 Hz). In this test the signal preconditioning was not performed while the main point from the test is to observe the background noise level.

The figures 4.7 (a, b and c) presents the measured (in pC) level of the background noise according to the standard IEC 60270 for the three selected fundamental frequencies.

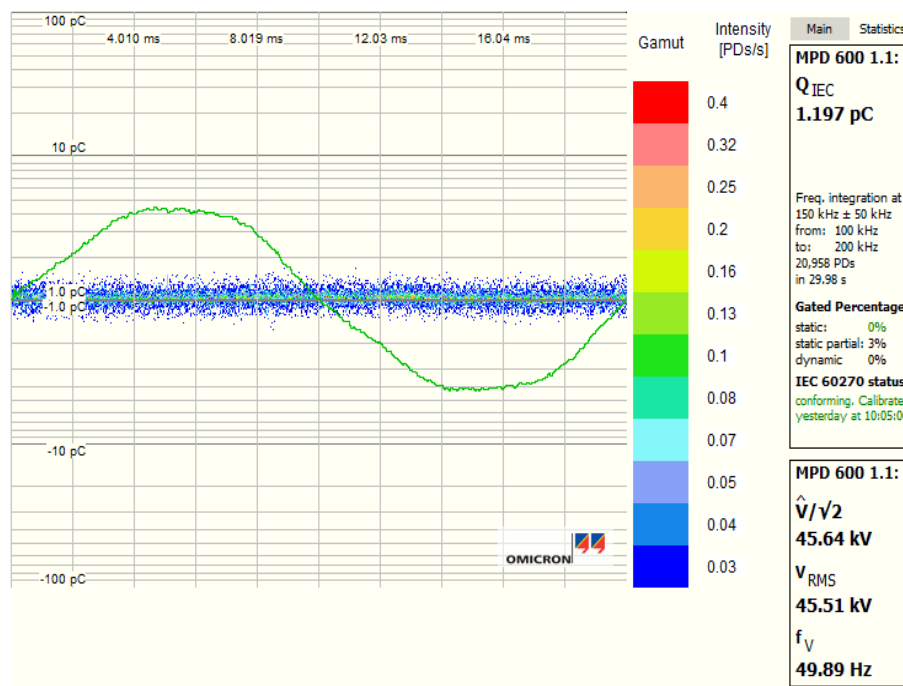
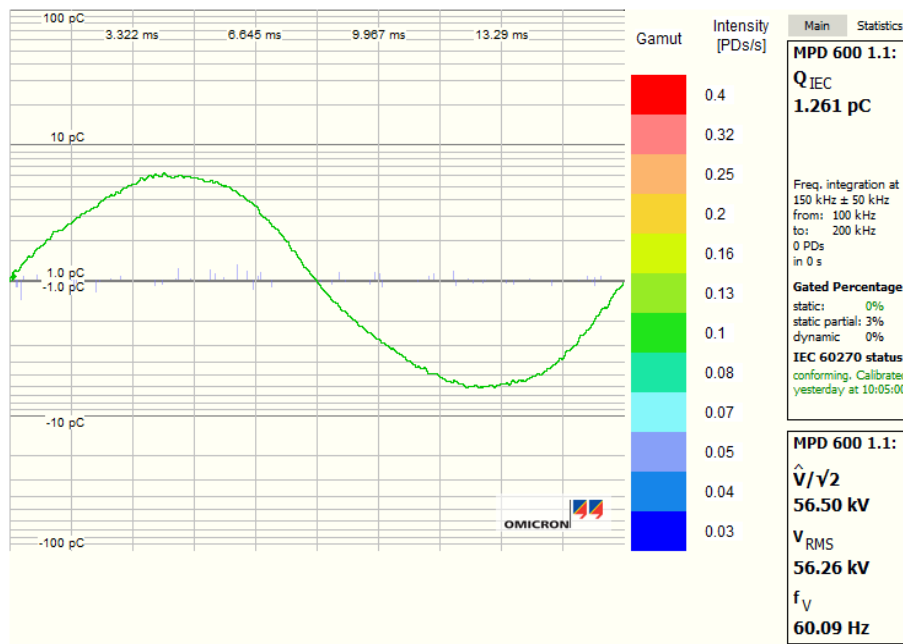
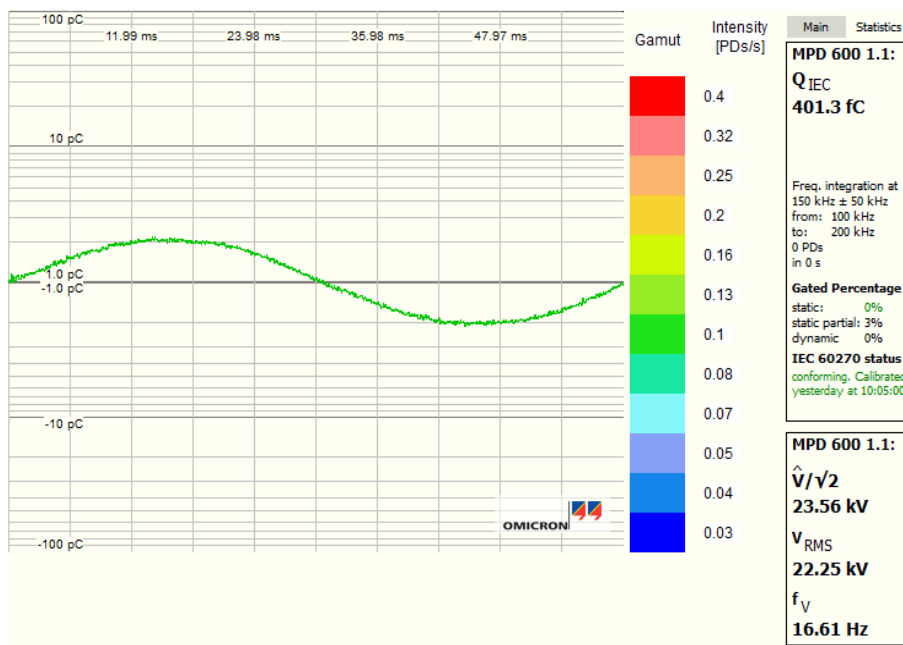


FIGURE 4.7: (a) Background noise in PD measurements at 50 Hz

The background level is measured within the bandwidth (100 to 200 kHz) and ranges from (0.4 to 1.2 pC) for the three cases (50 Hz, 60 Hz, 16.7 Hz). It is obvious as seen in figure 4.7 that the noise is proportional with the voltage level (if measured within the same bandwidth). As explained in clause 3.6, the highest carrier sidebanded frequencies are more close to 100 kHz, that means if the measurements band width is shifted (e.g : 200 kHz to 500) the background noise will be reduced to be less than 1 pC. In this case the measurements bandwidth is still within the recommended range according to (IEC 60270), but f_1 (figure 2.8-b) is out of the recommended range. Since the PD pulses has a wide spectrum range and through many lab experiment, it has been noticed that this shift of f_1 will not change the value of PD in pC in case of having real PD (adding a pin at the high voltage terminal).



(b) Background noise in PD measurements at 60 Hz



(c) Background noise in PD measurements at 16.7 Hz

FIGURE 4.7: Background noise level in PD measurements

4.4 Partial discharge measurements and intended harmonics

Generation of intended harmonics is a significant feature of the Pec-HV, it is required for the signal preconditioning, as well as for an experimental PD measurements investigations where a specific controllable amount of harmonics are needed.

Pec-HV is able to generate 3rd and 5th harmonics. The harmonics amplitude and phase shift (with respect to the fundamental frequency) are controllable.

Again the same test setup of figure 4.1 was used for this test experiment. The test was accomplished for the three fundamental frequencies at various amount of 3rd and 5th harmonics amplitudes. The voltage peak of the generated signal (fundamental + intended harmonics) must be within the linear region of the system (figure 2.20). In other words the peak voltage of the signal V_{sine} in figure 3.2 must be less than the peak of V_{tria} . Through these experiments it was noticed that generating the harmonics dose not effect on the background level.

Figure 4.8 shows one the performed PD measurements where a pin is fixed at the high voltage terminal to simulate a real PD pulses. The machine Pec-HV is started up without the generation of intended harmonics in as seen in figure 4.8-(a), where a 5th harmonic of 10% of the fundamental frequency's amplitudes was generated as seen in Figure 4.8 (b) .

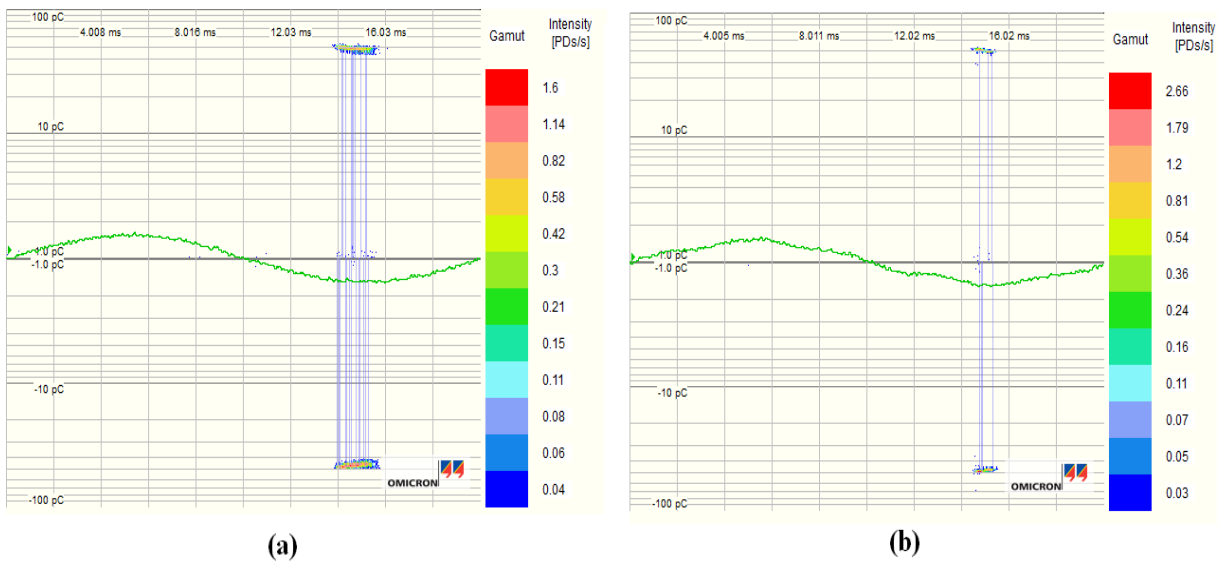


FIGURE 4.8: Stimulated PD corona measurements (a) Without intended harmonics . (b) with 10% 5th harmonic

The interested point for this thesis, is the quality of the generated signal, in other words the deviation between the required THD and the generated one. Figure 4.9 shows the quality of the generated 10% of the 5th harmonics where the measured THD is 10.02 % .

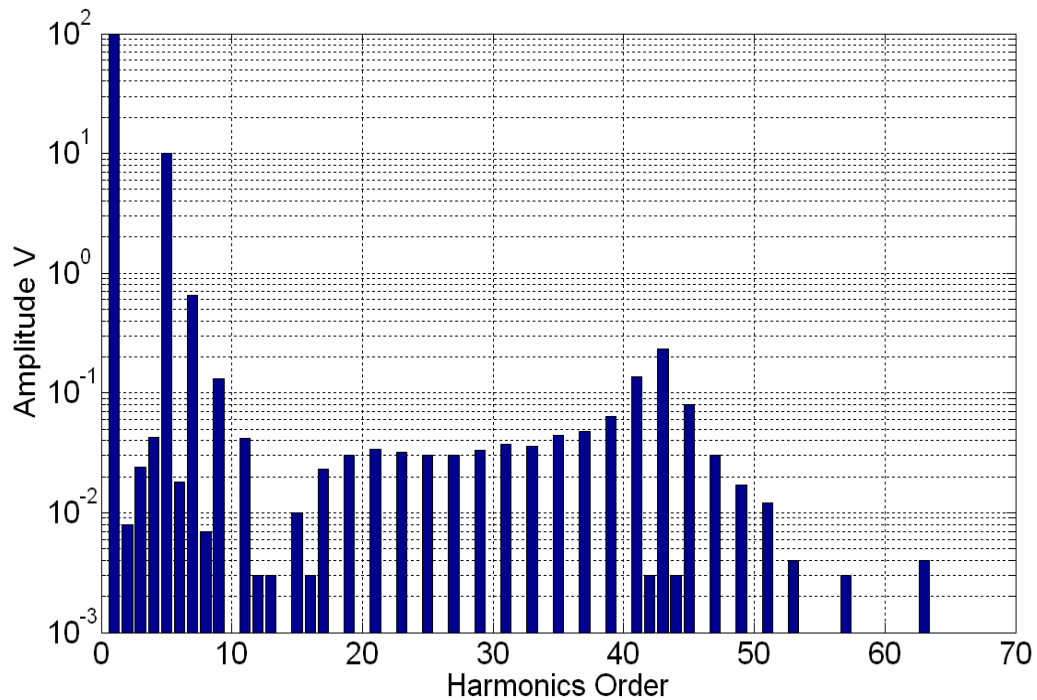


FIGURE 4.9: The quality of the generated intended harmonics for PD

4.5 Further Pec-HV Application

The Pec-HV algorithm is modified to produce a high frequency (up to 2 kHz) voltage sinusoidal signal which can be converted to a high current signal through a current transformer (up to 200 A in this measurements), this high current variable frequency signal is used for the shunt impedance measurement.

Modifying the En-Unipolar-PWM

Modifying the Pec-HV switching algorithm in order to produce the required high frequency signal is a challenge, since the impeded instructions in the DSP need to be processed much faster in this case (i.e 500 μs at 2 kHz) in order to complete the sine cycle.

According to experimental investigations, the best solution is to keep the triangle carrier frequency fixed, while the desired sinusoidal frequency is changeable (figure 4.10). In this case m_f or in other words the processed duty cycles per sine cycle are variable. The modified algorithm named High frequency(HF)-Unipolar-PWM.

Figure 4.11 Summarizes the implementation method of the HF-Unipolar-PWM in the DSP. The same as the previously explained about the EN-Unipolar-PWM where a duty cycles table is stored in the DSP (250 value), these duty cycles are calculated at 50 Hz sine by the MEN-Unipolar-PWM. The ISR time will depend on the selected frequency (equation 4.1). The carrier triangle time period is fixed here to roughly

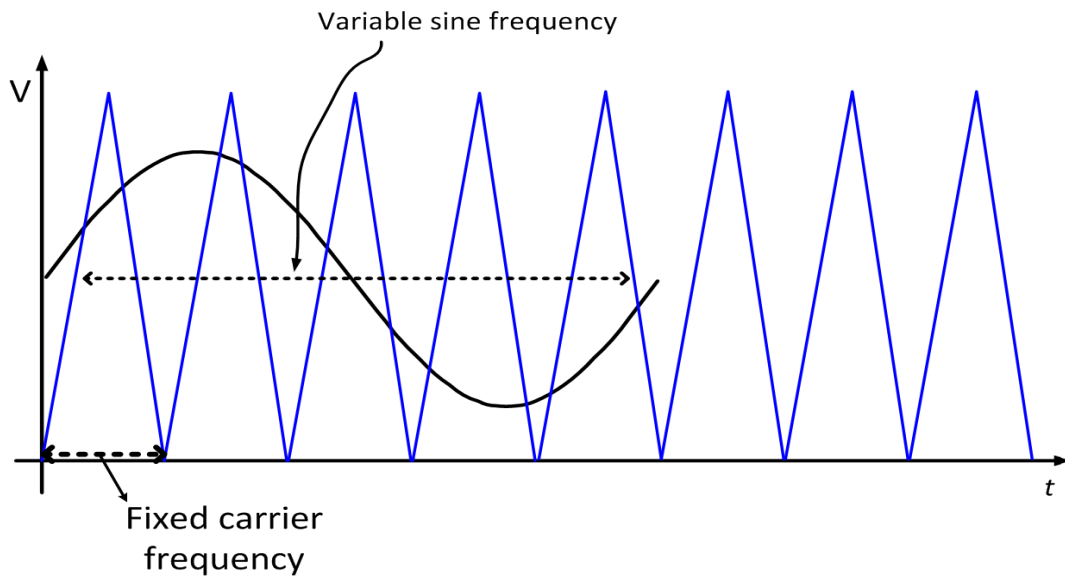


FIGURE 4.10: Modifying the switching algorithm to produce high frequency sine

$80\mu s$. The duty cycle value remains the same during the $80\mu s$. Therefore less duty cycle values will be processed when increasing the sine frequency. This will not sharply reduce the quality of the required sine signal. The signal quality was tested using the a computer sound card scope program since the THD can be measured up to 20 kHz. The signal worst THD is roughly 3.5% (through the frequency range 50 Hz to 2 kHz)

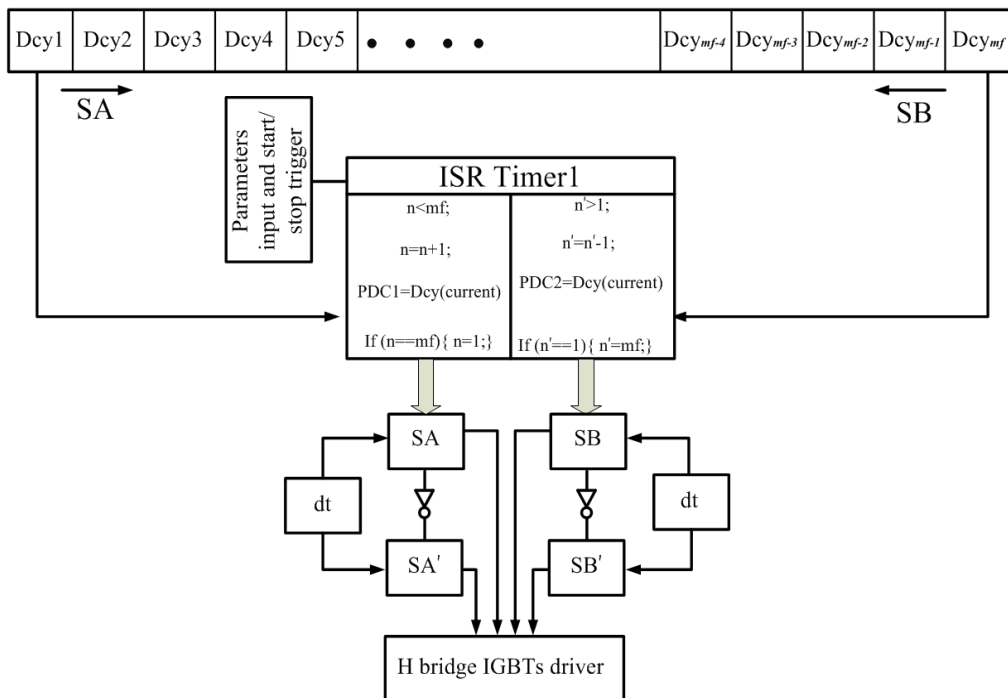


FIGURE 4.11: The implementation of the HF-Unipolar-PWM

$$ISR\ Time = \frac{1}{F * m_f} \quad (4.1)$$

where :

- ISR Time is the required time to update the duty cycle register in second.
- F is the desired sinusoidal frequency .
- m_f is the fixed m_f value at 50 Hz.

Figure 4.12 shows as example a 2 kHz sinusoidal signal produced by the HF-Unipolar-PWM measured at the output terminals of the Pec-HV, where the same characterised LPF is employed to filter the carrier frequency and its side-band harmonics.

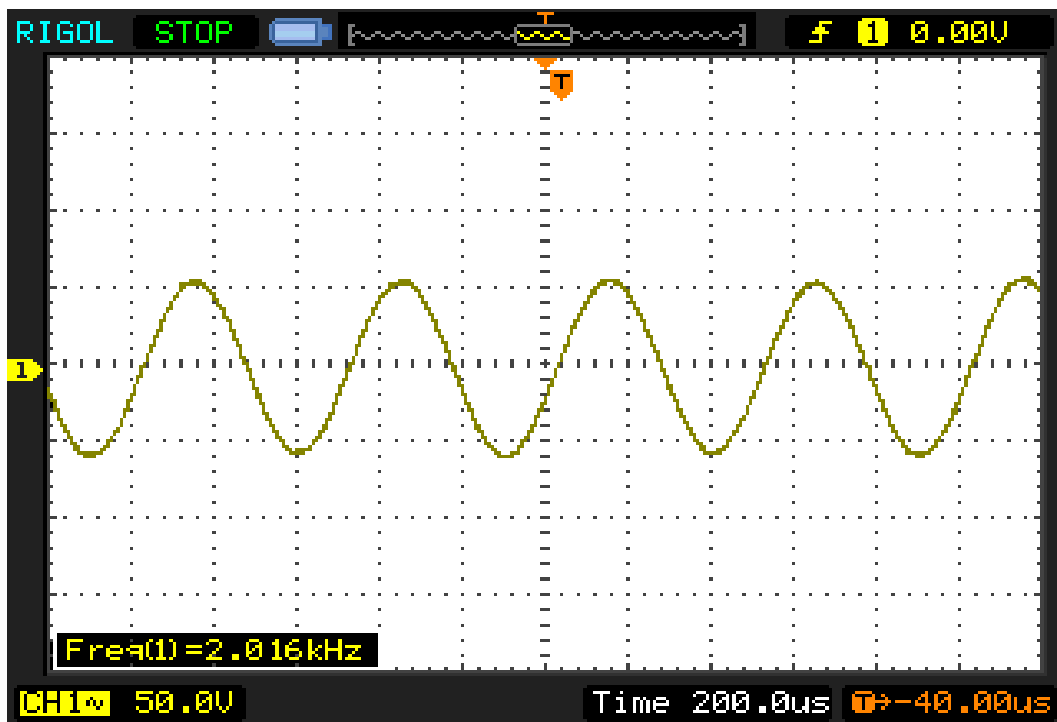


FIGURE 4.12: 2 kHz generated sine by HF-Unipolar-PWM

Shunt Impedance Measurement

The measurements are performed in the Lab of the University of Duisburg Essen. Figure 4.13 shows the measurements setup, where a current transformer is used to produce the required high current for the measurements, since Pec-HV has a maximum current capability of 6 A the maximum current at the transformer secondary is roughly

200 A. The shunt resistor is connected at the secondary of the current transformer, while a voltage drop at the shunt is measured using a low voltage measurement device and the current is measured by a current probe and a scope. The shunt impedance is then measured at a selected frequency values to cover the range from 50 Hz to 2 kHz. Figure 4.14 shows the result of this measurement, where the shunt impedance is slightly varied with the frequency.

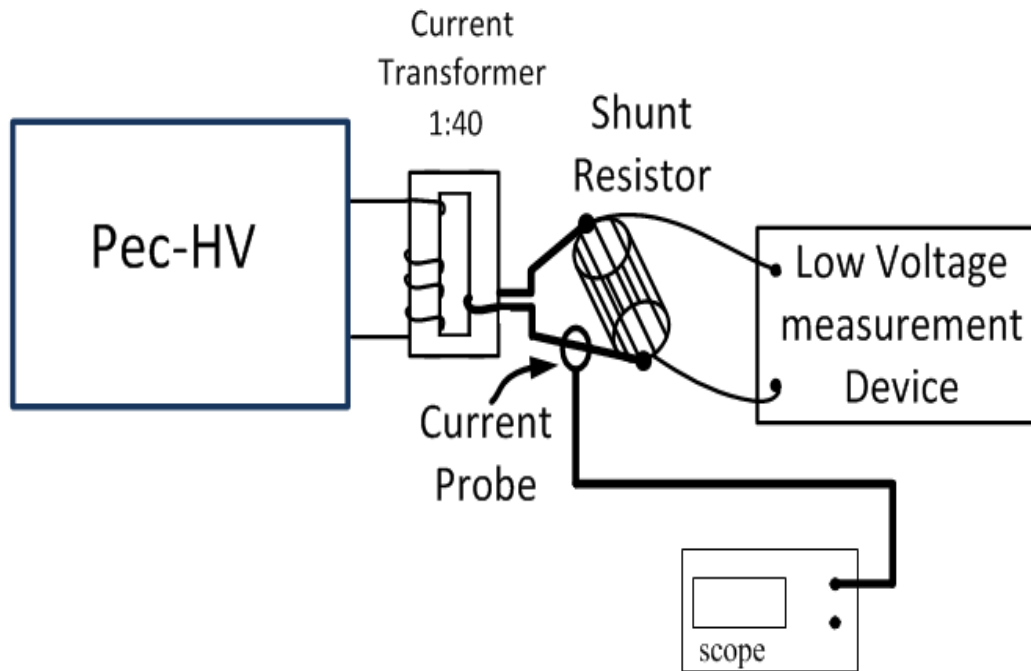


FIGURE 4.13: Shunt impedance measurement setup

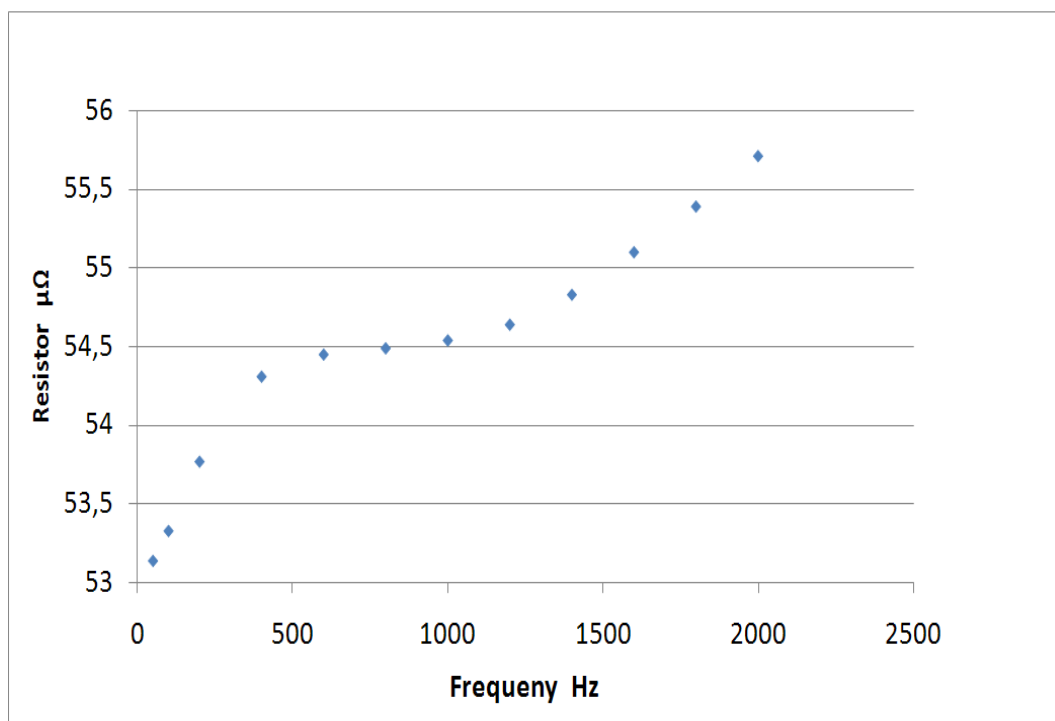


FIGURE 4.14: Shunt impedance with respect to variable frequency

5. Conclusions and Future work

5.1 Conclusions

In this dissertation, the use of pulsed power electronic device for high voltage testing is investigated and demonstrated experimentally.

The device Pec-HV core is a DC-AC Frequency converter/Harmonic generator based on the new Enhanced Unipolar Pulse Width Modulation Algorithm for one phase full bridge inverter (En-Unipolar-PWM). The PWM carrier frequency (triangle) and modulating frequency (desired sinusoidal) intersection points calculation problem was solved. The En-Unipolar-PWM algorithm was modelled using Matlab programming platform in order to calculate duty cycles corresponding to the intersection points and to simulate the algorithm outputs. The calculated duty cycle values stored in a digital signal processor (DSP) which controls the PWM switching process. The new MEn-unipolar-PWM Matlab model is able to handle all the system parameters including dead time, desired out put amplitude, harmonics amplitude, switching frequency and phase shift between the IH and the fundamental frequency.

The En-Unipolar-PWM algorithm was embedded in a suitable DSP and all the required hardware elements were designed/combined in order to accomplish the Pec-HV. Electromagnetic compatibility issues such, EMI and EMC filters, grounding and shielding was taken in account.

The developed system was validated by comparing the simulated En-Unipolar-PWM spectrum with real measured one using EMI time domain measurement methods.

An integrated protection unit was devolved for fast switching off the device in case of breakdown as well as current surge.

The En-Unipolar-PWM is modified to produce high frequency and high power sinusoidal signal (HF-Unipolar-PWM) for shunt impedance measurements and other applications where such a signal is required.

The device controlled by a computer and has the following features :

- Produce High quality ($THD < 0.5\%$) one phase controllable amplitude sinusoidal signal with different selectable frequencies (16,7 Hz, 50 Hz, 60 Hz) as well as the ability of signal preconditioning for HV tests (where a step up transformer is used).

- Fast switching off the applied voltage in case of voltage Breakdown (within roughly 50 μ s).
- Generate harmonics (3rd and 5th) of fundamental selected frequency with ability of controlling the harmonics amplitude and phase shift. Signal distortion in this case ($< 1\%$) from the intended one.
- Perform the PD measurements with/without harmonics and background noise is reduced to be roughly 1 pC.
- The device power efficiency is relatively high, power losses in switching elements (IGBTs) are 1.6% from the input power.
- The Pec-HV is able to produce high frequency and high power sinusoidal signal up to 2 kHz and 1.32 kW receptively.

5.2 Future work

- Use of Field Programmable Gate Array (FPGA) to be able to produce higher frequencies.
- The signal preconditioning can be developed to be performed in an automatic way. As a suggestion that can be achieved by applying the Evolutionary Algorithm EA, where the EA will perform a set of intended harmonics parameters (amplitude and phase shift) and comparing the results each time until achieving the optimal harmonics compensations.
- The idea of signal preconditioning or the undesired harmonic compensation opens the door for various new application fields where the compensation of harmonics is required, that is due to its simplicity and the low cost.

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