# Photodiodes and Image Sensors on Mechanically Flexible Ultra-Thin Silicon Chips-in-Foil

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# Preamble

This work was composed during my employment as a scientist at the chair Electronic Devices and Circuits (EBS) of the University of Duisburg-Essen. The presented results form part of the investigations conducted within the scope of the FLEXBild research project, which was founded by the German Research Foundation (DFG) for four consecutive years. The project has been successfully completed in collaboration with the Institute of Materials in Electrical Engineering, Chair 1 (IWE 1) of the RWTH Aachen University.

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# Zusammenfassung

CMOS-Bildsensoren haben in den letzten zwei Jahrzehnten enorme technologische Fortschritte erfahren und sich als eine wettbewerbsfähige Alternative gegenüber CCD-Bildsensoren auf dem Markt etabliert. Reduziert man die Chipdicke von CMOS-Bildsensoren von normal 725 µm auf $\leq$ 30 µm, erhält man mechanisch flexible Bildaufnehmer. Gewölbte CMOS-Bildsensoren würden für die optische Wahrnehmung völlig neue Möglichkeiten eröffnen (wie z. B. bei Insektenaugen). Betrachtet man die auf dem Chip integrierten Bauelemente und Schaltungen unter mechanischen Spannungen, stellt man fest, dass ihre elektrischen und optoelektronischen Eigenschaften von der ausgeübten mechanischen Spannung beeinflusst werden. Für den technischen Einsatz ist eine vom mechanischen Zustand des Bildsensors unbeeinflusste Funktion erforderlich. Der Einfluss von mechanischer Spannung auf die Bauelemente- und Schaltungs-Charakteristiken und seine Minimierung bzw. Kompensation sind daher von besonderem Interesse.

In dieser Arbeit wurden die optischen und elektrischen Eigenschaften von passiven und aktiven Bauelementen, sowie integrierten Schaltungen auf monokristallinen gedünnten flexiblen Siliziumchips unter mechanischen Spannungen untersucht. Der Einfluss von mechanischen Spannungen auf optische Eigenschaften (spektrale Lichtempfindlichkeit, Dunkelstrom und elektronisches Rauschen) einzelner p-n-Übergang-basierter Photodioden und Bildsensorarrays auf (100)-Siliziumwafern wurde theoretisch modelliert und experimentell charakterisiert. Weiterhin wurden die elektrischen Eigenschaften (Ladungsträgerbeweglichkeit, Schwellenspannung, 1/f Rauschen) von MOS-Feldeffekttransistoren in Bezug auf mechanischen Spannungen charakterisiert und ihre Abhängigkeit von der Orientierung zur Kristallorientierung des Substrats untersucht. Integrierte Schaltungen, wie Bandgap-Referenzspannungsquellen, Operationsverstärker und SC-basierte Schaltungen wurden unter mechanischen Spannungen theoretisch betrachtet, entworfen, gefertigt und experimentell charakterisiert.

Mit Hilfe des in dieser Arbeit vorgeschlagenen und eingesetzten Simulationskonzeptes, ist die Schaltungssimulation der obengenannten Abhängigkeiten möglich. Dadurch hat der Schaltungsentwickler die Möglichkeit Schaltungskonzepte zur Kompensation oder Minimierung der von der mechanischen Spannung hervorgerufenen Einflüsse zu simulieren. In dieser Hinsicht werden Schaltungskonzepte und Design-Regeln präsentiert, die den Einfluss von mechanischen Spannungen auf Bildsensorchips berücksichtigen und minimieren.

Im Rahmen dieser Arbeit wurde darüber hinaus ein mechanisch flexibler Bildsensorchip entworfen, simuliert und gefertigt, dessen Betrieb unabhängig von der ausgeübten mechanischen Spannung ist. Der ultra-dünne 20 µm Bildsensorchip ist geeignet auf zylindrisch gewölbte Oberflächen aufgebracht zu werden und erlaubt die Aufnahme raumrichtungsselektiver optischer Informationen im Sinne eines Panoramablicks.

# Abstract

CMOS image sensors (CIS) have experienced the last two decades tremendous technological advances rendering them a viable alternative to charged couple devices (CCDs) not only in high volume applications but also in applications which require high spatial and temporal resolution, high dynamic range, low noise or high sensitivity levels. CISs are employed due to their increased chip thickness (ca. 750 µm) solely in the traditional planar image acquisition. If the chip thickness could be reduced down to or less than 30 µm, the silicon chips would become mechanically flexible. Such flexible CISs could substantially extend the application spectrum of image sensors in non-conventional imaging systems (e.g. imitating insect vision). However, the on-chip integrated devices and circuits exhibit stress-induced changes on their electrical and optoelectronic characteristics. Since a stress independent operation is striven, the minimization or compensation of the influence of mechanical stress on the characteristics of devices and circuits is of great interest.

In this work optical and electrical properties of passive and active devices as well as integrated circuits on ultra-thin monolithic flexible silicon chips have been investigated under the application of mechanical stress. The influence of mechanical stress on the optical characteristics (spectral sensitivity, dark current and electronic noise) of p-n junction based photodiodes and image sensor chips on (100)-silicon wafers have been theoretically modeled and experimentally characterized. Moreover, the electrical characteristics (carrier mobility, threshold voltage and 1/f noise) of mechanically strained MOS field-effect transistors and their dependence on the channel orientation on the substrate have been investigated. Integrated circuits such as bandgap reference voltage sources, operational amplifiers and switched capacitor (SC) based circuits have been theoretically treated, designed, fabricated and experimentally characterized.

Within this framework a simulation technique has been proposed and deployed, which allows the simulation of the above mentioned stress dependence on device and circuit level. The analog circuit designer can employ the simulation technique toward the proposal of circuit topologies or techniques, which minimize or compensate the strain-induced changes on the circuit operation. In this direction, circuit concepts and design rules are proposed, which minimize the influence of mechanical stress on flexible CIS chips.

Within the scope of this work, a mechanically flexible CMOS image sensor chip has been designed, simulated and fabricated, which operation is stress independent. The developed ultra-thin 20 µm CIS chip can be wrapped around a cylindrically curved surface and thus record panoramic optical information.

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# List of Abbreviations

| | |
|---|---|
| 3D | three dimensional |
| | |
| a-Si | amorphous silicon |
| A/D | analog-digital |
| ADC | analog-to-digital converter |
| ADC | analog-to-digital conversion |
| APS | active pixel sensor |
| | |
| bcc | body-centered cubic |
| BGR | bandgap reference |
| BJT | bipolar junction transistor |
| | |
| CCD | charge coupled device |
| CDS | correlated double sampling |
| CG | conversion gain |
| CIS | CMOS image sensor |
| CMOS | complementary metal-oxide-semiconductor |
| CMP | chemical mechanical polishing |
| CV | capacitance-voltage |
| | |
| DbyT | dicing by thinning |
| DDS | delta-difference sampling or double-delta sampling |
| DIBL | drain-induced barrier lowering |

| | |
|---|---|
| DOS | density of states |
| dpi | dots-per-inch |
| DRIE | deep reactive-ion etching |
| | |
| ehp | electron-hole pair |
| | |
| fcc | face-centered cubic |
| FD | floating diffusion |
| FEM | finite element method |
| FET | field-effect transistor |
| FF | fill factor |
| FOV | field-of-view |
| FPA | focal plane array |
| FPGA | field programmable gate array |
| FPN | fixed pattern noise |
| FR4 | glass reinforced epoxy laminate |
| | |
| GBW | gain-bandwidth product |
| GUI | graphical user interface |
| | |
| HH | heavy hole |
| | |
| IC | integrated circuit |
| IR | infrared |
| ITRS | International Technology Roadmap for Semiconductors |
| | |
| LH | light hole |
| LOS | line-of-sight |
| | |
| MEMS | micro-electro-mechanical systems |
| MIM | metal-insulator-metal |
| MMIC | monolithic microwave integrated circuits |
| MOS | metal-oxide-semiconductor |
| MOSFET | metal-oxide-semiconductor field-effect transistor |

| | |
|---|---|
| OPV | organic photovoltaic |
| OWC | optical wireless communication |
| | |
| PCB | printed circuit board |
| PDMS | poly-dimethyl-siloxane |
| PGA | programmable gain amplifier |
| PI | polyimide |
| PIP | polysilicon-insulator-polysilicon |
| PPD | pinned photodiode |
| PPS | passive pixel sensor |
| PSD | power spectral density |
| PVC | poly-vinyl-chloride |
| | |
| R2R | roll-to-roll |
| RFID | radio frequency identification |
| ROI | region-of-interest |
| RTS | random telegraph signal |
| | |
| S/H | sample and hold |
| SAR | successive approximation register |
| SC | switched-capacitor |
| SCR | space-charge region |
| SF | source follower |
| Si | silicon |
| SiGe | silicon-germanium |
| SNR | signal to noise ratio |
| SoC | system-on-chip |
| SOI | silicon-on-insulator |
| SPI | serial peripheral interface bus |
| | |
| TCP | temperature coefficient of piezoresistance |
| TFT | thin film transistor |
| TG | transfer gate |

# List of Symbols

## Greek Letters

| Symbol | Unit | Description |
|---|---|---|
| $\alpha_{PD}$ | [-] | Coefficient incorporating all strain-induced changes on the photodiode characteristics sort |
| $\alpha$ | [-] | Frequency exponent in the unified 1/f noise model |
| $\alpha$ | [m] | Length of the edge of an fcc lattice |
| $\gamma$ | [$\sqrt{\mathrm{V}}$] | Body-effect coefficient of a MOSFET |
| $\gamma_{1/f}$ | [-] | Attenuation coefficient of the electron wave function |
| $\Delta$ | [eV] | Band separation between the two lowest conduction bands at the conduction band edge |
| $\bar{\bar{\varepsilon}}$ | [-] | Strain tensor |
| $\epsilon$ | [F/m] | Permittivity of a material |
| $\epsilon_s$ | [F/m] | Permittivity of silicon |
| $\eta$ | [-] | Dimensionless strain defined for computing the strain-induced conduction band degeneracy lifting |
| $\eta$ | [-] | Photodetector quantum efficiency |
| $\eta_{ext}$ | [-] | External quantum efficiency |
| $\eta_{int}$ | [-] | Internal quantum efficiency |
| $\lambda$ | [m] | Wavelength of impinging radiation |
| $\lambda$ | [$\mathrm{V}^{-1}$] | Channel length modulation parameter of a MOSFET |

| | | |
|---|---|---|
| $\mu$ | [H/m] | Permeability of a material |
| $\mu$ | [$m^2$/(Vs)] | Carrier mobility |
| $\mu_p$ | [$m^2$/(Vs)] | Hole mobility |
| $\Xi_d^i$ | [eV] | Dilatation deformation potential constant of valley $i$ |
| $\Xi_{ij}$ | [eV] | Elements of the deformation potential tensor |
| $\Xi_u^i$ | [eV] | Uniaxial deformation potential constant of valley $i$ |
| $\Xi_{u,sh}$ | [eV] | Shear deformation potential constant |
| $\pi$ | [-] | Mathematical constant equal to the ratio of a circle circumference to its diameter |
| $\pi_{11}^{(v)}$ | [$Pa^{-1}$] | Piezoresistance coefficient of silicon in the main crystallographic coordinate system |
| $\pi_{12}^{(v)}$ | [$Pa^{-1}$] | Piezoresistance coefficient of silicon in the main crystallographic coordinate system in Voigt notation |
| $\pi_{44}^{(v)}$ | [$Pa^{-1}$] | Piezoresistance coefficient of silicon in the main crystallographic coordinate system in Voigt notation |
| $\pi_L$ | [$Pa^{-1}$] | Longitudinal piezoresistance coefficient (across the [110] crystallographic direction) |
| $\pi_l$ | [$kg \cdot Pa^{-1}$] | Piezo-coefficients of the longitudinal effective mass |
| $\pi_T$ | [$Pa^{-1}$] | Transversal piezoresistance coefficient (across the [110] crystallographic direction) |
| $\pi_t$ | [$kg \cdot Pa^{-1}$] | Piezo-coefficients of the transversal effective masses |
| $\sigma$ | [Pa] | Applied mechanical stress |
| $\sigma_n$ | [-] | Electron capture cross section or scattering cross section |
| $\sigma_p$ | [-] | Hole capture cross section or scattering cross section |
| $\tau_g$ | [s] | Carrier generation lifetime in the semiconductor volume |
| $\tau_{gn}$ | [s] | Electron generation lifetime in the semiconductor volume |

| | | |
|---|---|---|
| $\tau_{gp}$ | [s] | Hole generation lifetime in the semiconductor volume |
| $\tau_p$ | [s] | Hole lifetime |
| $\phi_1$ | [-] | Digital signal controlling the first phase of an SC-circuit |
| $\phi_2$ | [-] | Digital signal controlling the second phase of an SC-circuit |
| $\Phi$ | $[\frac{\mathrm{s}}{\mathrm{m}^2}]$ | Photon flux |
| $\phi_{rst}$ | [-] | Digital signal controlling the in-pixel reset transistor |
| $\phi_{sel}$ | [-] | Digital signal controlling the in-pixel select transistor |
| $\phi_{sht}$ | [-] | Digital signal controlling the in-pixel shutter transistor |
| $\phi_p$ | [V] | Potential measuring the position of the Fermi level $E_F$ with respect to the band edge $E_V$ of a p-type semiconductor |
| $\phi_m$ | [V] | Metal work function |
| $\phi_{ms}$ | [V] | Metal-semiconductor work function difference |
| $\phi_s$ | [V] | Semiconductor work function |
| $\chi$ | [V] | Electron affinity for a semiconductor |
| $\chi_b$ | [-] | Ratio of body- to gate-transconductance of a MOSFET |
| $\chi_i$ | [V] | Electron affinity for an insulator |
| $\psi_B$ | [V] | Bulk semiconductor Fermi level potential |
| $\psi_{bi}$ | [V] | Built-in potential |
| $\psi_{Bp}$ | [V] | Potential measuring the position of the Fermi level $E_F$ with respect to the intrinsic level $E_i$ of a p-type semiconductor |
| $\psi_S$ | [V] | Semiconductor surface potential |

## Latin Symbols

| | | |
|---|---|---|
| $A$ | [m$^2$] | Area of a p-n junction interface |
| $A$ | [m$^2$] | Area of photodetector |
| $a$ | [eV] | Deformation potential constant of the valence band edge |
| $\mathbf{a}$ | [-] | Bravais lattice basis vector |
| $\mathbf{a}^*$ | [-] | Reciprocal lattice basis vector |
| $A_{CDS}$ | [-] | Closed loop AC gain of a CDS amplifier |
| $A_{CDS,OL}$ | [-] | Open loop AC gain of a CDS amplifier |
| $A_d$ | [-] | AC differential gain of a differential amplifier |
| $A_{hor}$ | [m$^2$] | Horizontal area of a p-n junction interface |
| $\mathbf{a}_i$ | [-] | Unit vector parallel to the **k** vector of valley $i$ |
| $A_{SF}$ | [-] | In-pixel source follower small signal voltage gain |
| $b$ | [eV] | Deformation potential constant of the valence band edge |
| $\mathbf{b}$ | [-] | Bravais lattice basis vector |
| $\mathbf{b}^*$ | [-] | Reciprocal lattice basis vector |
| $\bar{\bar{C}}$ | [-] | Elastic stiffness tensor |
| $c$ | [m/s] | Speed of light |
| $\mathbf{c}$ | [-] | Bravais lattice basis vector |
| $\mathbf{c}^*$ | [-] | Reciprocal lattice basis vector |
| $C_D$ | [F/m$^2$] | Depletion region equivalent capacitance per unit area |
| $c_{ijkl}$ | [N/m$^2$] | Elastic stiffness constants |
| $C_{it}$ | [F/m$^2$] | Associated capacitance to an interface-trap charge density |
| $C_{OX}$ | [F/m$^2$] | Oxide capacitance per unit area |
| $d$ | [eV] | Deformation potential constant of the valence band edge |
| $D_{it}$ | [eV$^{-1}$m$^{-2}$] | Trap density at an interface |
| $D_n$ | [m$^2$/s] | Diffusion coefficient of electrons in p-type silicon |
| $D_p$ | [m$^2$/s] | Diffusion coefficient of holes in n-type silicon |
| $E$ | [eV] | Energy |
| $E_C$ | [eV] | Conduction band edge energy level |

| | | |
|---|---|---|
| $\Delta E_C$ | [eV] | Conduction band energy shift |
| $\Delta E^i_{C,av}$ | [eV] | Conduction band energy shift average |
| $\Delta E^i_C$ | [eV] | Energy shift of the $i^{th}$ conduction band valley |
| $E_d$ | [eV] | Direct energy bandgap of a semiconductor |
| $\Delta E_F$ | [eV] | Strain-induced energy shift of the Fermi level |
| $E_F$ | [eV] | Fermi energy level |
| $E_{F,n}$ | [eV] | Quasi Fermi energy level for electrons |
| $E_{F,p}$ | [eV] | Quasi Fermi energy level for holes |
| $E_g$ | [eV] | Indirect energy bandgap of a semiconductor |
| $E_{gen}$ | [eV] | Average generation energy |
| $E_i$ | [eV] | Intrinsic energy level |
| $E_{ph}$ | [eV] | Photon energy |
| $\Delta E_{shear}$ | [eV] | Energy shift between the conduction band valleys along the axis [001] w.r.t. the other main crystallographic axes |
| $E_{t,S}$ | [eV] | Trap energy level at the semiconductor surface |
| $E_{t,V}$ | [eV] | Trap energy level in the semiconductor volume |
| $E_V$ | [eV] | Valence band edge energy level |
| $\Delta E^i_V$ | [eV] | Valence band shift under the application of mechanical stress for the light hole or the heavy hole band |
| $f$ | [Hz] | Frequency of impinging radiation |
| $F_{1/2}$ | [-] | Fermi-Dirac integral of order 1/2 |
| $f_{-3dB}$ | [Hz] | $-3$dB corner frequency |
| $F(E)$ | [-] | Occupancy of an energy level E |
| $\Delta \mathbf{F}_n$ | [N] | System of forces on a surface |
| $\mathbf{G}$ | [-] | Reciprocal lattice set of points |
| $GBW$ | [Hz] | Gain-Bandwidth product of an amplifier |
| $g_{ds}$ | [A/V] | MOSFET drain-source output conductance |
| $g_m$ | [A/V] | MOSFET gate transconductance |
| $g_{mb}$ | [A/V] | MOSFET body (backgate) transconductance |
| $G_{op}$ | $[\frac{\mathrm{s}}{\mathrm{m}^2}]$ | Generation of electron-hole pairs due to optical energy absorption |
| $h$ | [$\mathrm{m}^2$kg/s] | Planck constant |
| $\hbar$ | [$\mathrm{m}^2$kg/s] | Reduced Planck constant |

| | | |
|---|---|---|
| $I_D$ | [A] | MOSFET drain-source current |
| $I_{dark}$ | [A] | Dark current |
| $I_{diff}$ | [A] | Diffusion current |
| $I_{ge,S}$ | [A] | Generation current at the surface of a semiconductor material |
| $I_{ge,V}$ | [A] | Generation current in the volume of a semiconductor material |
| $I_{ph}$ | [A] | Photocurrent |
| $k$ | [eVK$^{-1}$] | Boltzmann constant |
| $\boldsymbol{k}$ | [m$^{-1}$] | wavevector |
| $k_r$ | [-] | Imaginary part of the refractive index of the semiconductor material |
| $L$ | [m] | Mask channel length of a MOSFET |
| $L_n$ | [m] | Diffusion length of electrons in p-type silicon |
| $L_p$ | [m] | Diffusion length for holes |
| $m$ | [-] | Multiplier equal to the W/L ratio of two MOSFETs forming a basic current mirror |
| $m_0$ | [kg] | Electron rest mass |
| $M_C$ | [-] | Number of equivalent minima in the conduction band |
| $m^i_{C,DOS}$ | [kg] | Density of states (DOS) effective mass of silicon $i^{th}$ conduction band valley |
| $m_{hh}$ | [kg] | Effective mass of heavy hole valence band |
| $m_l$ | [kg] | Longitudinal effective mass under no mechanical stress |
| $m_{lh}$ | [kg] | Effective mass of light hole valence band |
| $m^\sigma_l$ | [kg] | Longitudinal (out-of-plane) effective mass under mechanical stress |
| $M_{rst}$ | [-] | In-pixel reset transistor |
| $M_{sel}$ | [-] | In-pixel row select transistor |
| $M_{SF}$ | [-] | In-pixel transistor in a source follower configuration |
| $m_t$ | [kg] | Transversal effective mass under no mechanical stress |

| | | |
|---|---|---|
| $m_{t,\perp}^{\sigma}$ | [kg] | Transversal (in-plane) effective mass under mechanical stress vertical to the stress direction |
| $N$ | [$m^{-2}$] | Number of carriers per unit area |
| $N_A$ | [$m^{-3}$] | Doping concentration of acceptor impurities in a semiconductor material |
| $N_C$ | [$m^{-3}$] | Effective density of states in the conduction band |
| $N_D$ | [$m^{-3}$] | Doping concentration of donor impurities in a semiconductor material |
| $N(E)$ | [-] | Density of states of an energy level E |
| $n_i$ | [$m^{-3}$] | Intrinsic carrier concentration |
| $n_t$ | [$m^{-3}eV^{-1}$] | Trap distribution over space and energy levels |
| $N_{t,S}$ | [$m^{-2}$] | Trap density at the semiconductor surface |
| $N_{t,V}$ | [$m^{-3}$] | Trap density in the semiconductor volume |
| $N_V^{hh}$ | [$m^{-3}$] | Effective density of states in the heavy hole valence band |
| $N_V^{lh}$ | [$m^{-3}$] | Effective density of states in the light hole valence band |
| $P_{opt}$ | [W] | Radiant flux |
| $P$ | [m] | Perimeter of the space charge region of a p-n junction at the surface of a semiconductor |
| $p_{no}$ | [$m^{-3}$] | Hole density at thermal equilibrium |
| $Q_{depl}$ | [$C/m^2$] | Depletion charge density in the bulk semiconductor |
| $Q_{impl}$ | [$C/m^2$] | Charge density in the channel region of a MOSFET due to implantation of dopants |
| $\mathbf{R}$ | [-] | Bravais lattice set of points |
| $R$ | [-] | Coefficient of reflection |
| $R_{SD}$ | [$\Omega$] | Parasitic source-drain resistance of a MOSFET |
| $S$ | [A/V] | Substhreshold slope of the MOSFET drain-source current plotted against the applied gate voltage |
| $\bar{\bar{S}}$ | [-] | Elastic compliance tensor |
| $S$ | [-] | Scattering coefficient in the unified 1/f noise model |
| $S$ | [V/s] | Slope of a pixel circuit response |
| $S$ | [A/W] | Sensitivity of a photodiode |

| | | |
|---|---|---|
| $s_{11}^{(v)}$ | $[(N/m^2)^{-1}]$ | Elastic compliance coefficient of silicon in the main crystallographic coordinate system in Voigt notation |
| $s_{12}^{(v)}$ | $[(N/m^2)^{-1}]$ | Elastic compliance coefficient of silicon in the main crystallographic coordinate system in Voigt notation |
| $s_{44}^{(v)}$ | $[(N/m^2)^{-1}]$ | Elastic compliance coefficient of silicon in the main crystallographic coordinate system in Voigt notation |
| $s_g$ | [m/s] | Carrier generation velocity at the semiconductor surface |
| $S_{ID}$ | $[A^2/Hz]$ | Drain current noise power spectral density |
| $S_{I_D,1/f}$ | $[A^2/Hz]$ | MOSFET $1/f$ low frequency noise |
| $S_{I_D,th}$ | $[A^2/Hz]$ | MOSFET channel thermal noise |
| $s_{ijkl}$ | $[(N/m^2)^{-1}]$ | Elastic compliance constants |
| $s_{gn}$ | [m/s] | Electron generation velocity at the semiconductor surface |
| $s_{gp}$ | [m/s] | Hole generation velocity at the semiconductor surface |
| $T$ | [K] | Temperature |
| $\bar{\bar{T}}$ | [-] | Stress tensor |
| $t_{OX}$ | [m] | Thickness of gate oxide of a MOSFET |
| $u_x$ | [m] | Displacement component in x-direction |
| $u_y$ | [m] | Displacement component in y-direction |
| $u_z$ | [m] | Displacement component in z-direction |
| $U_S$ | $[m^{-2}s^{-1}]$ | Generation rate at the semiconductor surface |
| $U_V$ | $[m^{-3}s^{-1}]$ | Generation rate in the semiconductor volume |
| $V_A$ | [V] | Early voltage of a MOSFET |
| $V_{BS}$ | [V] | Substrate (bulk)-source potential difference |
| $V_{DD}$ | [V] | Power supply voltage |
| $V_{DS,sat}$ | [V] | Saturation drain-source voltage of a MOSFET |
| $V_{FB}$ | [V] | Flat band voltage |
| $V_{FD}$ | [V] | Voltage at a floating diffusion FD |
| $V_{in}$ | [V] | Input voltage |
| $V_{ov}$ | [V] | Gate overdrive |

| | | |
|---|---|---|
| $V_{PD}$ | [V] | Voltage at the terminals of a photodiode PD |
| $V_R$ | [V] | Applied positive reverse voltage at a p-n junction |
| $V_T$ | [V] | Threshold voltage of a MOSFET |
| $v_{th}$ | [m/s] | Thermal velocity of generated carriers |
| $W$ | [m] | Mask channel width of a MOSFET |
| $W_D$ | [m] | Width of the depletion region of a pn junction |
| $W_{n,hor}$ | [m] | Width of the horizontal depletion region or SCR in the n-region of a pn junction |
| $W_{n,ver}$ | [m] | Width of the vertical depletion region or SCR in the n-region of a pn junction |
| $W_{p,hor}$ | [m] | Width of the horizontal depletion region or SCR in the p-region of a pn junction |
| $W_{p,ver}$ | [m] | Width of the vertical depletion region or SCR in the p-region of a pn junction |

# Chapter 1 - Introduction

The advancement of semiconductor technology and microelectronics has spanned the past sixty years ranging from the first successful fabrication of an integrated circuit (IC) in 1958 conceived by Jack Kilby to the integration of billions of transistors with a minimum gate length of 14 nm on a single chip in 2013. Integrated circuits find themselves in various applications such as laptop computers, cellphones, medical products, digital cameras and integrated sensors.

Monocrystalline silicon (Si) is nowadays the main material used as a substrate for the fabrication of ICs in the most complementary metal-oxide-semiconductor (CMOS) manufacturing technologies available worldwide. Lately organic semiconductors technology has gained an increasing attention in the electronic industry and is expected to be an enabling technology platform for new electronic applications and markets [MSvVH12][BAH+09]. One of them, namely the flexible electronic industry, has been revolutionized through the advances in organic semiconductors mostly through the rapid technological progress in flexible displays during the past decade. Flexible electronic products fabricated either on silicon or on organic semiconductors range from foldable displays [WS09], conformable sensors and micro-systems [SKS+05], medical implants [SHH+99] to electronic paper [RBB+01]. Flexible electronics based on organic semiconductors though can compete with silicon either in the very low priced segment by using high throughput roll-to-roll printing manufacturing technology [BAH+09] or in applications where switching speeds are not crucial, such as flexible displays. However, many applications which would benefit from a mechanically flexible substrate require parallel superior switching speeds such as high quality image sensors, medical implants, smart cards or monolithic microwave integrated circuits (MMIC).

Ultra-thin silicon chips technology opens the pathway not only to the further miniaturization of ICs by enabling their three-dimensional stacked integration but also to their mechanical flexibility due to silicon inherently excellent mechanical properties. Moreover, ultra-thin silicon chips can be combined with bendable sensors, batteries and/or organic electronics and can be encapsulated on a common flexible polymeric substrate, facilitating the emerging new class of flexible electronic products called chips-in-foil or systems-in-foil [vdBdBvMD08][DvdBV+11]. Mechanical flexibility of ultra-thin chips is exploited to support either or both mechanical reliability or bendability of the product. For instance, biomedical sub-retinal implants should be extremely thin so that they can adapt to the shape of the retina [BAH+09]. Another interesting application which requires both bendability as well as a substrate featuring high carrier mobilities is a mechanically flexible high temporal resolution CMOS image sensor.

CMOS image sensors (CISs) have experienced the last two decades tremendous technological advances rendering them a viable alternative to charge coupled device (CCD) not only in high volume applications but also in applications which require high spatial resolution, high dynamic range, low noise or high sensitivity levels. Moreover, CISs offer the ability to integrate sensing with analog and digital processing down to the pixel level, which in turn has enabled a plethora of new imaging applications for the consumer, commercial, and industrial markets [EGE05]. CMOS image sensors for such specific purposes are called smart CMOS image sensors and can incorporate next to the traditional correlated double sampling (CDS) and analog-to-digital conversion (ADC) functions like feature extraction, pattern recognition, target tracking and on-chip image processing.

## 1.1 Motivation

Traditional silicon ICs are being manufactured on wafers up to a millimeter thick, in order to be mechanically stable and rigid enough so as to survive the CMOS fabrication process. There are many applications though, where the silicon substrate thickness is reduced down to 100 µm. Silicon wafers are still rigid, but they must be handled very carefully. Between 50 and 100 µm, a wafer may fracture under its own weight [Bur13]. Below the 50 µmlimit silicon wafers become again mechanically stable and flexible. Reducing the thickness below 10 µm, the wafer becomes even optically transparent [Bur13]. Such ultra-thin silicon chips are able to bend, twist and roll up, while being mechanically stable and still made of high-performance crystalline silicon [Bur13]. Therefore, ultra-thin silicon chips are a promising if not the only one platform for the creation of bendable electronic systems with high performance, since flexible organic semiconductors are very slow to substitute silicon in applications like consumer and biomedical devices, due to their decreased carrier mobility. Future flexible electronic systems would benefit from the combination of high-performance ultra-thin silicon chips with low cost organic electronics. Ultra-thin Si chips with thicknesses less than 20 µm are being employed towards this direction, i.e., for realizing bendable, foldable and in general flexible systems such as retinal implants [GHE+09], radio frequency identification (RFID) tags embedded in paper [MSM+12], mechanical stress and pressure sensors [HMG11], high-density brain activity systems [VKV+11] and electronic skin [KLM+11].

Looking back at nature we can clearly see that most of the living organisms possess curved photoreceptors in order to turn the light information of their environment into a neural signal, which will provide them important feedback for navigating and orientating themselves or recognizing preys or predators. However, although nature was and is always inspiring engineers, most of today's electronic imaging systems such as CCDs or CISs are not conformable due to their fabrication on solid, rigid silicon wafers. Therefore, their use is limited in the conventional optical systems based on a planar image surface and utilizing therefore expensive and complex optics. However, flexible CISs that would conform on an arbitrary cylindrical or hemispherical surface would extend the application spectrum of image sensors and open up new vistas of the image sensor market. For instance, a bendable CIS could be wrapped around a cylindrical rod and collect light information from a 360° panoramic field-of-view (FOV). In addition to that, bendable image sensors offer many advantages when compared with their planar counterparts. Curved focal plane arrays (FPAs) could enable not only the study of nature (i.e., locomotion of invertebrates using low resolution compound eyes) but also provide a way to lower the number of optical elements used in a traditional optical system, to reduce aberrations including astigmatism and coma, and to increase off-axis brightness and sharpness [RCD+08]. Therefore, bendable CMOS image sensors have drawn the attention of the research community in the last ten years and constitute also part of this work investigations.

Ultra-thin Si chip manufacturing technology combined with a mechanically flexible encapsulation to provide both handling support as well as electrical connectivity could be exploited towards the development of a flexible CIS. However, remaining compatible with standard commercially available CMOS fabrication processes is challenging and would be beneficial for a wide spectrum of applications which require low cost and high quality manufacturing. Not only existing imaging applications would benefit from such development, but also new and exciting application fields would arise, such as panoramic biofluorescence imaging, where a biological sample is wrapped around a flexible image sensor, monolithic electronic compound eyes for robotic vision, wireless optical communications utilizing a 360° optical communications hub or endoscopic cameras and capsules with a panoramic FOV.

However, whenever mechanical stress is exerted onto a silicon chip, the crystal structure of the semiconductor substrate is being altered and its crystal symmetry may be reduced. Macroscopically this is leading to shifts in the electrical and optical characteristics of the integrated devices, such as input and output characteristics of

metal-oxide-semiconductor field-effect transistors (MOSFETs), capacitance and dark current of a p-n junction based photodiode or resistance values of integrated resistors. These effects known as piezoresistance or piezojunction effects and their influence on the behavior of analog circuits and systems (i.e., CMOS image sensors) have not been profoundly investigated. This information is though very important for the design of a bendable image sensor on a monolithic semiconductor substrate, which operation should be mechanical stress independent. The analog IC designer has to gain insight on how the effects emerging from the application of mechanical stress influence the operation of the designed circuit. Additionally, it would be advantageous to offer the designer a simulation technique of these influences. Thereby the circuit dependence on a defined mechanical stress level is precisely quantified and in parallel the IC designer is assisted in the definition of potential compensation measures against negative strain-induced effects.

## 1.2 Research Goal and Scientific Approach

The main goal of this work is to systematically analyze the influences induced by uniaxial mechanical stress on the optical and electrical characteristics of integrated p-n junction based photodiodes and integrated analog circuits employed towards the design of a flexible CIS on monolithic ultra-thin Si chips-in-foil. A further objective of this thesis is the proposal of design rules and circuit concepts, which take the influences caused by mechanical stress into account and act towards their minimization or compensation. Thereby, it is aimed at designing and fabricating analog integrated circuits, which are minimally stress dependent (unless they are operated as stress sensors), achieving thus a uniform operation under any stressed state. CMOS image sensors hold also a very important position within this work. The influence of uniaxial mechanical stress on the signal path of a readout chain of a CIS should be examined. Furthermore, a simulation technique of the effects induced by the application of mechanical stress on the integrated devices should be presented and introduced in the IC simulator. In order to demonstrate the results of this dissertation on a systems level, the design, layout and fabrication of a bendable monolithically integrated CMOS image sensor which operates stress independently is striven.

The scientific approach of this work is illustrated in figure 1.1, where it is divided into three main categories: Simulation, modeling and experiments. These were per-

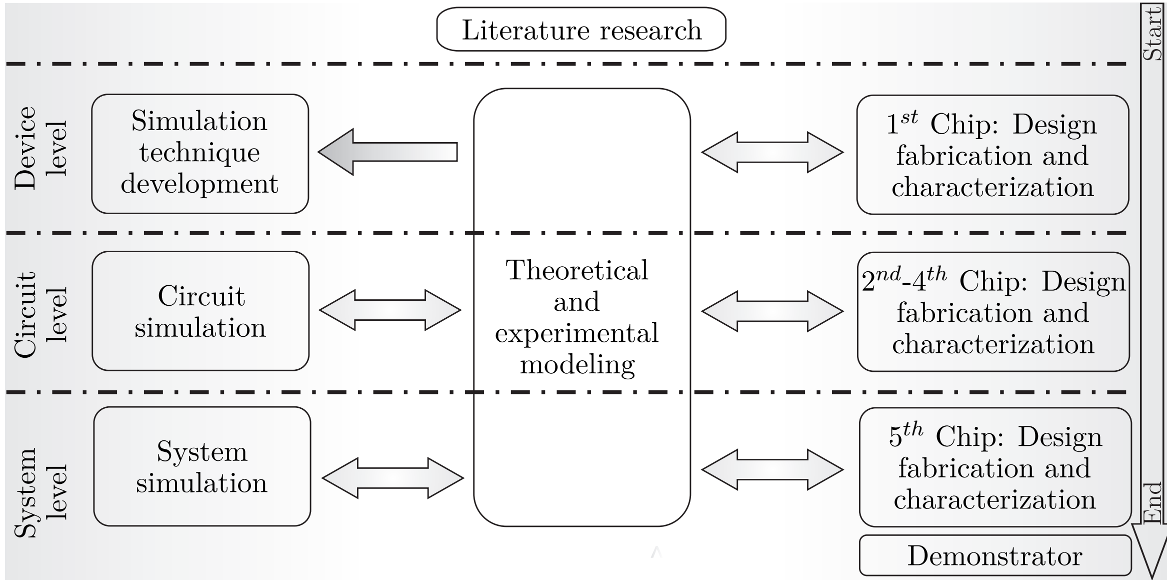


***Figure 1.1: Scientific approach.*** *The steps undertaken and the chips fabricated for the completion of this work are shown here. Simulation, modeling and experiments were performed and compared in three abstraction levels.*

formed on three different abstraction levels, namely on the device, circuit and system level. Starting from the device level modeling and characterization provides a solid background for the development of the needed simulation technique. Subsequently, not only circuits but entire systems can be simulated under a defined mechanical stress level. Thereby, design concepts minimizing the circuit dependence on the applied mechanical stress can be simulated on the computer. By means of these simulation data as well as the theoretical modeling results the next ICs are designed. Following, these ICs are experimentally characterized and the obtained data are compared with the theory. The last step is the design and fabrication of a flexible CIS, which will serve as a demonstrator of this work results.

## 1.3 State of the Art

The state of the art is presented in this section with respect to three main categories: Integrated devices under mechanical stress, flexible sensors either on monocrystalline ultra-thin silicon substrates or organic substrates and compound electronic eyes.

**Integrated devices and circuits under mechanical stress**

Piezoresistivity in semiconductor materials like silicon and germanium and its effect on the electronic band structure was initially observed by Smith in 1954 [Smi54]. Mechanical strain influences not only the properties of passive integrated devices such as resistors [SJ01], but also alters the input and output characteristics of active devices such as MOS transistors [DM69] [HFST91] and bipolar junction transistors (BJTs) [FM00]. Furthermore, the piezojunction effect discovered in 1951 by Hall, Bardeen and Pearson [HBP51] was investigated mainly during 1960s. Forward biased p-n junctions were experimentally examined under the application of mechanical stresses typically higher than 1 GPa [WHB64] [Kan67] [MW73]. The existing models of these investigations are only valid for very high compressive stresses in the range of 1-10 GPa, which rarely appear in the applications of circuits and sensors [Fru01]. Recently, a piezojunction model of the saturation current of forward biased BJT transistors was proposed in [CF02] and [CF04].

Although mechanical strain on certain crystal orientations leads to a significant improvement of the electrical characteristics of the stressed devices, its positive effects mainly on the carrier mobilities have not been exploited towards the enhancement of the electronic properties of MOS transistors until the 1980s, where experiments with Si layers grown on relaxed silicon-germanium (SiGe) substrates were conducted by [MGJ82] and [PBL+84]. The thin Si layer takes the larger lattice constant of the SiGe substrate and creates biaxial tensile stress on the entire silicon substrate [TSCN06]. Apart from this global substrate-induced stress technique, the application of externally applied mechanical stress on wafer level has also been extensively studied [BJSO01]. Moreover, the last twenty years locally process-induced strain has been investigated in order to introduce stress directly into the channel of MOS transistors. This was performed either via deposition over the MOSFETs of so-called high stress capping layers [LTF04] [SHO+01] or by a SiGe doping in the drain and source regions of the MOSFETs [RTL+02] [GPO00]. Process-induced uniaxial strain was one of the technologies projected by the International Technology Roadmap for Semiconductors (ITRS) [ITR04] to be enabling higher saturation current drive values needed in the next generation digital CMOS fabrication processes. Strained-Si MOSFETs have been adopted the last years in the mass production of sub-100 nm digital CMOS technologies [TSCN06] [TAA+04a] [TAA+04b] [BAB+04]. Hereby, uniaxial tensile strain is introduced into the n-type MOSFET, while uniaxial compressive strain into its p-type counterpart. These particular strains increase not only the respective carrier mobilities in the channel of

the transistors (and thus the saturation drain-source current) but also reduce the gate leakage currents [TSCN06].

However, in the case of externally applied global stress as it is for ultra-thin silicon chips under bending, mechanical strain can alter negatively the electrical properties of integrated devices, since all devices are subject to the same stress direction. Such stress-induced shifts in the integrated devices characteristics might not be detrimental for digital circuits, due to their high signal swing but are vital for analog circuits, which are extremely sensitive to shifts of devices operating point. In [AKM+07] several circuits were fabricated on single-crystalline silicon ribbons on a plastic substrate and shifts up to 20 % of a ring oscillator output frequency were observed under bending. However, the reasons leading to such behavior were not presented. Integrated bandgap voltage references and their dependence on mechanical stress were examined in [Fru01] and techniques for improving their accuracy were put forward. In [JRS95] the effects of stress-induced mismatches on fundamental analog circuits were shortly presented and simulated, while in [JSR+00] a theoretical analysis of these influences was given.

**Flexible sensors and their fabrication**

Flexible electronic systems have been developed either on organic or silicon-based substrates. Starting from the former, organic semiconductors possess a high potential in the market regarding their flexibility and stretchability. Moreover, organic polymers can be produced at low-cost, can possess a large area and be lightweight. The existing manufacturing techniques can be fully automated and can be used for a large scale electronics production. The most important representatives are roll-to-roll (R2R) manufacturing [HCYX11], screen printing [TdGS04], ink-jet printing [XL11] and spray coating [GMR+10], [MMM+05]. Organic photodiodes can be deployed either towards solar cell manufacturing or image sensing applications. In [KWS+12] less than 2 µm thick polymer-based photovoltaic solar cells were presented. These ultra-thin organic photovoltaic (OPV) devices exhibit a 4.2 % power conversion efficiency and can reversibly attain mechanical strains of more than 300 %. In [NWC+08] a 4 µm thick image sensor incorporating organic bulk heterojunction photodiodes with low dark current and efficient charge collection is reported. The mechanically flexible sensor backplane was fabricated at on a plastic substrate using inkjet-printed masks and the sensor consisted of 180 × 180 pixels with 75 dots-per-inch (dpi), incorporating amorphous silicon (a-Si) thin film transistors (TFTs). In [SHMS05] a proposed 16 pixel line sensor consists of a flexible micro-lens array and organic field-effect phototransistors on a flexible polyimide (PI) substrate. This device was operated as a

flexible thin line sensor zooming in and out by changing its curvature [SHMS05]. A large-area, flexible, and lightweight sheet image scanner on a plastic film by integrating high-quality organic transistors and organic photodetectors was fabricated in [SIK+04]. The 400 µm thick scanner incorporates 5184 sensor cells with a 36 dpi resolution and utilizes thin-film transistors with 18 µm channel lengths and electron mobilities of 0.7 $cm^2/(Vs)$. In [KB13] the authors present a novel bendable image sensor that is based on a luminescent concentrator film which absorbs light from a specific portion of the spectrum and re-emitts it at a lower frequency. A thin-film luminescent concentrator is a flexible, fully transparent, scalable, and low-cost polymer film. The sensor exhibits a dynamic range of 10 bits and a signal to noise ratio (SNR) of 20 dB. Another bendable image sensor on organic substrate has been presented in [SWL09b]. The sensor was first fabricated on a flat flexible plastic surface and then shaped to a good approximation of a hemispherical dome, using a cut and bend approach, following the design principles of a geodesic dome. The utilized a-Si photodiodes show an increased dark current of 1 $nA/mm^2$ [SWL09a] and the incorporated TFTs exhibit a mobility of 0.5-1 $cm^2/(Vs)$. Organic flexible image sensors were announced to become a mass product within 2014 [Jam13] [Log13], targeting low cost and low performance applications mainly in the industrial and consumer markets. Potential applications include smart packaging and sensors for medical equipment and biomedical diagnostics, user identification by fingerprint scanning, environmental scanning surfaces and three dimensional (3D) interactive user interfaces for consumer electronics.

The drawback of organic image sensors, as the presented values elucidate, is the slow operating frequency due to the low-carrier mobility in organic transistors, low resolution and low dynamic range [WS09]. Therefore, for high-performance applications image sensors need to be fabricated on inorganic semiconductors. However, combining an organic photoconductive layer over a thick CMOS chip has also been demonstrated [BPS+12] [IHM+07]. This technology is very promising for compensating the loss of sensitivity in modern silicon CMOS image sensors due to the constant pixel-size shrinking. In [BPS+12] was demonstrated that the light sensitivity of present CISs can be increased up to 100 % by replacing silicon photodiodes with an organic photoactive layer deposited with a simple low-cost spray-coating process. The demonstrated ICs of this work are not thin enough to be bendable. Although combining this technology with the ultra-thin chip manufacturing processes stated before can lead to high performance, high sensitivity, small pixel-size and flexible CISs.

For silicon based flexible electronic systems, the thickness of the chip fabricated on

traditional wafers has to be reduced in order to gain flexibility or ultra-thin silicon chips have to be fabricated from the ground up. There are many different processes to reduce the initial 725-775 µm thickness of a wafer.

Traditional wafer thinning is mainly performed using chemical mechanical grinding, polishing and lapping, a procedure often called chemical mechanical polishing (CMP). Here, the backside of a wafer is removed by mechanical or chemical means and the thinned wafer is sawed using standard sawing techniques. However, due to the mechanical processing, micro-cracks arise at the sawing lines influencing the mechanical stability of the ultra-thin chips. Thus, utilizing the technique proposed in [LKSA01] the influence of micro-cracks induced by sawing are eliminated. The technique called dicing by thinning (DbyT) utilizes deep trenches in the wafer front side, which have been prepared on the rigid wafer directly after the CMOS fabrication process (post-processing). The trench depth defines the projected final wafer/chip thickness. The trenched wafer goes then through the CMP process, until the trenches are reached and opened from the backside, enabling a self-acting die separation [LKSA01].

In [DRH+08] a way to thin and curve silicon dies for nonplanar focal plane array applications was successfully demonstrated. Dummy chips without any functional ICs were fabricated and thinned down to 30 µm. This approach utilizes a post-foundry deep reactive-ion etching (DRIE) process to microstructure of a monolithic silicon die or wafer in small silicon islands. The islands are interconnected through ultra-thin silicon wires acting as silicon springs. The elastic deformation of the silicon springs allows for sufficient deformation of the silicon membrane to conform to a hemispherical shape [DRH+08]. This approach can be performed either on silicon-on-insulator (SOI) wafers or on bulk wafers with a (111) crystal orientation (traditional CMOS processes utilize (100) Si bulk wafers). Devices and circuits are supposed to be integrated on the silicon islands, thus reducing both fill factor and resolution of a potential CIS fabricated using this technology.

Another promising but costly technique to acquire ultra-thin chips is making use of SOI wafers as proposed in [KSS+08]. Here, the integrated circuits are fabricated on the top thin silicon layer over the silicon dioxide using traditional CMOS fabrication processes. Afterwards, the silicon dioxide layer is selectively etched away and the thin top silicon layer is detached from the substrate. Following this technique ultra-thin silicon structures with a thickness of 200 nm to 1 µm can be realized and transferred on flexible PI or poly-dimethyl-siloxane (PDMS) substrates and can be bent up to a

bending radius of 5 mm [AKM+07] [AKL+06] [RSH10]. A similar technique as the one described in [LKSA01] and proposed by [MMB+06] uses trenches and selective etching to create ultra-thin flexible silicon ribbons and membranes on bulk (111)-oriented silicon wafers.

Next to the presented thinning techniques using either bulk or SOI wafers, a novel fabrication process to build ultra-thin silicon chips from scratch has been introduced in [BAH+09]. In this technique, a standard silicon bulk wafer has to be pre-processed before any device integration to develop thin silicon membranes over narrow substrate cavities utilizing implantation, etching, annealing and epitaxial growth techniques. The following step is the device integration on these thin silicon membranes using a CMOS fabrication process. To reduce the possibility of a chip warpage during fabrication, vertical anchors are placed between the membrane and the substrate of the carrier wafer. Controlled anchor fracture is performed either via externally induced or process induced mechanical stress [BAH+09]. Following the CMOS fabrication process, a post-processing module takes place, where trenches are etched around the membrane. At the end, the thin chip is detached from the carrier wafer using a pick and place technique leading to the fracture of the remaining vertical anchors.

Different fabrication techniques which first curve the silicon substrate on a spherically curved glass substrate and then deposit the imager structures via soft lithography have been presented in [JAEN04] and in [RCC+99]. To date no results of this approach are known to produce a fully functional CIS with a high fill factor [ID10].

Curved silicon based CMOS image sensors – one of the main foci of this work – have been in the epicenter of research the last ten years. In [JXM+11] a silicon imaging device is described utilizing photodetector arrays on thin elastomeric membranes, capable of reversible deformation into hemispherical shapes with radii of curvature that can be adjusted dynamically, via hydraulics. The detector consists of an array of silicon unit cells, each of which includes a thin 1.25 µm silicon photodiode. The unit cells are interconnected with serpentine shaped ribbons to form an overall system with an open mesh geometry [JXM+11] [RSH10]. Combining this type of detector with a similarly tunable, fluidic plano-convex lens yields a hemispherical camera with variable zoom and excellent imaging characteristics [JXM+11]. However, due to the distance between the islands both the resolution as well as the fill factor of the sensor are being negatively affected. A hemispherically curved monolithic silicon infrared (IR) image sensor (microbolometer) was demonstrated in [DFB+12]. The IR detector used to

realize this hemispherical IR camera is a standard $320 \times 256$ pixel array at 25 µm pitch. The infrared image sensor was then attached to a hemispherical glass holder with a radius of 70 mm, which illustrates that monolithic silicon sensors can be bent in relatively large bending radii. A hemispherically curved CCD at wafer scale has been demonstrated in [SCT+04]. In this work a 4 inch 30 µm wafer was thinned using the principle of frame thinning and was laminated on a curved glass layer with a curvature radius of 431 mm. Another hemispherically curved large area CCD was demonstrated by the Jet Propulsion Laboratory [ID10]. The wafer scale sensor was thinned and its curvature was modified on the fly by applying air pressure to the thinned membrane. Such wafer scale detectors bent on relatively high curvature radii of 250-500 mm are of high interest in astronomical telescopes [ID10]. Wafer scale curved CCDs or CMOS image sensors would simplify the telescope adjoining optics, reducing the number of optical elements and the occurrence of optical aberrations associated with large corrective optics used by flat detectors [SCT+04]. Moreover, the image quality through fewer optical elements and fewer air-glass surfaces would be optimized, while eliminating field flattening elements [ID10]. Hemispherically bent ultra-thin silicon chips were investigated in [STTS06] respective their bending and surface strength. Moreover, the authors performed a structural optimization of a curved thin image sensor using finite element method (FEM) simulations and genetic algorithms. They concluded that the optimum thickness of a $6 \times 6$ mm$^2$ chip conformed to a hemispherical surface is 51 µm at an optimum bending radius of 20 mm with respect to the lowest fracture probability (2 %).

Other applications of flexible ultra-thin silicon based electronic devices include RFID tags embedded in paper as the ones demonstrated in [MSM+12] [DDF+05]. In [DDF+05] the ICs were fabricated on SOI wafers and transferred on a PI foil. The total thickness of the RFID chip accounted 10 µm and the maximum achieved bending radius was 0.7 mm. Furthermore, ultra-thin bendable electronics conformed to the human skin have been presented in [KLM+11], which were almost invisible to the user. The active elements on these chips use established electronic materials, such as silicon and gallium arsenide, in the form of filamentary serpentine nanoribbons and micro- and nanomembranes [KLM+11] fabricated using the techniques described before. Flexible silicon chips find also applications in biomedical engineering such as the high-density electrode arrays for mapping brain activity developed in [VKV+11] or retinal implants presented in [GHE+09]. Another application where thinned silicon chips can be found is the three dimensional (3D) chip integration. 3D chip interconnection enables lower

cost, higher performance, smaller form factor and heterogeneous integration for chips manufacturing [Yu06] [RKW+10].

**Compound electronic eyes**

Compound electronic eyes mimicking the biological eyes of insects constitute another application for bendable ultra-thin CMOS image sensors. In nature compound eyes of insects show outstanding capabilities for fast panoramic motion detection, proximity estimation, for a wide FOV as well as for reducing the volume of the optical system. All these advantages come along with an inevitable reduction of the visual acuity of the eye. Furthermore, the curvature radii of biological compound eyes are relatively small in comparison with the curvature radii that hemispherically bent thinned Si-monolithic image sensors can achieve before fracturing. The largest biological compound eye is an apposition type eye and belongs to the dragonfly *Anax junius* with a curvature radius of 14.3 mm [Lan97]. Thus, due to the lack of curved monolithic image sensor arrays, electronic compound eyes can be fabricated either structuring the silicon substrate in interconnected silicon islands as presented above, or using discrete electronic components on a flexible printed circuit board (PCB) or by combining spherically curved polymer micro-lens structures with a pinhole array on top of a conventional planar CCD or CIS.

A spherical artificial compound apposition eye has been demonstrated in [RDZT07] utilizing the latter technique. The compound eye features an imaging micro-lens array which is patterned on a separate spherical bulk lens by means of a special modified laser lithography system. This process is capable of generating micro-lens structures with low shape deviation on curved surfaces [RDZT07]. Diverse techniques to fabricate three dimensional (3D) artificial compound eye micro-lens structures have been reported in literature, such as soft lithography [KTH+11], polymer reconfigurable microtemplating [JKL06], a technique utilizing hybrid sol-gel glass [ZXH+05] and a technique using femtosecond laser-enhanced wet etching, casting and thermo-mechanical processing [QCL+12].

An artificial compound eye has been recently developed on a flexible PCB within the scope of the european CurvACE project. The sensor consists of three materially and functionally different layers based on a planar fabrication technology. First an optical layer composed of an array of highly transparent polymer micro-lenses focuses light precisely onto a silicon-based planar 300 µm rigid photodetector layer. Finally, a flexible electromechanical interconnection layer, formed by a PI PCB, physically

supports the ensemble [FPCV+13]. The total thickness of the structure is 950 µm, which renders it rigid and not flexible. To obtain flexibility on the horizontal axis (for cylindrical bending), a columnwise high-precision cutting (dicing) of the rigid layers is performed until reaching the flexible interconnection layer, which remains intact [FPCV+13]. Moreover, by properly designing the micro-lens array on top of the planar photodetector array a wide FOV of $180° \times 60°$ has been achieved. The authors designed the sensor based on the characteristics of the *Drosophila melanogaster* compound eye. However, the achieved FOV is 2.6 times lower and the eye diameter more than 35 times larger in comparison to the insect eye. Achieving a similar, if not larger, FOV and a smaller eye diameter is a very challenging task. Combining a micro-lens or waveguide structure on top of the ultra-thin CMOS image sensor proposed in this work can address these issues.

## 1.4 Thesis Outline

The structure of this work involves seven chapters. Chapter 1 introduced the reader to the work, presented the motivation of this research and defined the research goal and scientific approach followed to reach it. The chapter closed with an in-depth analysis of the state of the art w.r.t. strained-Si technology and flexible electronics.

Chapter 2 puts forward the theoretical background supporting this work. The reader is introduced to the theory of elasticity and to the fundamentals of semiconductor device physics. The chapter closes with a brief summary on CMOS image sensor architectures, pixel structures and peripheral readout electronics.

Chapter 3 introduces a model describing the strain-induced effects anticipated in the fabricated devices and circuits. Deformation potential theory allows the calculation of the energy band shifts, which along with the strain-induced changes of the energy band curvatures permit the quantification of the effects on the carrier concentrations in each conduction and valence band. This model is used to describe the changes in the I-V characteristics of reversed biased p-n junction based photodiodes and MOS capacitors. Piezoresistance theory on MOSFETs is briefly presented and employed towards modeling of analog circuits under mechanical stress. Basic as well as elaborate analog circuit configurations deployed in CIS readout electronics under the application of mechanical stress are discussed and analyzed.

Chapter 4 presents the simulation technique for devices and circuits under mechanical stress. Simulation results of the proposed model for strained photodiodes in the previous chapter are shown here. A novel simple but accurate simulation technique of uniaxially strained metal-oxide-semiconductor (MOS) transistors is introduced into the circuit simulator and is employed towards the simulation of circuits and systems under stress. Simulation results of bandgap reference circuits, operational amplifiers and CIS readout electronics are presented in this chapter. Goal of these investigations is the proposal of design guidelines for stress-independent circuit operation.

Chapter 5 presents briefly the experimental methods used in this work before proceeding to the presentation of experimental results. All designed test structures featuring integrated devices, circuits and test image sensors to investigate the presented theory are introduced. The fabrication techniques for obtaining ultra-thin silicon chips appear next and the chapter closes with the presentation of the mechanical, electrical and electro-optical measurement setups used throughout the experimental part of this work.

Chapter 6 presents the experimental results obtained in this work. p-n junction based photodiodes are electrically and optically characterized under mechanical stress and the results are compared with the proposed model. Measurements of uniaxially strained MOS capacitors and MOS transistors are analyzed. Circular gate format p-type transistors are introduced as a stress-independent alternative. Bendable image test sensors are characterized under stress and the operation of a bandgap reference circuit under mechanical stress is evaluated and discussed. Based on the accomplished results, the design of a flexible image sensor for bendable applications is presented. The proposed sensor is designed to exhibit a mechanical stress independent operation, which renders it the first CMOS image sensor ever published in literature with such feature.

Chapter 7 discusses the obtained design techniques towards the minimization of the strain-induced effects on the circuit operation. Potential applications of the fabricated flexible image sensor are presented. Concluding remarks and summary of the results of this thesis are put forward.

# Chapter 2 - Theoretical Background

In the following sections the essential theoretical background supporting this work is briefly presented. First, an introduction to elasticity theory is put forward followed by the fundamentals of semiconductor physics with respect to integrated devices in a modern CMOS process. Next, a review of basic analog circuits and their application in CMOS image sensors are presented.

## 2.1 Elasticity Theory

Elasticity is a physical property of a solid material to regain its original shape after removing the applied external force, which has deformed it. Two basic types of force act on a body to deform its shape. Forces of the first type are called surface forces, since they act on the surface of the body (i.e., produced by contact with another solid) [DR78]. Forces of the second type are called body forces, since they act on each element of the body (i.e., gravitational or centrifugal force field) [DR78].

### 2.1.1 Stress

Consider an arbitrary internal or external surface, which may be plane or curvilinear in a cartesian coordinate system. Let the surface outer normal be in the positive $z$ direction. Over a small area $\Delta\mathrm{A}$ of this surface at a point P, a system of forces acts with a resultant represented by $\Delta\mathbf{F}_n$, as shown in figure 2.1. Dividing $\Delta\mathbf{F}_n$ by the increment of area $\Delta\mathrm{A}$, the average stress acting over the area is obtained. In the limit as $\Delta\mathrm{A}$ approaches zero, the resultant stress $\mathbf{T}_n$ is obtained at point P:

$$\mathbf{T}_n = \lim_{\Delta\mathrm{A}\to 0} \frac{\Delta\mathbf{F}_n}{\Delta\mathrm{A}} \tag{2.1.1}$$

Resolving the resultant stress into its components along the $x$, $y$ and $z$ axes, three cartesian stress components can be obtained for this particular surface. Repeating the same procedure using surfaces, which outer normals are in the positive $x$ and $y$ directions another six cartesian stress components can be obtained. Arranging all of

these components in a matrix, the stress tensor $\bar{\bar{T}}$ can be formed:

$$\bar{\bar{T}} = \begin{Vmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{Vmatrix} \tag{2.1.2}$$

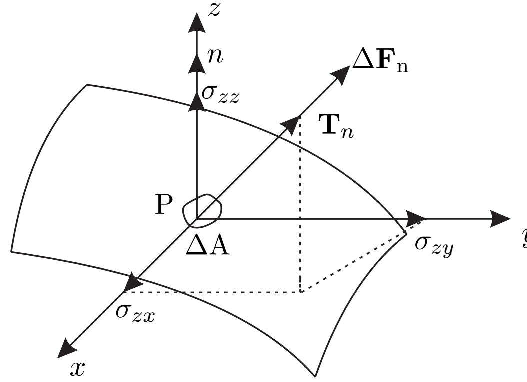


***Figure 2.1: Resultant of forces acting over area $\Delta A$.*** *The resultant stress $\mathbf{T}_n$ coincides with the line of action of the resultant force $\Delta\mathbf{F}_n$ and can be resolved in its cartesian components $\sigma_{zz}, \sigma_{zx}$ and $\sigma_{zy}$.*

A tensor is a mathematical notation, usually represented by an array, to describe a linear relation between two physical quantities [STN07]. In equation (2.1.2) the first subscript refers to the outer normal of the plane, on which the stress component acts. The second subscript gives the direction, in which the stress acts. For normal stress components positive signs indicate tension, while negative signs indicate compression [DR78].

Under the static equilibrium condition, the distribution of the stresses produced throughout a body must be such that the overall equilibrium of the body is maintained. In other words, both the summation of all forces along one direction and the summation of all momenti in one direction should amount to zero. Considering these equilibrium conditions it can be shown [DR78]:

$$\sigma_{ij} = \sigma_{ji}, \quad \text{for } i, j \in \{x, y, z\} \tag{2.1.3}$$

### 2.1.2 Strain

Consider an arbitrary body subjected to a system of forces in a cartesian coordinate system. In general individual points of the body will move. The movement of an arbitrary point is a vector quantity called displacement, which can be resolved in its cartesian components such that $u_x$, $u_y$, $u_z$ are the displacements components in the $x$, $y$, $z$ directions respectively. The movement of two arbitrary points P, Q relative to each other is known as deformation. Strain is a geometric quantity, which depends on the relative movements of two points in the body and thus is related only to the deformation displacements [DR78]. Similar to stress, strain is classified into two types: normal and shear strain. The former is defined as the change in the length of a line segment between to points divided by the original length of the line segment. The latter is defined as the angular change between two line segments which were originally perpendicular. Following the procedure described in [DR78] normal strains $\varepsilon_{ii}$ can be described by:

$$\varepsilon_{ii} = \sqrt{1 + 2\frac{\partial u_i}{\partial x_i} + \left(\frac{\partial u_x}{\partial x_i}\right)^2 + \left(\frac{\partial u_y}{\partial x_i}\right)^2 + \left(\frac{\partial u_z}{\partial x_i}\right)^2} - 1 \qquad (2.1.4)$$

where $i \in \{x, y, z\}$ and $x_i = x, y, z$.

Similarly the shear strain components can also be related to the displacements. The angle between two line segments in the deformed state can be expressed in terms of the displacement gradients, since the cosine of the angle between any two intersecting lines in space is the sum of the pairwise products of the direction cosines of the lines with respect to the same set of reference axes [DR78]. This leads to the following equation for shear strains $\varepsilon_{ij}$:

$$\varepsilon_{ij} = \frac{1}{2}\arcsin\left(\frac{\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i} + \frac{\partial u_x}{\partial x_i}\frac{\partial u_x}{\partial x_j} + \frac{\partial u_y}{\partial x_i}\frac{\partial u_y}{\partial x_j} + \frac{\partial u_z}{\partial x_i}\frac{\partial u_z}{\partial x_j}}{(1+\varepsilon_{ii})(1+\varepsilon_{jj})}\right) \qquad (2.1.5)$$

where $i \neq j \in \{x, y, z\}$.

In a wide variety of engineering problems the displacements and strains produced by the applied forces are very small and thus the displacement gradients are small as

well. Therefore, it can be assumed that products and squares of displacement gradients can be neglected [DR78]. Using these assumptions equations (2.1.4) and (2.1.5) can be reduced to:

$$\varepsilon_{ii} = \frac{\partial u_i}{\partial x_i} \quad \text{and} \quad \varepsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right) \tag{2.1.6}$$

and the resulting strain tensor $\bar{\bar{\varepsilon}}$ becomes:

$$\bar{\bar{\varepsilon}} = \begin{Vmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{Vmatrix} \tag{2.1.7}$$

In literature, instead of shear strain components $\varepsilon_{ij}$ engineering shear strains components $\gamma_{ij} = 2\varepsilon_{ij}$ are mostly used.

### 2.1.3 Stress-Strain Relation

In the previous subsections the notions of stress and strain have been introduced and treated so far individually. In this subsection the Hook's law of elasticity is introduced. In the linear theory of elasticity, Hooke's law is an approximation which states that the deformation of an elastic material (strain) is proportional to the force applied and causing the deformation (stress). The linear relationship between stress $\sigma_{ij}$ and strain $\varepsilon_{kl}$ can be formulated mathematically as:

$$\sigma_{ij} = \sum_{kl} c_{ijkl}\varepsilon_{kl} \ , \qquad \text{for } i, j, k, l \in \{x, y, z\} \tag{2.1.8}$$

The coefficients $c_{ijkl}$ are called elastic stiffness constants and the tensor $\bar{\bar{C}}$ elastic stiffness tensor. Recall that both stress as well as strain tensors are second order tensors. This means, that the $\bar{\bar{C}}$ tensor is comprised of 81 coefficients and has to be a fourth order tensor. Due to the symmetry of the strain and stress tensors can be written $c_{ijkl} = c_{jikl} = c_{ijlk}$. In a similar manner the relation between strain and stress can be defined with the help of the inverse of the elastic stiffness tensor called compliance

tensor $\bar{\bar{S}}$:

$$\varepsilon_{kl} = \sum_{ij} s_{ijkl}\sigma_{ij} \ , \qquad \text{for } i,j,k,l \in \{x,y,z\} \tag{2.1.9}$$

In the Appendix both elastic stiffness and compliance coefficients used in this work are presented.

## 2.2 Fundamentals of Semiconductor Device Physics

For the comprehensive understanding of semiconductor devices the study of the physics of semiconductor materials themselves is crucial, due to their natural dependence. Therefore, before elaborating on semiconductor device physics, the first subsection is dedicated to a brief review of the basic physics and properties of a semiconductor crystal, emphasizing mostly on Si. Next, fundamental physics of semiconductor devices used in this work, such as p-n junctions, photodiodes and MOSFETs, are put forward.

### 2.2.1 Silicon Crystal and Band Structure

Crystals are formed by stacking atoms in the three dimensional space by following certain "stacking rules". Assume the atoms to be ideal spheres and closely packed on a plane to form a hexagonal structure as shown in figure 2.2. The next step toward the formation of a three dimensional atomic structure, is to stack the second level of atoms on top of the already formed hexagonal structure. There are two options for the atoms to occupy the next layer, either B or C, as shown in figure 2.2. If the stacking sequence is "ABCABC...", then the crystal has the cubic symmetry and this type of stacking sequence constructs the face-centered cubic (fcc) crystal lattice [STN07]. A crystalline cell of an fcc lattice with an edge length of $\alpha$ is shown in 2.2. Stacking such cells in the three dimensional space leads to the formation of a crystal. The silicon crystal is an object of high symmetry. Exploiting this property with the use of group theory, complicated algebra in describing the crystal can be abbreviated [Hes00]. A crystal consists of a basis and a Bravais lattice. The basis can be anything ranging

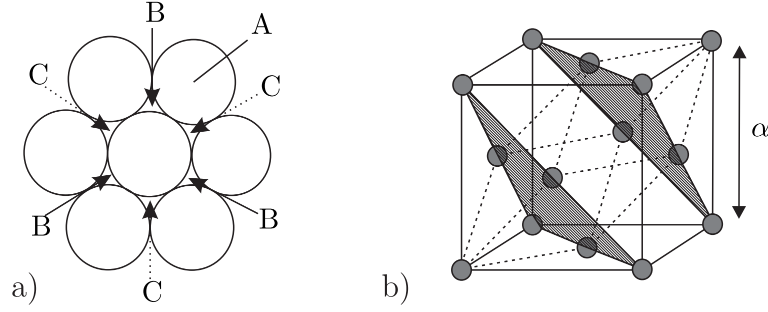


***Figure 2.2: Atom stacking sequence and a simple fcc lattice.*** *a) Atom stacking sequence. The hexagonal structure comprises atom layer A. b) The crystalline cell of a simple fcc lattice is shown here. It is comprised of a cube with atoms at every vertex and also an atom at the center of each cube surface. The atoms on the vertices are in the layer A, if assuming that the shadowed layers are B and C. Following the convention to define the edges of the crystalline cell along the <100> direction, the closely packed planes are the shaded (111) planes. (Adapted from* [STN07]*).*

from atoms to molecules. The Bravais lattice is a set of points $\mathbf{R}$, which is generated by three non-coplanar vectors $\mathbf{a}$, $\mathbf{b}$, and $\mathbf{c}$ of the three dimensional space [Hes00]. These basis vector describe a crystalline solid such that the crystal structure remains invariant under translation through any vector that is the sum of integral multiples of these basis vectors [SN10]. The Bravais lattice vectors $\mathbf{a}$, $\mathbf{b}$ and $\mathbf{c}$ for silicon and its direct lattice $\mathbf{R}$ can be thus described by:

$$\mathbf{a} = \frac{\alpha}{2}\left[0,1,1\right]^{\mathrm{T}},\ \mathbf{b} = \frac{\alpha}{2}\left[1,0,1\right]^{\mathrm{T}},\ \mathbf{c} = \frac{\alpha}{2}\left[1,1,0\right]^{\mathrm{T}} \tag{2.2.1}$$

$$\mathbf{R} = m\mathbf{a} + n\mathbf{b} + p\mathbf{c}, \qquad \text{where } m, n, p\ \in\ \mathbb{Z}. \tag{2.2.2}$$

Similarly, for a given set of basis vectors the reciprocal basis vectors $\mathbf{a}^*$, $\mathbf{b}^*$, and $\mathbf{c}^*$ and the reciprocal lattice $\mathbf{G}$ can be obtained using:

$$\mathbf{a}^* = 2\pi\frac{\mathbf{b}\otimes\mathbf{c}}{\mathbf{a}\cdot\mathbf{b}\otimes\mathbf{c}},\ \mathbf{b}^* = 2\pi\frac{\mathbf{c}\otimes\mathbf{a}}{\mathbf{a}\cdot\mathbf{b}\otimes\mathbf{c}},\ \mathbf{a}^* = 2\pi\frac{\mathbf{a}\otimes\mathbf{b}}{\mathbf{a}\cdot\mathbf{b}\otimes\mathbf{c}} \tag{2.2.3}$$

$$\mathbf{G} = h\mathbf{a} + k\mathbf{b} + l\mathbf{c}, \qquad \text{where } h, k, l\ \in\ \mathbb{Z}. \tag{2.2.4}$$

Silicon as well as many other important semiconductors have diamond lattice structures, which belong to the tetrahedral phases. This means that every atom is surrounded by four equivalent nearest neighbors, which lie at the corner of a tetrahedron.

***Table 2.1: Brillouin zone edges and their corresponding axes.*** *Point Γ corresponds to the center of the Brillouin zone, while points X and L correspond to the middle of the square and hexagonal surfaces respectively. For the lattice constant of relaxed silicon holds* $\alpha = 0.5431$ nm. *(After* [SN10]*).*

| Points and coordinates | Degeneracy | Axis |
|---|---|---|
| $\Gamma, (0,0,0)$ | 1 | |
| $X, {}^{2\pi}/_{\alpha}(\pm1,0,0), {}^{2\pi}/_{\alpha}(0,\pm1,0), {}^{2\pi}/_{\alpha}(0,0,\pm1)$ | 6 | $\Delta, \langle 1,0,0\rangle$ |
| $L, {}^{2\pi}/_{\alpha}(\pm{}^{1}/_{2}, \pm{}^{1}/_{2}, \pm{}^{1}/_{2})$ | 8 | $\Lambda, \langle 1,1,1\rangle$ |
| $K, {}^{2\pi}/_{\alpha}(\pm{}^{3}/_{4}, \pm{}^{3}/_{4}, 0), {}^{2\pi}/_{\alpha}(0, \pm{}^{3}/_{4}, \pm{}^{3}/_{4}), {}^{2\pi}/_{\alpha}(\pm{}^{3}/_{4}, 0, \pm{}^{3}/_{4})$ | 12 | $\Sigma, \langle 1,1,0\rangle$ |

The bond between two nearest neighbors is formed by two electrons with opposite spins [SN10]. The silicon crystal can be visualized as two interpenetrating fcc lattices by shifting each other for a distance $\alpha/4$ along the crystalline cell diagonal, as illustrated in figure 2.3a). Its reciprocal lattice is a body-centered cubic (bcc) lattice and the Wigner-Seitz cell of this lattice is known as the first Brillouin zone, shown in figure 2.3b). Greek letters denote lines of high symmetry, while Roman letters denote symmetry points on the first Brillouin zone. These points and their coordinates are listed in table 2.1. It can be shown [SN10] that a fcc direct lattice with a lattice constant $\alpha$ corresponds to a bcc reciprocal lattice with spacing $4\pi/\alpha$. The reciprocal lattice is of great importance in the visualization of the energy-momentum ($E$-$\boldsymbol{k}$) relationship, when the coordinates of the wave vectors $\boldsymbol{k} = \pm{}^{2\pi}/_{\lambda}$ are mapped into the coordinates of the reciprocal lattice [SN10].

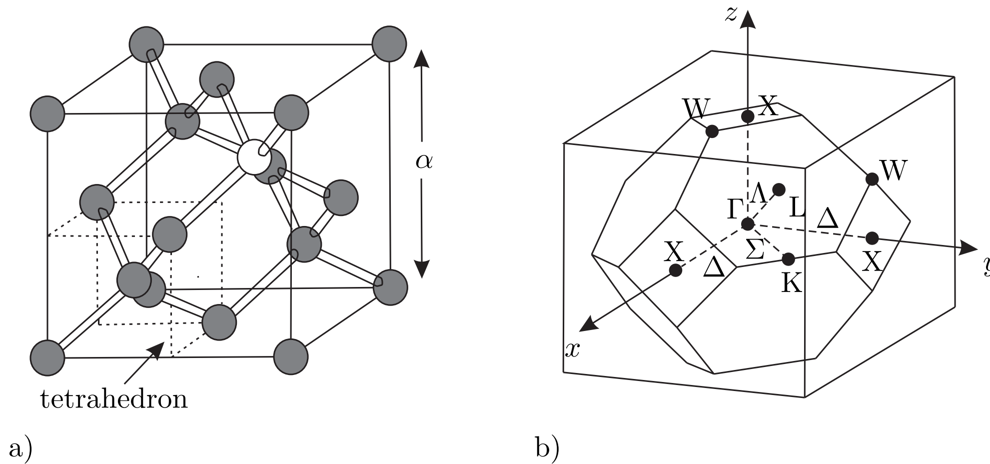


***Figure 2.3: Silicon diamond crystal structure and first Brouillin zone.*** *a) Silicon diamond structured primitive cell (direct lattice) and the corresponding tetrahedron are shown here. b) Silicon primitive cell in the reciprocal lattice can be represented by a Wigner-Seitz cell referred to as first Brillouin zone. Notice that the zone extends to* ${}^{2\pi}/_{a}$ *in one direction. (After* [SN10]*).*

The energy-momentum ($E$-$\boldsymbol{k}$) relationship for the carriers in a crystal is very important, for example in the interactions with photons or phonons (lattice vibrations) where both energy and momentum have to be conserved [SN10]. This will lead to the concept of energy gap (also known as energy bandgap). The variation of energy with the wavevector $\boldsymbol{k}$ in a crystalline solid is described by the band structure. The band structure is usually obtained by solving the Schrödinger equation of an approximate one-electron problem, using the Bloch theorem [SN10]. The symmetry of the lattice in the real space is also reflected in the band structure, thus if the symmetry is reduced severe consequences on the band structure are anticipated. For example translational symmetry imposes the fact that the electronic waves in a crystal are described with Bloch waves, which are plane waves modulated by periodic functions following the crystal periodicity. Silicon features a cubic lattice symmetry, thus its band structure follows the same symmetry. Figure 2.4 illustrates the band structure of silicon. Notice the shaded region is a forbidden energy range, where no allowed states exist. This region is the energy gap or bandgap and allowed electronic states exist either in the upper or lower side of the gap. The upper bands are called conduction bands $E_C$, while the lower ones valence bands $E_V$. As illustrated in figure 2.4 the minimum of the conduction band in silicon is located near the $X$ point along the $\Delta$ symmetry axis. The valence band maximum is located at the $\Gamma$ point. Thus the minimum energy gap in silicon lies between two different wave vectors and thus it is an indirect energy gap $E_g$ and hence silicon an indirect semiconductor. At room temperature and under normal atmospheric pressure the bandgap for relaxed high-purity Si lies at 1.12 eV and exhibits a negative temperature coefficient [SN10]. For the lowest conduction band in silicon there are six equivalent conduction band valleys along the principal $\langle 100\rangle$ axes, which can be attributed to the symmetry of fcc lattice. For the lower bands, there exist three valence bands. Two of them are degenerate at $k = 0$ ($\Gamma$ point), while the third one lies very close since the spin-orbit interaction causes a splitting of the band with a split-off energy equal to 44 meV. The former degenerate bands are the heavy hole (HH) and light hole (LH) band, while the latter one is called split-off (SO) band. This valence band structure is encountered in all cubic semiconductors.

Near the conduction band edges (i.e., principal band minima) the band structure can be approximated by a parabolic equation representing ellipsoidal constant energy

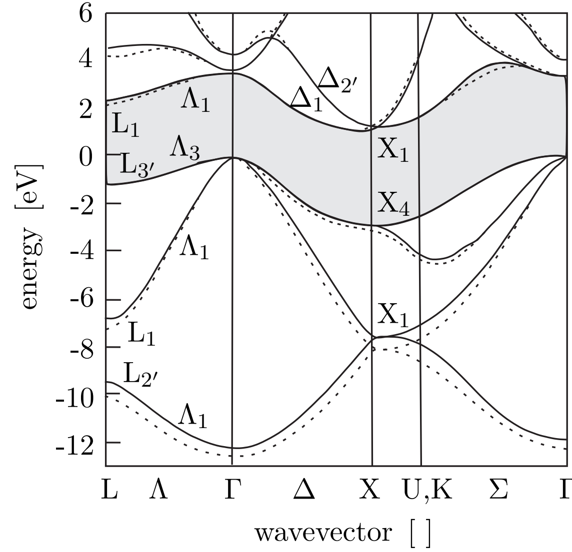


***Figure 2.4: Silicon energy band structure.*** *Notice that the minimum of the conduction band at $X_1$ is misaligned with the valence band maximum at $\Gamma$. (After* [YC10]*).*

surfaces, as shown in figure 2.5:

$$E(k) = \frac{\hbar^2}{2}\left(\frac{k_x^2}{m_l} + \frac{k_y^2}{m_t} + \frac{k_z^2}{m_t}\right) \tag{2.2.5}$$

where $\hbar$ the reduced Planck constant and $m_l$, $m_t$ the associated longitudinal (along the symmetry axis) and transversal (perpendicular to the symmetry axis) effective masses respectively. For the valence band edges, the same parabolic approximation can be followed but only along a certain direction. Thus, the upper two valence bands can be approximated with two parabolic bands with different curvatures. However, due to the interactions between the carriers of the bands near the extremum, approximations beyond the order of parabolic are necessary [Hes00]. A good approximation as warped spheres is given by [DKK55]:

$$E\left(k\right) = \frac{\hbar^2}{2m_0}\left(Ak^2 \pm \sqrt{B^2k^4 + C^2\left(k_x^2k_y^2 + k_y^2k_z^2 + k_z^2k_x^2\right)}\right) \tag{2.2.6}$$

where $m_0$ is the electron rest mass, the + sign is for the light hole band (the band with greater convexity or lower effective mass), the - sign is for the heavy hole band (the band with lower convexity or greater effective mass) and $A$, $B$, $C$ are the inverse band

parameters [Pul10]. The shape depends strongly though on the energy, but usually the surfaces are described as those of warped spheres. The effective mass of the bands are thus in general a tensorial defined as [SN10]:

$$\frac{1}{m_{ij}} \equiv \frac{1}{\hbar^2} \frac{\partial^2 E(k)}{\partial k_i \partial k_j} \tag{2.2.7}$$

Approximating the warped surfaces as spheres allows effective masses for the heavy $m_{hh}$ and light $m_{lh}$ holes to be identified as scalar values, used mostly in calculations [Pul10].

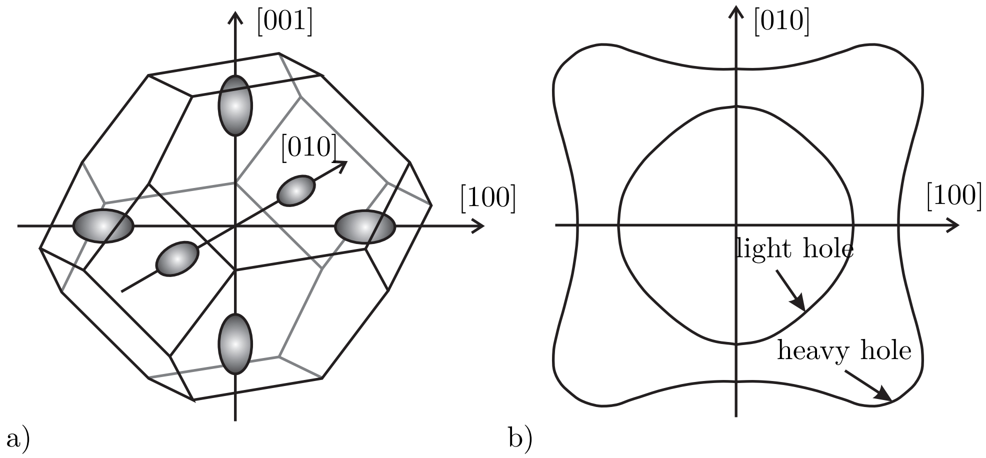


***Figure 2.5: Constant energy surfaces of conduction and valence bands in silicon.*** *a) Sixfold degenerate conduction band prolate spheroids (ellipsoids) along the principal axes* ⟨100⟩ *with their centers located at about three-fourths of the distance from the Brillouin zone center. b) Heavy and light holes warped constant energy surfaces. (After* [SN10] *and* [Hes00]*).*

The energy bands of silicon has been extensively studied the last 50 years. Several numerical methods have been used in order to solve Schrödinger equation and visualize the band structure. Most frequently the empirical pseudopotential method is used. This technique is based on the observation that the effective potential for electrons near the Fermi level can be split into two parts, the part due to the core (hard core ionic potential), and the part due to the other valence electrons. The assumption of this method is that the relative effect of the core in silicon is small, so that it can be replaced by an effective soft pseudopotential [Phi58]. Another method also frequently used in the literature is the $\boldsymbol{k} \cdot \boldsymbol{p}$ method [Sei40], which expands the Schrödinger equation by a $\boldsymbol{k} \cdot \boldsymbol{p}$ term and a parabolic term in $k$. Once knowing both energy and

periodic function at a point $\boldsymbol{k}_0$ and treating the aforementioned terms as perturbations the complete band structure can be calculated using perturbation theory [YC10]. The method called tight-binding approximation constitutes another technique of calculating the energy dispersion of silicon. This technique starts from a completely opposite approach in comparison to the pseudopotential method, which assumes that electrons are nearly free and that their wave functions can be approximated by plane waves. Here the electrons are assumed to be tightly bound to their nuclei as in atoms. The atoms will be brought then together and the electron wave functions will be approximated by linear combinations of the atomic wave functions [YC10]. However, this method would work well for the valence band electrons since these are concentrated mainly in the covalent bonds, thus retaining their atomic character. For the conduction band electrons, which are delocalized, this method is not a good choice [YC10].

Moreover, the carrier concentration and their distribution in each band and sub-band is also very important for the electronic properties of a semiconductor material. Starting from a high-purity silicon crystal the number of electrons $n$ in the occupied conduction band levels can be calculated by multiplying the density of states $N(E)$ with the occupancy $F(E)$ and integrating over the whole conduction band

$$n = \int_{E_C}^{\infty} N\left(E\right) F\left(E\right) dE \tag{2.2.8}$$

However, near the conduction band minima and for low carrier densities and temperatures the density of states in silicon can be approximated by:

$$N\left(E\right) = M_C \frac{\sqrt{2}}{\pi^2} \frac{\left(m_l m_t m_t\right)^{1/2} \left(E - E_C\right)^{1/2}}{\hbar^3} \tag{2.2.9}$$

and the integral in equation (2.2.8) can be solved using the Fermi-Dirac distribution function to describe the occupancy as:

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_C}{kT}\right) \quad \text{with} \quad N_C \equiv 2M_C \left(\frac{2\pi kT}{h^2}\right)^{3/2} \left(m_l m_t m_t\right)^{1/2} \tag{2.2.10}$$

where $k$ is the Boltzmann constant, $h$ the Planck constant, $T$ is the temperature, $m_l$, $m_t$ are the effective masses along silicon principal axes, $M_C$ the number of equivalent minima in the conduction band, $N_C$ is the effective density of states in the conduction

band and $F_{1/2}$ is the Fermi-Dirac integral of order $1/2$. Consequently, for each $i^{th}$ pair of ellipsoids in the conduction band the number of electrons $n^i$ can be formulated:

$$n^i = \frac{N_C}{3} \frac{2}{\sqrt{\pi}} F_{1/2} \left( \frac{E_F - E_C}{kT} \right) \tag{2.2.11}$$

where $i$ denotes the $i^{th}$ pair of ellipsoid. Following a similar procedure near the top valence band edges and accounting the contributions of HH and LH bands separately yields for the hole density $p$:

$$p = N_V^{hh} \frac{2}{\sqrt{\pi}} F_{1/2} \left( \frac{E_V^{hh} - E_F}{kT} \right) + N_V^{lh} \frac{2}{\sqrt{\pi}} F_{1/2} \left( \frac{E_V^{lh} - E_F}{kT} \right) \tag{2.2.12}$$

$$N_V^{hh} \equiv 2 \left( \frac{2\pi m_{hh} kT}{h^2} \right)^{3/2} \quad \text{and} \quad N_V^{lh} \equiv 2 \left( \frac{2\pi m_{lh} kT}{h^2} \right)^{3/2} \tag{2.2.13}$$

where $m_{lh}$, $m_{hh}$ are the effective masses of light and heavy holes respectively, $N_V^{lh}$, $N_V^{hh}$ are the effective density of states in the LH and HH valence band respectively and $F_{1/2}$ is the Fermi-Dirac integral of order $1/2$.

### 2.2.2 p-n Junctions

In the previous section the intrinsic case of silicon and its band structure was studied. However, in CMOS technology donor or acceptor impurities are introduced in the substrate, in order to facilitate the needed free carriers to allow conduction. Impurity atoms are introduced through implantation in the silicon crystal lattice, thus replacing silicon atoms. Implantation of acceptor atoms with three valence electrons like Boron ([He]2s$^2$ 2p$^1$) in the silicon lattice leads to the formation of covalent bonds between the implanted atom and the surrounding silicon atoms, leaving however an electron deficiency in one of the four covalent bonds (p-type material). Similarly implanting a donor atom with five valence electrons like Arsenic ([Ar]4s$^2$ 3d$^1$0 4p$^3$) or Phosphor ([Ne]3s$^2$ 3p$^3$) will form all four covalent with the surrounding silicon atoms, leaving in this case one valence electron of the donor atom weakly bound to the valence band or nearly "free" (n-type material). The introduced energy levels of impurities lie within the energy gap of intrinsic silicon either close to the conduction band minimum (donors) or close to the valence band maximum (acceptors). Thus the Fermi level is shifted

toward the conduction or the valence band, respectively, as shown in figure 2.6.

Let us now assume an abrupt change of the doping of a semiconductor material from p-type to n-type. The interface between the two regions is known as p-n junction. At thermal equilibrium the net current flow through the junction is zero, thus imposing the constraint that the Fermi level within the material must be spatially constant.

Thus, the Fermi levels in the n- and p-type region respectively have to align to each other. As as consequence the corresponding energy bands in the p- and n-type region do not lie at the same level, creating the so called built-in or diffusion potential, which in turn implies an electric field within the junction. The latter will cause the flow of free carriers or the formation of an electric current, which is the drift-current component. Moreover, if $N_A$ and $N_D$ are the fully ionized impurity concentrations in the p- and n-type side respectively, the concentration gradient will also cause the diffusion of electrons from the n- to the p-region and holes from the p- to the n-region. This current component is the diffusion-current and fully balances the drift-current at equilibrium, thus fulfilling the net zero current condition and the flat Fermi level. The built-in potential $\psi_{bi}$ assuming complete ionization of impurities in non degenerate semiconductors is given by [SN10]:

$$\psi_{bi} \approx \frac{kT}{q} \frac{N_D N_A}{n_i^2} \tag{2.2.14}$$

where $n_i$ is the intrinsic carrier concentration. Due to the mentioned flow of electrons to the p-side, where electrons have a high probability to recombine with holes, the n-side close to the interface with the p-region is depleted from free carriers and only positive charged ions are left behind. Similarly for the interface on the side of the p-type region which is left behind with negatively charged ions. This transition region is called depletion region or space-charge region (SCR) and has a width $W_D$ which is given by [SN10] under the assumption of an abrupt junction:

$$W_D = \underbrace{\sqrt{\frac{2\epsilon_s\left(\psi_{bi} - 2kT/q\right)}{q} \frac{N_A}{N_D(N_A + N_D)}}}_{W_{Dn}} + \underbrace{\sqrt{\frac{2\epsilon_s\left(\psi_{bi} - 2kT/q\right)}{q} \frac{N_D}{N_A(N_A + N_D)}}}_{W_{Dp}} \tag{2.2.15}$$

$$= \sqrt{\frac{2\epsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\left(\psi_{bi} - 2kT/q\right)} \tag{2.2.16}$$

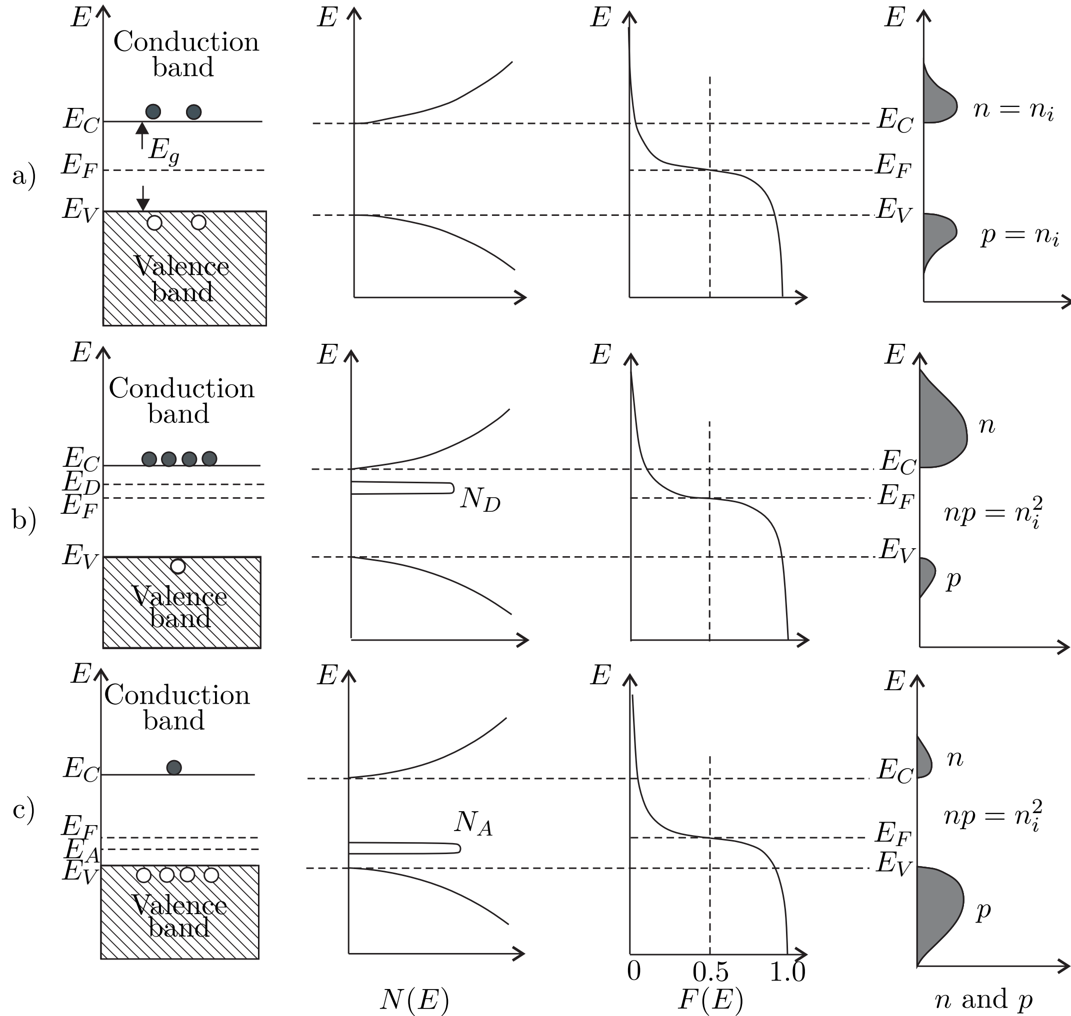


***Figure 2.6: Energy band diagram and carrier distributions of an n-type and a p-type material.*** *a) Fermi level $E_F$, conduction band $E_C$ and valence band $E_V$ energy level for intrinsic silicon at thermal equilibrium. Note that electron concentration $n$ and hole concentration $p$ are equal to the square of the intrinsic carrier concentration $n_i$. b) $E_F$, $E_C$, $E_V$ and donor $E_D$ energy levels for n-type silicon at thermal equilibrium. In this case electron concentration $n$ is larger than the hole concentration $p$ but their product is equal to the intrinsic carrier concentration $n_i$. c) $E_F$, $E_C$, $E_V$ and acceptor $E_A$ energy levels for p-type silicon at thermal equilibrium. In this case hole concentration $p$ is larger than the electron concentration $n$ while their product equals to the square of the intrinsic carrier concentration $n_i$. (After* [SN10] *and* [TN98]*).*

where $\epsilon_s$ the permittivity of silicon, $k$ the Boltzmann constant, T the temperature, $N_A$ and $N_D$ are the fully ionized impurity concentrations in the p- and n-type side, respectively and $W_{Dn}$, $W_{Dp}$ the SCR widths in the n- and p-type region, respectively. Until now no voltage was assumed to be applied on the p-n junction. An externally applied voltage $V$ would break the thermal equilibrium condition and lead to an electrostatic potential variation equal to $\psi_{bi} - V$. The depletion region width becomes therefore:

$$W_D = \sqrt{\frac{2\epsilon_s\left(\psi_{bi} - V - 2kT/q\right)}{q}\frac{N_A + N_D}{N_A N_D}} \tag{2.2.17}$$

where $V$ is the applied voltage, which is positive for forward biasing the junction (higher potential on the p-region) and negative for reverse biasing. The term $2kT/q$ in equation (2.2.17) will give more accurate results for the properties of the depletion region [SN10], but can be omitted in hand calculations. The charge per unit area distributed in the depletion region gives rise to a depletion region capacitance $C_D = \epsilon_s/W_D$, equivalently to parallel plate capacitor of separation $W_D$ and dielectric constant $\epsilon_s$.

Looking at the minority carrier densities $n$ and $p$ at thermal equilibrium in an abrupt p-n junction, depicted in figure 2.7, and assuming that Maxwell-Boltzmann statistics apply, can be obtained:

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right),\ p = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \tag{2.2.18}$$

Applying a voltage at the junction leads to a change to the minority carrier density on both p- and n-type side and by defining quasi-Fermi levels $E_{Fn}$ and $E_{Fp}$ for each side respectively can be obtained:

$$n = n_i \exp\left(\frac{E_{Fn} - E_i}{kT}\right),\ p = n_i \exp\left(\frac{E_i - E_{Fp}}{kT}\right) \tag{2.2.19}$$

### 2.2.3 p-n Junction Based Photodiodes

The depletion region of a p-n junction and the ability to increase its width by the application of an external reverse bias, as equation (2.2.17) dictates, along with the photoelectric effect enable the use of p-n junctions as photodiodes. The internal field

at the junction serves as the separation mechanism of generated electron-hole pairs (ehps) due to photon energy absorption impeding that way their direct recombination. Before continuing with the descriptions of important properties of photodiodes such as the dark current $I_{dark}$, the photocurrent $I_{ph}$, the quantum efficiency $\eta$ and the sensitivity $S$, the fundamentals of semiconductor based phototransduction are put forward.

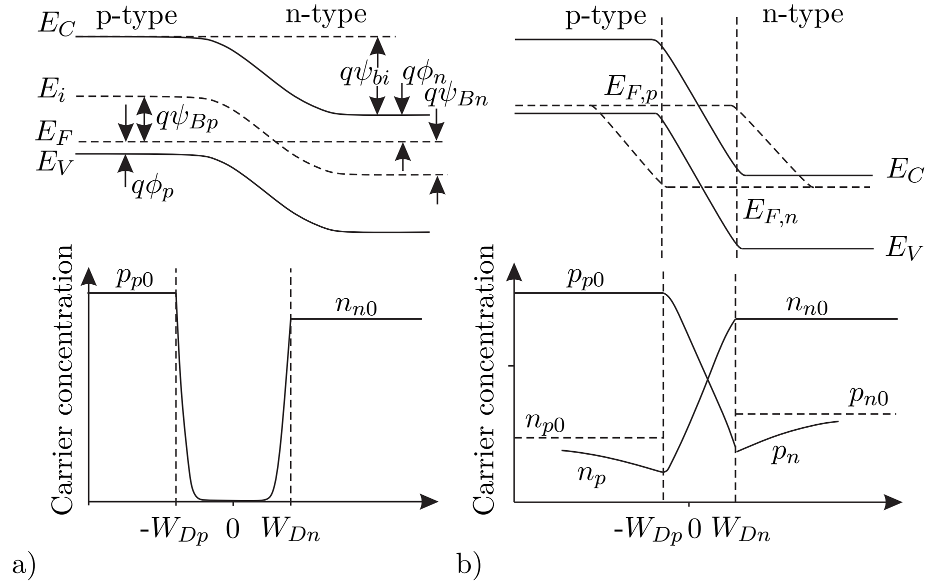


***Figure 2.7: Energy band diagram of a p-n junction.*** *a) Free carrier concentration and energy bands in a p-n junction under thermal equilibrium. b) Carrier concentration and energy bands in a p-n junction under reverse bias. (After* [SN10] *and* [Hes00]*).*

Let electromagnetic radiation propagate through a semiconductor material with an initial intensity or photon flux $\Phi_0(\lambda)$, where $\lambda$ is the wavelength of the impinging radiation. The photon flux $\Phi(\lambda)$ per unit area in units of photons/m$^2$/s can be obtained by dividing the optical power density of the electromagnetic wave, described through the Poynting vector, with the photon energy $E_{ph} = hc/\lambda = hf$. With the help of the wavelength dependent absorption coefficient $\alpha(\lambda)$ the photon flux at a certain depth $z$ of the semiconductor material across the propagation direction (assumed to be vertical to the planar interface air-semiconductor), yields for the remaining (not absorbed) photon flux $\Phi(z, \lambda)$:

$$\Phi(z, \lambda) = \Phi_0(\lambda) \exp(-\alpha(\lambda) z) = \left( \frac{\sqrt{\epsilon/\mu}\varepsilon_0^2}{hc/\lambda} \right) \exp\left( -\frac{4\pi k_r}{\lambda} z \right) \qquad (2.2.20)$$

where $h$ is the Planck constant, $\lambda$ and $f$ are the wavelength and frequency of the impinging radiation respectively, $c$ denotes the speed of light, $k_r$ is the imaginary part of the refractive index of the semiconductor material, $\epsilon$ and $\mu$ the permittivity and permeability of the material respectively. The absorption of photons in the semiconductor material leads to the generation of an electron-hole pair through the excitation of valence band electrons to the conduction band contributing to the formation of a photocurrrent $I_{ph}$. However, for an electron of the valence to be excited to the conduction band both energy and momentum have to be conserved. In the case of light illumination on an indirect semiconductor the photon energy $E_{ph}(\lambda) = hf = hc/\lambda$ can be partitioned in three categories, namely:

$$\left.\begin{array}{rll} & E_{ph}(\lambda) & < E_g \\ E_g < & E_{ph}(\lambda) & < E_d \\ & E_{ph}(\lambda) & > E_d \end{array}\right\} \tag{2.2.21}$$

where $E_g$ the indirect energy bandgap of the semiconductor (1.124 eV at $T = 300$K for Si) and $E_d$ the direct energy bandgap of the semiconductor (3.4 eV at $T = 300$K for Si). The absorption of photons and the consequent generation of an electron-hole pair requires not only the conservation of energy in the photoeffect process but also the momentum conservation of the electron-photon system. Due to this reason only vertical band-to-band transitions are allowed in the band structure [Sin96]. However, involving lattice vibrations (phonons) in an electron-photon system will introduce the needed momentum $\hbar k$ and allow that way indirect band-to-band transitions. The absorption of photons with energy in the first category of equation (2.2.21) will take place only if there are forbidden energy states within the energy bandgap, introduced for example by impurities as described in section 2.2.2. Here, the absorption or emission of a phonon needs to take place as well. This process is called extrinsic transition [SN10] and constitutes the fundamental of the entire silicon based solid-state imaging [Dur09]. Intrinsic transitions (band-to-band) involve photons belonging to the other two categories of equation (2.2.21) [SN10]. Involving again an absorption or emission of a phonon is essential for photons with energy $E_{ph}(\lambda) < E_d$ to contribute in the intrinsic photoeffect. The optical generation rate of carriers $G_{op}$ can then be obtained as:

$$G_{op} = \eta_{int}(\lambda)\alpha(\lambda)\Phi(z,\lambda) = \eta_{int}(\lambda)\alpha(\lambda)\Phi_0(\lambda)\exp(-\alpha(\lambda)z) \tag{2.2.22}$$

where $\eta_{int}$ is the internal quantum efficiency, which describes the number of the generated ehps per absorbed photon and $\alpha(\lambda)$ denotes the wavelength dependent absorption coefficient. Here, it is worth to note that the external quantum efficiency $\eta_{ext}$ can also be defined as the number of the generated ehps per incident photon and is used mainly in photodetector systems benchmarking. The internal quantum efficiency is mostly assumed to be equal to unity for photon energies larger than the bandgap energy of the material. However, unwanted absorption mechanisms such as excitation of already free carriers or generation of ehps, which remain bound together by Coulombic attraction [Pul10] (excitons), render $\eta_{int}$ less than unity. Moreover, for photon energies larger than an average generation energy $E_{gen}$ ($E_{gen} \approx 3.65$eV for Si) $\eta_{int}$ can be larger than unity, since there is enough energy to excite more than one valence electron. Nevertheless, when illuminating with visible light the approximation $\eta_{int} \approx 1$ is reasonable.

At this point, after the brief introduction in semiconductor based phototransduction, important properties of p-n junctions deployed as silicon based photodetectors are presented. First, the external quantum efficiency $\eta_{ext}$ constitutes one of the fundamental properties of a photodetector and is defined as the probability of an ehp generation from an impinging photon or the number of the generated ehps per incident photon [SN10]. The external quantum efficiency of a detector $\eta_{ext}$ is strongly wavelength dependent and can be measured by determining the generated photocurrent $I_{ph}$ under a given photon flux $\Phi$. Recall that the photon flux can be calculated by dividing the radiant flux $P_{opt}$ with the photon energy $E_{ph}$:

$$\eta_{ext}(\lambda) = \frac{I_{ph}}{q}\Phi(\lambda) = \frac{I_{ph}}{q}\left(\frac{E_{ph}}{P_{opt}}\right) \tag{2.2.23}$$

Another metric describing the spectral response of the photodetector is the sensitivity $S$ in units of A/W and is defined as the ratio of the measured photocurrent under a given radiant flux $P_{opt}$:

$$S = \frac{I_{ph}}{P_{opt}} = \eta_{ext}(\lambda)\frac{q}{E_{ph}} \tag{2.2.24}$$

Furthermore, the photocurrent generated within the reversed biased depletion region of a p-n junction when illuminated with light can be in detail described making use of equation (2.2.22). Some of the photogenerated carriers will be generated in the

depletion region and will be directly separated from the internal electrical field of the SCR (recall subsection 2.2.2) and constitute the drift component of the photocurrent. Carriers generated outside of the SCR have to diffuse until reaching the reversed biased junction and will constitute the diffusion component of the photocurrent. Following the analysis described in [SN10] by solving the continuity equation the photocurrent $I_{ph}$ is obtained:

$$I_{ph} = I_{ph,drift} + I_{ph,diffusion} \tag{2.2.25}$$

$$I_{ph} = qA\Phi_0 \left[1 - \exp(-\alpha(\lambda)W_D)\right] + qA\Phi_0 \frac{\alpha(\lambda)L_p}{1+\alpha(\lambda)L_p} \exp(-\alpha(\lambda)W_D) + \frac{qp_{n0}AD_p}{L_p}$$

$$I_{ph} \approx qA\Phi_0 \left[1 - \frac{\exp(-\alpha(\lambda)W_D)}{1+\alpha(\lambda)L_p}\right] \tag{2.2.26}$$

$$D_p = \left(\frac{kT}{q}\right)\mu_p \quad \text{and} \quad L_p = \sqrt{D_p \tau_p}$$

where $A$ the photodetector active area, $p_{no}$ the equilibrium hole density, $\mu_p$ the hole mobility, $\tau_p$ the lifetime of the excess holes, $D_p$ and $L_p$ the diffusion coefficient for holes and the diffusion length for holes respectively. Equation (2.2.23) with the help of (2.2.26) and accounting for the reflection coefficient $R$ yields:

$$\eta_{ext}(\lambda) = (1-R)\left[1 - \frac{\exp(-\alpha(\lambda)W_D)}{1+\alpha(\lambda)L_p}\right] \tag{2.2.27}$$

In the last part of this subsection dark current considerations of p-n junction based photodetectors are put forward. Dark current or reverse biased leakage current belongs to the vital properties of a photodiode or a pixel within an image sensor, since it limits the device dynamic range by increasing shot noise and the overall performance of the imager. Moreover, there is a correlation between dark current and fixed pattern noise reduction [LFM+03]. Therefore, a theoretical description and categorization of the different dark current components in p-n junction based photodiodes will be given in this part.

The first dark current component to be addressed is the diffusion dark current from the neutral region outside of the depletion region, where there is no electric field [SN10]. Both electrons and holes are taken into account as minority carriers in the p- and n-type

regions respectively. Therefore, the diffusion current comprises of both the electron and hole diffusion currents. Under the assumption of an abrupt p-n junction depletion layer, the assumption that Boltzmann statistics are valid and that the minority carrier densities are much smaller compared with the majority ones (low-injection assumption) the diffusion current $I_{diff}$ is obtained:

$$I_{diff} = \frac{qAD_p p_{no}}{L_p} + \frac{qAD_n n_{po}}{L_n} \equiv \frac{qAD_p n_i^2}{L_p N_D} + \frac{qAD_n n_i^2}{L_n N_A} \tag{2.2.28}$$

where $A$ the area of the p-n junction interface, $D_n$ and $D_p$ the diffusion coefficient of electrons and holes, respectively, $L_n$ and $L_p$ the diffusion length of electrons and holes, respectively and $N_D$ and $N_A$ the donor (in n-type region) and acceptor (in p-type region) impurity concentrations, respectively. Note that $A$ is not only the horizontal area of the photodiode $A_{hor}$ but also the vertical area around the perimeter of the diode as illustrated in figure 2.8. Thus it can be rewritten for the diffusion current $I_{diff}$:

$$I_{diff} = \frac{q(A_{hor} + Pd_{ver})D_p n_i^2}{L_p N_D} + \frac{q(A_{hor} + Pd_{ver})D_n n_i^2}{L_n N_A} \tag{2.2.29}$$

where $P$ the perimeter of the SCR at the semiconductor surface and $A_{hor}$ the area of the horizontal p-n junction interface in the semiconductor body.

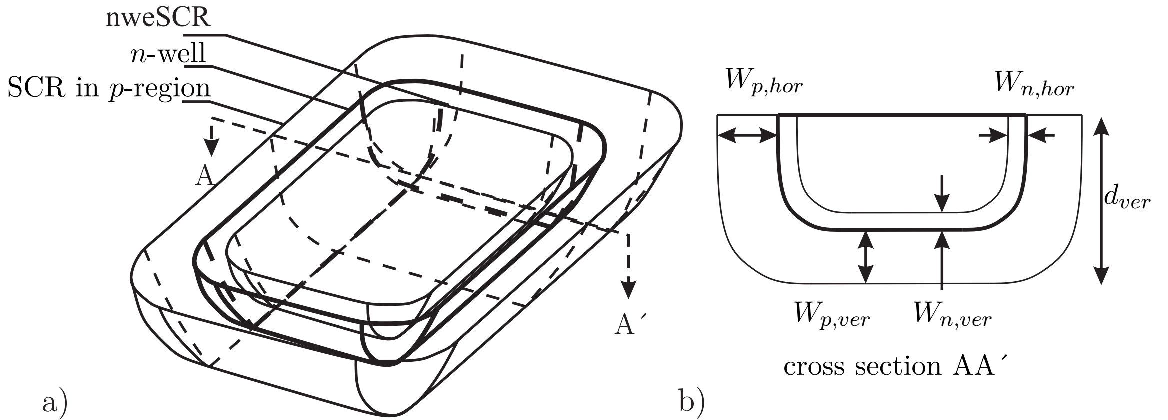


***Figure 2.8: A three-dimensional aspect of an abrupt p-n junction.*** *Note the different areas of the p-n junction in a) accounted in the calculation of the diverse dark current components and its cross section in b). $W_{p,hor}$ and $W_{n,hor}$ are the widths of the horizontal SCR in the p and n-region respectively. Similarly, $W_{p,ver}$ and $W_{n,ver}$ denote the widths of the vertical SCR in the p and n-region respectively.*

Next to the diffusion current, another important component is the current formed from minority carriers generation within the depletion region. When external voltage is applied at the junction, the thermal equilibrium is disturbed ($np \neq n_i^2$). Processes such as generation or recombination of carriers act toward the restoration of the system's equilibrium. In the case of reverse bias ($pn < n_i^2$) thermal generation of carriers is taking place through the help of bulk traps with energy levels within the energy bandgap of silicon. Here, two main generation mechanisms can be distinguished. The first includes generation of minority carriers at the interface of the depletion region with the semiconductor surface, while the second includes the generation of carriers within the depletion away from the surface. This categorization is performed since the energy levels of the traps within the silicon crystal volume are mainly introduced by dopants and/or lattice defects, while at the silicon surface traps are primarily caused by dangling bonds (i.e., ionic charges on or outside silicon's surface, which induce image charges in silicon [SN10]). The rate of ehps generation can be described by Shockley-Read-Hall statistics [Sch06] [SN10]. Under the assumptions $p \ll n_i$ and $n \ll n_i$ for the reversed biased p-n junction the generation rate in the semiconductor volume $U_V$ and semiconductor surface $U_S$ is given by:

$$U_V = -\frac{\sigma_p \sigma_n v_{th} N_{t,V} n_i}{\sigma_n \exp\left[(E_{t,V} - E_i)/kT\right] + \sigma_p \exp\left[(E_i - E_{t,V})/kT\right]} \tag{2.2.30}$$

$$U_S = -\frac{\sigma_p \sigma_n v_{th} N_{t,S} n_i}{\sigma_n \exp\left[(E_{t,S} - E_i)/kT\right] + \sigma_p \exp\left[(E_i - E_{t,S})/kT\right]} \tag{2.2.31}$$

where $\sigma_n$, $\sigma_p$ the electron and hole scattering cross sections, $N_{t,V}$, $N_{t,S}$ the trap densities at the semiconductor volume (in units of $m^{-3}$) and surface (in units of $m^{-2}$) respectively, $E_{t,V}$, $E_{t,S}$ the trap energy levels at the semiconductor volume and surface respectively and $v_{th}$ the thermal velocity of the carriers. Knowing the generation rate and by integrating over the depletion region in the volume and at the surface under the same assumptions yields for the volume and surface generation currents $I_{ge,V}$ and $I_{ge,S}$ respectively:

$$I_{ge,V} = q n_i W_D (A_{hor} + P d_{vert}) \frac{1}{\underbrace{\tau_{gp} \exp\left[\frac{E_{t,S} - E_i}{kT}\right] + \tau_{gn} \exp\left[\frac{E_i - E_{t,V}}{kT}\right]}_{\tau_g}} \tag{2.2.32}$$

$$I_{ge,S} = qn_i PW_{D,surf} \underbrace{\frac{s_{gn}s_{gp}}{s_{gn}\exp\left[\frac{E_{t,S}-E_i}{kT}\right] + s_{gp}\exp\left[\frac{E_i-E_{t,S}}{kT}\right]}}_{s_g} \tag{2.2.33}$$

where $\tau_{gn}= (\sigma_n v_{th} N_{t,V})^{-1}$, $\tau_{gp}= (\sigma_p v_{th} N_{t,V})^{-1}$ the generation time of electron and holes in the depletion region in the semiconductor volume respectively, $s_{gn}= \sigma_n v_{th} N_{t,S}$ and $s_{gp}= \sigma_p v_{th} N_{t,S}$ the surface generation velocities of electron and holes respectively. Moreover, $\tau_g$ and $s_g$ are defined as the generation lifetime of carriers in the depletion region in the semiconductor volume and the surface generation velocity of carriers in the depletion region at the surface respectively.

### 2.2.4 Metal-Oxide-Semiconductor Capacitors

After having introduced the p-n junction, another fundamental device in CMOS technology is the MOS capacitor. Similarly to the previous subsection, an ideal structure of an MOS capacitor is assumed, as shown in figure 2.9a). The capacitance of this structure in the general case consists of a series combination of an oxide capacitance $C_{OX}$ and a semiconductor capacitance $C_D$ as depicted in figure 2.9b). An ideal capacitor is defined as the MOS structure with no interface traps or oxide charges and with zero leakage through the oxide layer (i.e., infinite insulator resistivity). For the case shown in figure 2.9c) the metal work function $\phi_m$ is less than the semiconductor work function $\phi_s$ (non-zero $\phi_{ms}$), thus causing a band bending near the oxide-semiconductor interface in equilibrium. Therefore, in order to reach the flatband condition, where all bands are flat (or exhibit zero slope) within the semiconductor, a voltage $V_{FB}$ has to be applied at the metal gate of the device. With respect to the flatband condition, there are three cases that an MOS capacitor can be in, once voltage is applied at the metal gate.

In case of a more negative applied voltage $V$ at the metal gate with respect to the flatband voltage $V_{FB}$, positive charges on the semiconductor side are gathered near the oxide-semiconductor surface in order to maintain the space-charge neutrality principle. Since there is no leakage through the ideal structure, an electric field is formed within the oxide layer and consequently the band bending is induced. The conduction band edge $E_V$ bends upwards near the surface getting closer to the Fermi level $E_F$. Since the carrier density depends exponentially on the energy difference $(E_F - E_V)$ an accumulation of majority carriers (in this case holes) is caused at the

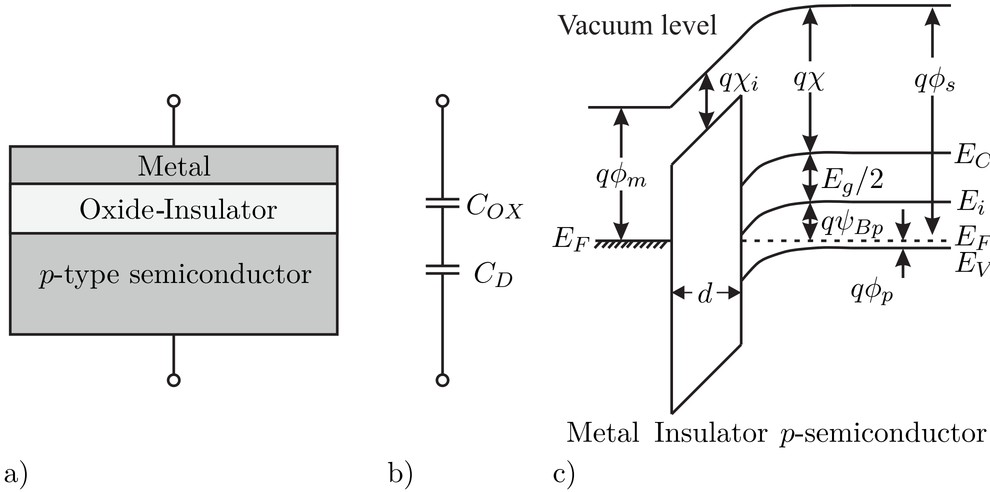


***Figure 2.9: Structure of an ideal metal-oxide-semiconductor capacitor.*** *a) The structure of an ideal MOS capacitor b) An equivalent electrical model c) Energy band diagram of the idealized device. Note how the non-zero $\phi_{ms}$ ($\phi_m<\phi_s$) causes a band bending. $\chi$ and $\chi_i$ are the electron affinities for the semiconductor and the insulator respectively. $\psi_{Bp}$ and $\phi_p$ are potentials measuring the position of the Fermi level $E_F$ with respect to the intrinsic energy level $E_i$ and the band edge $E_V$ respectively.*

interface. This situation is called accumulation and in this case the total capacitance illustrated in figure 2.9 becomes almost equal to $C_{OX}$.

The next case that the semiconductor surface can exist, arises after the application of a slightly larger positive voltage at the metal gate with respect to the flatband voltage. Under this condition, the positive charges deposited on the metal gate repel the positive charges from the semiconductor surface, thus leading to a depletion from majority carriers near the interface with a depletion region width of $W_D$. Now the bands are bend downward, hence allowing the conduction band edge to come closer to the Fermi level. This situation is called depletion and in this case the total capacitance illustrated in figure 2.9 has to account for the depletion capacitance $C_D$ in the semiconductor body.

The last and very interesting case arises when an even more positive voltage at the metal gate with respect to the flatband voltage is applied. Then the bands bend even more downward, causing a deeper depletion until the point when the intrinsic level $E_i$ crosses the Fermi level $E_F$ at the semiconductor surface. In other words, at this point the majority carriers near the surface are not anymore holes but electrons. Therefore, the surface is facing the well known inversion, an effect with vast importance in the operation of MOS field-effect transistors (FETs). Once inversion of the semiconductor

surface has started, the depletion region stops widening because of the high mobile electron density at the interface region. This large density of induced free carriers causes all additional applied voltage at the metal gate to be dropped across the oxide since small changes in semiconductor band bending will cause exponential increases in the inversion charge [MS08]. The maximum width of the depletion region $W_{D,max}$ can be obtained following an analysis similar to [MS08] and [SN10]:

$$W_{D_{max}} \cong \sqrt{\frac{4\epsilon_s \psi_B}{qN_A}} = \sqrt{\frac{4\epsilon_s (E_i - E_F)}{q^2 N_A}} \tag{2.2.34}$$

where $\psi_B$ measures the position of the Fermi level $E_F$ with respect to the intrinsic energy level $E_i$, $\epsilon_s$ the permittivity of silicon and $N_A$ the acceptors impurity concentration. The onset of strong inversion is assumed to begin by a surface potential $\psi_S$ equal to $2\psi_B$.

Table 2.2 summarizes the total capacitance under the three operating conditions for an MOS capacitor.

***Table 2.2: MOS capacitance in different regions of operations.*** *Note how the capacitance saturates under the inversion condition. This is a unique characteristic of MOS capacitors not encountered in p-n junctions.*

| Capacitance | Accumulation | Depletion | Inversion |
|---|---|---|---|
| $C_{MOS}$ | $C_{OX}$ | $\dfrac{C_{OX}}{1 + \dfrac{C_{OX} W_D}{\epsilon_s}}$ | $\dfrac{C_{OX}}{1 + \dfrac{C_{OX} W_{D,max}}{\epsilon_s}}$ |

Before closing this subsection, it is worth to note that an MOS capacitor in modern processes is fabricated using n+ or p+ heavily doped polysilicon as the metal gate. The doping concentration of polysilicon plays a significant role on the capacitance-voltage (CV) characteristics of the device. The interesting advantage of using heavily doped polysilicon is that different work functions $\phi_m$ of the gate electrode can be achieved by merely changing the doping level [TN98] [SN10]. This in turn will shift the CV characteristics and with the right choice of gate type and doping level the silicon surface can be varied from accumulation to inversion [SN10].

### 2.2.5 Metal-Oxide-Semiconductor Field-Effect Transistors

The introduction of the fundamentals on MOS capacitors serves an additional purpose, i.e., a smooth transition into the MOS field-effect transistor concept. The device operation is based on the modulation of a channel conductivity between two ohmic contacts, namely the source and the drain. The channel is formed under a metal-oxide gate with geometrical dimensions $W$ (channel width) and $L$ (channel length), similarly to the presented MOS capacitor under the inversion condition. Its conductance is controlled capacitively through the modulation of the charge density under the oxide by applying a potential to the metal gate (this forms a vertical electrical field). Moreover, the substrate of the device is usually held at a constant potential $V_B$. The potential difference between the source and substrate can also modulate the channel conductance (sometimes referred to as back-gate-effect or body-effect). Carrier flow is additionally controlled by the application of a potential difference between the drain and source regions (i.e., this forms a horizontal electrical field). In case of electron flow in the channel the device is an n-type MOSFET (heavily doped $n+$ drain and source regions on a p-type substrate), while in case of holes flow the device is a p-type MOSFET (heavily doped $p+$ drain and source regions on an n-type substrate). It is interesting to note that the metal gate electrode is replaced by a heavily doped polysilicon electrode in today's CMOS technologies.

In the following paragraphs and chapters the source contact will be treated as the voltage reference and the discussion in this subsection will be limited to n-type MOSFETs. Extending the following to p-type MOSFETs requires usage of the corresponding parameters and reversal of the polarity of the applied voltages. Let us recall the inversion condition in the MOS structure. The gate voltage required for that comprises of the needed flatband voltage and the voltages across the semiconductor oxide and the semiconductor surface. Moreover, in real MOS devices the region under the gate (channel region) is also implanted by additional impurities. That way and according to the implantation type (n- or p-type dopants) the gate voltage needs either to be further increased in order to invert the channel region or a lower gate voltage will be sufficient for the inversion. The gate voltage needed for a strong inversion is called

threshold voltage $V_T$ and is given by:

$$V_T = V_{FB} + \psi_S - \frac{Q_{depl}}{C_{OX}} + \frac{Q_{impl}}{C_{OX}} = V_{FB} + 2\psi_B + \frac{Q_{impl} + \sqrt{2q\epsilon_s N_A(2\psi_B - V_{BS})}}{C_{OX}} \quad (2.2.35)$$

where $\epsilon_s$ the permittivity of silicon, $N_A$ the acceptors impurity concentration, $Q_{depl}$ is the bulk depletion charge density, $Q_{impl}$ is the charge density due to the implantation, $V_{BS}$ is the substrate (or bulk) potential referred to source and the surface potential $\psi_S \cong 2\psi_B$ for the onset of inversion. Note that $C_{OX}$ is the gate oxide capacitance per unit area. Equation (2.2.35) clearly shows the threshold voltage dependence from the bulk-source voltage $V_{BS}$ and $V_T$ can be rewritten including the body-effect coefficient $\gamma$ as:

$$V_T(V_{BS}) = V_T(V_{BS} = 0) + \gamma\left(\sqrt{2\psi_B - V_{BS}} - \sqrt{2\psi_B}\right) \quad (2.2.36)$$

By adjusting the implantation in the channel region and thus the charge density $Q_{impl}$, the threshold voltage of the device can be precisely set. Devices featuring a positive threshold voltage are referred as enhancement n-type MOSFETs, while devices with a negative threshold voltage are called depletion n-type MOSFETs. Reversing the polarity of the threshold voltage, this categorization is valid for p-type MOSFETs as well.

For long channel length n-type devices, using the gradual channel approximation [PS66] [TN98] and simplifying further with the use of the charge-sheet approximation [Bre78] [TN98] the basic expressions of the drain-source current can be derived in the diverse regions of operation of a MOSFET. For short channel devices the Schichmann-Hodges model [SH68] is adopted. Depending on the applied gate and drain voltages, there exist three main regions of operation, namely the subthreshold, the linear (or resistive) and the saturation region. Table 2.3 shows the basic equations governing the latter two regions of operation. The subthreshold region is also of great importance, providing information of how sharp the drain-source current drops with the gate bias. In this region of operation the semiconductor surface is in either weak inversion or depletion, thus the dominating component of the drain-source current is the diffusion component. Following an analysis presented in [SN10] the drain-source current can be found to depend exponentially on the applied gate voltage, as expected for a diffusion dominated current transport [TN98]. This exponential behaviour can be described by

defining the subthreshold slope $S$:

$$S = \left(\frac{d(\log_{10} I_D)}{dV_G}\right)^{-1} = \ln 10 \frac{kT}{q}\left(1 + \frac{C_D + C_{it}}{C_{OX}}\right) \tag{2.2.37}$$

where $C_{it}= q^2 D_{it}$ the associated capacitance to a potentially high interface-trap density $D_{it}$.

The classification of the models in two categories respective to the channel length of MOSFETs stems from the fact, that with the ever decreasing transistor dimensions important effects arise, which impose modifications on the existing mathematical models. MOSFETs featuring channel lengths less than 1-2 µm are considered to be short-channel MOSFETs and the classical square-law model fails to describe their voltage-current (I-V) transfer characteristics. The most significant effects, often named short-channel effects, are velocity saturation, channel length modulation, drain-induced barrier lowering (DIBL), breakdown and the significance of the drain-source series resistance [TN98]. In a short-channel MOSFET and especially in the linear regime is the latter effect of great importance. The drain/source resistance may be an appreciable fraction of the channel resistance and thus not negligible as in long-channel devices. Therefore, a voltage drop across the drain and source regions can lead to a significant current degradation [TN98]. Using the channel-resistance method [CCMG80] the drain/source parasitic resistance $R_{SD}$ can be extracted (employed in this work as well).

For simplifying calculations in analog circuits employing MOS transistors small signal models are used for linearization of the non-linear equation of the transistor shown in table 2.3. Therefore, small signal parameters such as the gate transconductance $g_m$, the output conductance $g_{ds}$ and the body or back-gate transconductance $g_{mb}$ are defined in the saturation region as follows:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.2.38}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{2\psi_B - V_{BS}}} g_m = \chi_b \cdot g_m \tag{2.2.39}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \tag{2.2.40}$$

where $\chi_b$ is the ratio of body- to gate-transconductance of a MOSFET.

The last part of this section is dedicated to MOSFET drain-current noise and its modeling. There are two main noise components present in MOS transistors a) the channel thermal noise $S_{I_D,th}$ and b) the low frequency $1/f$ noise $S_{I_D,1/f}$. The former arises due to the thermal motion of carriers in the channel and depends on the region of operation of the transistor. In the linear region of operation $S_{I_D,th}$ is given by equation (2.2.41), while in the saturation region by equation (2.2.42) [Tsi99]:

$$S_{I_D,th}|_{lin} = 4kTg_m \tag{2.2.41}$$

$$S_{I_D,th}|_{sat} = \frac{4}{3}kTg_m \tag{2.2.42}$$

where $g_m$ the gate transconductance and $k$ the Boltzmann constant. The latter noise component, has several origins and different models exist in literature describing this frequency dependent noise. The three most accepted models are a) the mobility fluctuation model or Hooge's model [Hoo76], b) the carrier number fluctuation model or Mc-Worther's model [McW55] and c) the unified $1/f$ noise model [HKHC90]. There is no universally accepted model on the $1/f$ noise theory, but the most widely accepted is the unified model combining both mobility $\mu$ and number of carriers $N$ fluctuation. The low frequency $1/f$ noise $S_{I_D,1/f}$ is given by:

$$S_{I_D,1/f} = \frac{kT(1 + \mu S \cdot N)^2 n_t\left(E_{F,n}\right)}{\gamma_{1/f} W L N^2} \frac{{I_D}^2}{f^{\alpha}} \tag{2.2.43}$$

where $k$ the Boltzmann constant, $I_D$ the drain-source current, $W$ and $L$ the transistor's gate width and length respectively, $\alpha$ the frequency exponent, $S$ a scattering coefficient, $\mu$ the carrier mobility, $N$ the number of carriers per unit area, $E_{F,n}$ the quasi Fermi energy level, $n_t(E_{F,n})$ the trap distribution over space at the quasi Fermi level, $\gamma_{1/f}$ the attenuation coefficient of the electron wave function and $\alpha$ the noise exponent on the frequency.

***Table 2.3: n-type MOSFET characteristics.*** *Cross sections are not drawn in scale. $E_c$ is the critical electrical field at the onset of carrier velocity saturation in the short channel transistor, where the carrier velocity is a factor of 2 less than the low-field formula would predict* [GHLM01].

| | | Region of operation and equations | IV-Characteristics | Cross section |
|---|---|---|---|---|
| Long-channel nMOSFET | triode | $I_D = k\frac{W}{L}\left( (V_{GS} - V_T)\, V_{DS} - \frac{V_{DS}^2}{2}\right)$<br>$V_{GS} > V_T$<br>$V_{DS} < V_{GS} - V_T$ | | |
| | saturation | $I_D = \frac{k}{2}\frac{W}{L}(V_{GS} - V_T)^2 \cdot \left(1 + \frac{V_{DS}}{\lvert V_A \rvert}\right)$<br>$V_{GS} > V_T$<br>$V_{DS} \geq V_{GS} - V_T$ | | |
| Short-channel nMOSFET | triode | $V_T < V_{DS,sat}$ | | |
| | saturation | $I_D = \left(\frac{1}{1+\frac{V_{GS}-V_T}{E_c L}}\right) \frac{k}{2}\frac{W}{L}(V_{GS} - V_T)^2 \cdot \left(1 + \frac{V_{DS}}{\lvert V_A \rvert}\right)$<br>$\lambda = -\frac{1}{V_A}$ with $V_A < 0$<br>$V_{DS} \geq V_{DS,sat}$ | | |

## 2.3 CMOS Image Sensors

Next to charge coupled detectors, image sensors fabricated on CMOS technology were introduced in the 1990s, with the main advantage of integrating into or around the photoactive array one or more MOS transistors for amplification, addressing or image processing purposes. CMOS image sensors have been extensively studied the last twenty years and remain today under continuous development. Nowadays, the image sensor market is shared among CISs and CCDs, which had dominated the field of imaging sensors for a long time [Oht08]. This section is dedicated on a brief overview of the fundamental characteristics and architecture of CMOS image sensors. The diverse pixel structures will be introduced and the peripheral electronics needed to read out the photoactive array will be presented.

### 2.3.1 System Architecture

The fundamental parts forming a CMOS image sensor are a) an one- or two-dimensional active or passive imaging array of photoactive picture elements (pixels), where the charge-to-voltage conversion occurs, b) the digital electronics for the x-y addressing of the array and c) the analog or mixed signal column electronics employed to drive the addressed analog value to the d) output circuitry, which forms the last fundamental system component. Starting from the imaging array, its performance is very critical since it affects significantly the overall image quality. Every pixel of any CIS features a photodetector and transistors belonging to the addressing circuitry. While passive pixel sensors (PPSs) incorporate only the latter two devices, active pixel sensors (APSs) feature additional active in-pixel circuitry for buffering the voltage signal to the column electronics, as depicted in figure 2.10. The digital row addressing circuit (vertical access circuitry) is an one-dimensional array of decoders and/or shift registers used to select the row of pixels to be connected to the column bus and fed parallely into the column circuitry. The column electronics or sometimes referred to as column readout electronics include typically a sample and hold (S/H) circuit, an analog buffer and low-frequency noise canceling circuits employing the CDS technique, which will be treated in subsection 2.3.3. Another column addressing circuit (horizontal access circuitry) serially shifts the output of the selected column bus to the output circuitry. The output circuitry consists typically of a high-speed buffer able to drive the relatively

large output pad parasitic capacitance. The described parallel to serial multiplexing technique is repeated for the entire matrix, generating an output video stream.

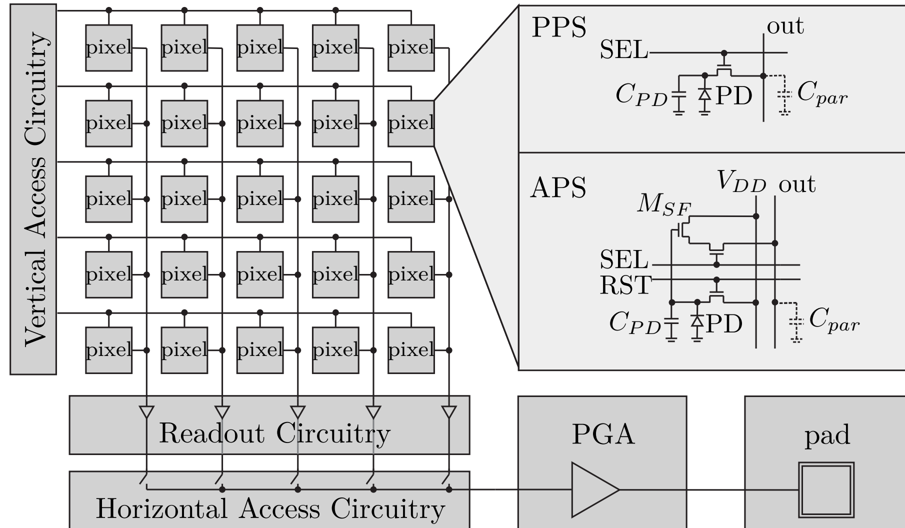


***Figure 2.10: CMOS image sensor architecture containing a two-dimensional imaging array.*** *The three main parts forming a CIS are shown. A programmable gain amplifier (PGA) is used here to drive the output chip pad. In a PPS architecture only passive components and a SEL switch for row addressing are included in the pixel. On the contrary, in an APS design an amplifying transistor $M_{SF}$ in a source follower configuration is additionally incorporated.*

The described architecture only covers the basic components of a CMOS image sensor. This architecture can be enhanced with a plethora of mixed signal circuits offered by using CMOS technology. Examples include on-chip global ADC or even massively parallel column ADC circuits [SMKT07] for the output digitization. Algorithms for enhancing the image quality, dynamic range or frame acquisition speed such as multiple sampling [CXMT12], multiple exposures [SMKT07], binning [KKK+12], pipelining and region-of-interest (ROI) readout [SHF+02] techniques can be implemented. Timing and control circuits implementing global and/or rolling shutter readout techniques are common blocks of today's CMOS image sensors. Moreover, chips featuring image processing cores such as compression, feature extraction [CPCY13] or pattern recognition [ZFW11] circuitry have already been demonstrated and are referred to as vision chips. In- [ASBSH98] or off-pixel [THK+13] memory as well as communication interfaces [KT06] can be part of a CIS.

### 2.3.2 Photodiode and Pixel Considerations

In this subsection a closer look is taken at the heart of every CIS, namely the pixel matrix. Basic APS design families are presented and compared, leaving their older counterpart (PPS architecture) outside of the scope of this work. In order to allow a simple and quick way of describing the pixel structure, a shorthand notation enumerating the number of transistors within each pixel is used. For example a 4T pixel design refers to a pixel structure with four in-pixel transistors. However, as we be shown later in the section not all of the enumerated transistors are true transistors, since transfer gates are also enumerated. This shows the apparent confusion caused by such a nomenclature. Alternatively, the pixel classification can be performed based on the employed photodetector [Oht08]. In this subsection pixel families based on photodiodes will be presented.

The simplest and widely employed APS pixel design family is the 3T-APS illustrated in figure 2.11a). Here, the three transistors are a reset transistor $M_{rst}$ for resetting the photodetector after each integration period, the row select transistor $M_{sel}$, which belongs to the addressing circuitry and connects the pixel output to the column bus, and a transistor $M_{SF}$ in a source-follower configuration. The 3T pixel family can be implemented with different photodetectors available in a CMOS process. Next to the standard p-n junction based photodiodes with either a highly doped shallow n+ region or with a deeper n-type well (n-well) on the epitaxial p-type substrate (p-epi), pinned photodiodes (PPDs) are available in many commercial CMOS processes, as shown in 2.11b). The advantage of using the shallow p+ pinning implantation on top of the n-type region in PPDs, is that the peak of the electrostatic potential is shifted away from the surface, separating that way the potential well (or accumulation region) from the semiconductor/oxide interface, as depicted in figure 2.11. This separation provides significantly lower dark current (and thus lower dark noise) as well as higher quantum efficiency for shorter wavelengths, since the potential well is further away from the high interface-trap density of the surface. In addition to that, the p+ layer ensures the full depletion of the n-region. Moreover, CMOS processes offering extra p-type wells (p-well) allow formation of p-n junction based photodiodes between either the n+ or the n-well implantation and the extra p-well. Moreover, the capacitance of the photodiode is increased due to the presence of two p-n junctions.

The operation of the 3T pixel family is based on three steps. First the photodetector is reset through $M_{rst}$ at a voltage level $V_{rst}$. Then, $M_{rst}$ is turned off and the integration

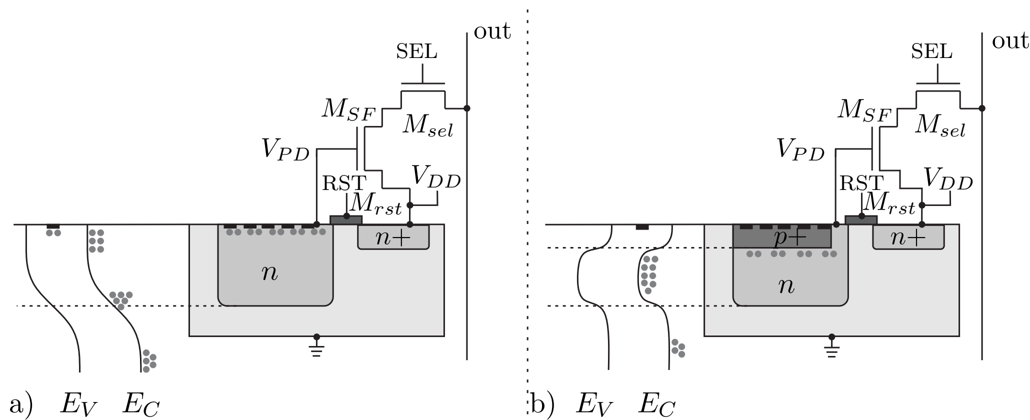


***Figure 2.11: 3T active pixel sensor design.*** *The energy band diagrams of the photodetector are depicted next to its cross section. Interface-trap energy levels are denoted with black squares. a) p-n junction based photodiode b) pinned photodiode. Note how the maximum electrostatic potential is away from the surface in the case of a PPD and how the accumulation well is separated from the surface traps.*

time starts, while the photogenerated carriers are accumulated in the integration node capacitance $C_{pix}$, formed from the parallel combination of the photodetector capacitance $C_{PD}$ and the gate-source capacitance $C_{GS}$ of the source follower (SF) $M_{SF}$. The voltage level on the integration node capacitance drops during the integration time. The voltage change, when one charge has been accumulated in the photodetector, is called conversion gain (CG) and equals $q/C_{pix}$. After a defined integration time, the transistor $M_{sel}$ is turned on and the pixel voltage level of the photodetector is fed to the column bus. Finally $M_{sel}$ is turned off and the entire process is repeated for the following line. The pixel integration node capacitance is typically large in 3T pixel designs leading to increased thermal kTC noise generated in the reset transistor [HL11]. Low-frequency noise canceling techniques such as CDS cannot only reduce the $1/f$ but also reduce the kTC noise, but the kTC noise reduction is difficult to implement on a 3T pixel design. Furthermore, a global concurrent integration period on every row (global shutter or snapshot technique) is not possible using the the 3T pixel family, since the integration node and the readout node are shared. Thus, only the rolling shutter technique can be implemented, where every row is reset, illuminated and read out, before continuing to the next row.

The issues encountered in the previous design, can be partially alleviated by adding a fourth transistor in the pixel. In this paragraph the 4T-APS family is addressed, where the photoactive and the integration node are separated, as illustrated in figure 2.12. In this pixel structure, the added transfer gate (TG) (note that this is not a true

transistor) allows the transferring of the accumulated charges in the photodetector (PPD) to the charge-voltage conversion site, namely the floating diffusion (FD). The operation of pixel is based on the fact that charges accumulate during integration time in the photodetector, keeping the transfer gate open. After a predefined integration time, the FD is reset, the TG is closed and the accumulated charges are converted into voltage on the FD capacitance. The readout of this signal through the column electronics takes places after $M_{sel}$ is turned on, that way allowing $M_{SF}$ to drive the column bus. Separating the photoactive from the readout node helps gaining the most out of the application of the CDS technique, as it will be illustrated in the next subsection. However, this pixel design has also its disadvantages mainly due to the difficulty of the PPD fabrication itself to achieve a complete transfer from the photodetector to the FD. An incomplete transfer may cause image lag [Oht08]. Next to that, noise levels are lower that the 3T pixel family in expense of an increased fill factor (FF), which is the ratio of the photoactive to the entire pixel area.

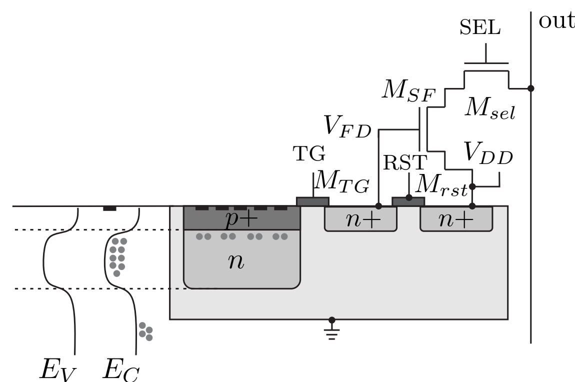


***Figure 2.12: 4T active pixel sensor design.*** *Note the extra transistor used $M_{TG}$. In reality it is a transfer gate (TG) connecting the photoactive element (PPD) with the floating diffusion, where the charge-voltage conversion takes place.*

Adding more transistors within the pixel area, will often lead to enhanced functionality employing extra features without always improving pixel performance. By simply adding another transistor serving as a reset transistor of the PPD, the 5T design family has arisen. Many pixel designs also share some of the transistors, giving rise to families such 1.25T APS or 1.5T APS, which are beyond the scope of this work.

### 2.3.3 Readout Electronics Overview

In this subsection the fundamental readout electronics typically encountered in a CIS are discussed. Namely, the reset transistor $M_{rst}$ used and its implications, the in-pixel amplification transistor $M_{SF}$ and its biasing, the CDS technique circuit implementation, as well as the employed ADC circuits. Next to the mentioned analog/mixed-signal circuits, the essential digital circuitry operating a CIS will be introduced.

As depicted in figures 2.11 and 2.12 the reset operation of either the photodiode or the FD is performed through a MOSFET $M_{rst}$. Usually, an nMOSFET is used to set the reset voltage at the node, a technique called soft reset. The gate of the nMOSFET is set to the highest potential of the circuit $V_{DD}$ and due to the threshold drop needed to keep the transistor conducting, the maximum reset voltage on the node is $V_{DD} - V_T$. Therefore, the transistor operates at the end of the reset procedure very close to the subthreshold region, reaching slowly the voltage $V_{DD} - V_T$ (explaining where the name "soft" comes from), thus from the one reducing kTC noise while from the other causing image lag. To address this issue, two in- and two off-pixel solutions have been proposed. The first is the use of an in-pixel pMOSFET, which however requires more area, reducing the pixel FF. The second in-pixel solution is the hard reset technique, where the gate voltage applied to the nMOSFET is set to $V_{DD} + V_T$, so that the reset procedure finishes quickly [Oht08], or by driving the gate with $V_{DD}$ but setting the drain voltage of $M_{rst}$ at a sufficiently lower voltage than $V_{DD}$, thus decreasing the saturation level of the photodetector. Both techniques however increase the kTC noise. The first off-pixel technique, is the flush reset [PYC+03] technique, combining the advantages of the previous two techniques, in expense of adding extra control circuits on the column electronics. Finally the active reset technique, stabilizing the reset node voltage utilizing active capacitive feedback and bandlimiting through the column electronics, is able to drastically reduce kTC noise.

In all previously presented APS pixel families, the voltage stored at the integration node is read out by a simple transistor in a source follower configuration. Assuming an ideal tail current source setting the current through $M_{SF}$ the small signal voltage gain $A_{SF}$ of the SF is given by:

$$A_{SF} = \frac{g_m}{g_m + g_{mb} + g_{ds}} \tag{2.3.1}$$

where $g_{ds}$ is the output conductance of the amplifying transistor, $g_m$ and $g_{mb}$ the transistor gate transconductance and body transconductance, respectively. The in-pixel SF affects not only the noise figure of the entire pixel (1/f or random telegraph signal (RTS) noise due to the surface-lying channel), but also its linearity since the SF DC response is not linear over the entire operation region. When the voltage level of the integration node drops close to the threshold voltage, $M_{SF}$ starts operating in moderate or weak inversion. Moreover, its voltage gain as equation (2.3.1) dictates, is less than unity. A solution against this non-linearity over the input range is to use a depletion MOSFET exhibiting negative threshold voltages, sometimes though at the expense of increasing noise levels. To address both issues originating from the standard SF, a buried channel SF was proposed in [WSR+08], which exhibited both reduced noise as well as negative threshold voltage (thus improving the output swing) compared to a standard surface SF.

As was earlier underlined, thermal noise is generated in the in-pixel reset transistor while charging the integration node after an illumination period. This noise, referred to as kTC noise, can be eliminated using the widely adopted correlated double sampling technique. The fundamental assumption behind this technique is that both the signal level after illumination and the reset level show the same voltage fluctuation or in other words the signal and reset levels are correlated in terms of both having the same fluctuation at the readout node [HL11]. Figure 2.13 shows two possible implementations of the CDS technique in the analog domain. In a) two S/H circuits are used to store

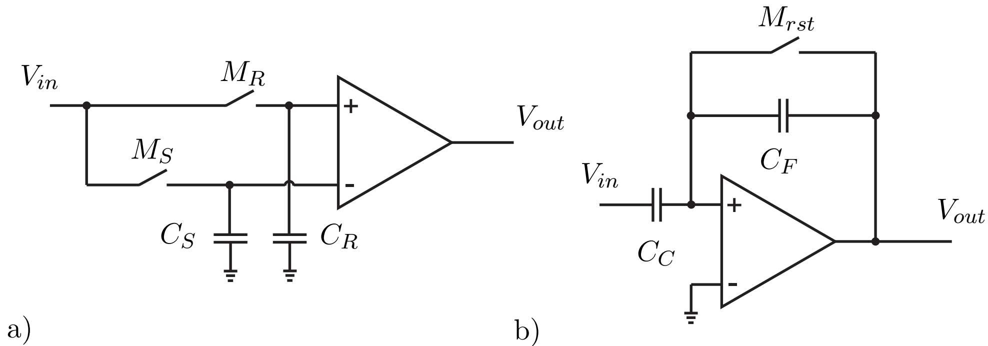


***Figure 2.13: Circuit implementation of correlated doubled sampling (CDS).*** *The implementation on the left a) is based on two S/H circuits feeding a differential amplifier, while the one on the right b) is based on an SC amplifier. In reality all switches are implemented using MOSFETs.*

the signal and reset value, which consequently will be subtracted at the differential amplifier. In b) the implementation utilizes a switched-capacitor (SC) circuit, where

the switches have to be activated in the following way. During the reset phase the pixel output will be stored in capacitor $C_C$ keeping the feedback switch closed. With the start of the integration period the feedback switch is opened and the signal level is continuously subtracted from the previously stored value at the capacitor $C_C$ with the help of the negative feedback over $C_F$. The CDS technique allows both a kTC noise reduction as well as a reducing low frequency 1/f noise of the in-pixel SF. All these however at the cost of increasing the thermal white noise power [FHB+03]. The CDS technique can be applied in the column level, chip level or even in-pixel level. The latter affects the pixel FF drastically, while the column level CDS exhibits high column fixed pattern noise (FPN), which represent the regular spatially fixed variations of the output signal originating from the mismatch among devices of every column and offset and gain variations among the column circuits. The latter issue can be resolved through either a technique called delta-difference sampling or double-delta sampling (DDS) following the CDS technique [MKG+97]. Another proposed way is the use of column ADC circuits as described in [STMH06] and [FKIN05].

On-chip analog to digital converters are in some applications such as high-frame rate readout a mandatory choice. Depending on the pixel count and on the desired frame rate of the CIS the ADC circuitry can be implemented either on-chip- or on-column-level (column shared [LCC+11] or massively parallel [CCL+11] [KBT+03] architectures). However, pixel level ADC designs have also been reported [YFG98] [RJ03]. All existing ADC architectures have been integrated on CMOS image sensors and reported in literature, such as flash [JLY13], successive approximation register (SAR) [DTM+13], cyclic [LCC+11], single slope [TCWB13] and $\Delta\Sigma$ [CCL+11] analog-digital (A/D) converters.

Next to the presented analog/mixed-signal circuitry encountered in a CIS, digital circuitry has to be implemented around the sensor serving two reasons. First, for the implementation of the row and column addressing circuits of the matrix and second for any digital processing after the frame acquisition and digitization. Communication interfaces do also fall in the latter category. For the row-column (or x-y) addressing either shift registers with parallel set-reset function or decoders in conjunction with multiplexers and control circuitry are mainly used. For a deeper understanding of the digital circuitry or for their technical realization it is useful to consult either a textbook [WH10] or the work in [Kle12], where the circuitry implemented for the CMOS image sensor developed within the framework of this thesis are described in detail.

## 2.4 Synopsis

In this chapter, the fundamental background supporting this work has been presented. Principles of elasticity theory have been put forward and the stress-strain relation has been introduced, since these notions are broadly used in the following chapters. The application of mechanical stress on ultra-thin silicon membranes alters the energy band structure of silicon, thus the fundamentals of semiconductors physics with emphasis on silicon have been presented. Following the basics of crystals and their band structure, the carrier concentrations for each energy band have been derived. Due to the fact that p-n junction based photodiodes are the heart of the developed flexible image sensor in this work, both the p-n junction theory as well as the fundamentals of photo transduction deploying silicon based photodiodes have been introduced. Moreover, since MOS transistors are one of the the basic building blocks in the developed system, the MOSFET principle of operation, its modeling as well as the effects encountered in today's short channel transistors have been described. The last section of the chapter is dedicated to a brief but comprehensive review of CMOS image sensors, covering the system architecture, the photosensing elements and their integration in diverse pixel designs and the on-chip readout electronics.

# Chapter 3 - Modeling Strain-Induced Effects on Devices and Circuits

In the following sections the strain-induced effects on the band structure of silicon will be modeled. Towards this goal the deformation potential theory is discussed and the energy band shifts are calculated (section 3.1). The former mathematical description of the strain-induced changes of the band structure will be used together with the changes of the energy band curvatures (i.e., the effective mass change) to quantify the effects on the carrier concentrations in each conduction and valence band. Next, this result will be used in section 3.2 to describe changes in the I-V characteristics of reversed biased p-n junction based photodiodes and MOS capacitors. In the following, the piezoresistance theory on MOSFETs will be briefly presented in section 3.4 and employed toward the modeling of analog circuits under mechanical stress. Both basic analog circuit configurations such as a source follower or a current mirror as well as elaborate analog circuits deployed in CIS readout electronics will be discussed and analyzed under the application of mechanical stress in sections 3.5 and 3.6 respectively. Section 3.7 summarizes and closes this chapter. The presented results and models are published by the author in [DHG12], [DHG13] and [DHM+13].

## 3.1 Band Structure of Strained Silicon

As mentioned in section 2.2.1 the reciprocal lattice of silicon, where the band structure is constructed, is a bcc lattice. Cubic crystals (together with hexagonal) possess the highest symmetry of all crystal systems. In addition, the band structure has to have the same symmetry as the lattice itself. Hence, it is logical to anticipate, that changing the symmetry properties of a crystal will lead to alterations of its band structure. There are two main symmetry systems in a crystal, namely the point and the translational symmetry. For a thorough understanding of symmetry systems and operations it is advisable to refer to textbooks such as [Jur74], [BP74] or [STN07]. As an example, neglecting spin-orbit interaction, at the $\Gamma$ point of the reciprocal lattice the band structure has to follow the same point symmetry as the cubic crystal, which imposes a three-fold degeneracy of the valence bands at this point (which is not the case for non-cubic semiconductors). Including spin-orbit interaction, the special rotational symmetry of spin has to be taken into account [STN07], which results into a doubly degenerate valence band at $\Gamma$ and one split-off band as discussed in section 2.2.1. Similarly, due to the cubic symmetry and the six-fold degeneracy of the $\Delta$ axis in the Brillouin zone (refer to table 2.1) the energies at all equivalent points on this

axes must be the same. Therefore, the conduction bands of silicon, which are located along the $\Delta$-axes have to be degenerate. This degeneracy is called star degeneracy, since it takes place in different $k$ points, which can be transformed the one into the other employing symmetry operations.

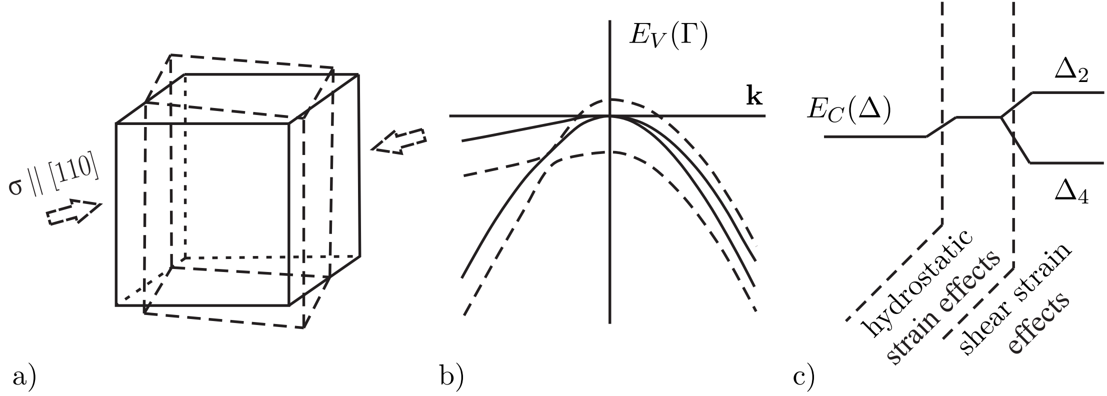


***Figure 3.1: Deformation of a cubic crystal under mechanical stress and the strain-induced band shifting.*** *a) Cubic crystal deformation under the application of* [110] *uniaxial stress. Note how the cubic symmetry is lowered to orthorhombic by the shear strain-induced change of the upper and lower planes into rhombuses. (After* [STN07]*). b) Silicon's valence band degeneracy lifting under* [110] *uniaxial compressive stress. c) Silicon's conduction band star degeneracy lifting under* [110] *uniaxial compressive stress.*

The application of mechanical stress on a crystal in the general case will deform it and lower its symmetry. Lowering its symmetry, as made clear after the latter observations, will alter the semiconductor's band structure. Under the special case of hydrostatic stress, the symmetry of a cubic crystal will not be altered, and hence all observations about the band degeneracies still hold. However, when looking at the distance between the valence and conduction band (i.e., the bandgap), a bandgap shift is observed. This can be explained by the simple observation, that hydrostatic stress will not change the shape of the cubic crystal, but it will change the interatomic distance. Compressive stress will lower this distance, thus leading to an increased interatomic interaction and hence to an increased bandgap. On the contrary, tensile stress will increase the interatomic distance and hence lead to a decreased bandgap. A general mechanical stress will however also induce shear strain, for example the application of uniaxial stress across the [110] direction. Shear stress will reduce the symmetry of the crystal from cubic into orthorhombic symmetry [STN07]. Due to the symmetry reduction, the degeneracies discussed above, are fully or partially lifted, as illustrated in

figure 3.1. This will be treated mathematically in the following subsections. Emphasis is given on the application of uniaxial stress across the [110] direction, because this stress has been applied during the experimental procedures of this work, since modern CMOS manufacturing processes use typically (100) wafers inscribing the devices along the [110] or $\left[\bar{1}10\right]$ directions. In the Appendix both the strain tensor in the case of [110] uniaxial stress, as well as the reduced Voigt notation used throughout this chapter are presented.

### 3.1.1 Strain-Induced Conduction Band Shift

The conduction band shift caused by strain will be treated by means of the deformation potential theory. Deformation potentials are constants relating the strain to the band energy shifts. This theory was introduced by Bardeen and Schockley [BS50] extending the effective mass approximation method in order to study the interaction of electrons and acoustic modes of vibrations (phonons). The same method was also used by Bir and Pikus [BP74] while studying the energy bands of strained materials. Basically, the energy shift $\Delta E_C$ can expressed by:

$$\Delta E_C = \sum_{ij} \Xi_{ij} \varepsilon_{ij} \tag{3.1.1}$$

where $\Xi_{ij}$ and $\varepsilon_{ij}$ the elements of the deformation potential and the strain tensor $\bar{\bar{\varepsilon}}$, respectively. Using the same notation as in the previous chapter, the energy shift $\Delta E_C^i$ of valley $i$ (along the $\Delta$ and $\Lambda$ axes) for a homogeneous deformation described by a strain tensor $\bar{\bar{\varepsilon}}$ can be expressed as

$$\Delta E_C^i = \Xi_d^i Tr(\bar{\bar{\varepsilon}}) + \Xi_u^i \mathbf{a}_i^T \bar{\bar{\varepsilon}} \mathbf{a}_i \tag{3.1.2}$$

where $Tr(\bar{\bar{\varepsilon}})$ is the trace of the strain tensor $\bar{\bar{\varepsilon}}$ and $\mathbf{a}_i$ is a unit vector parallel to the $\boldsymbol{k}$ vector of valley $i$. $\Xi_d^i$ and $\Xi_u^i$ are the dilation and uniaxial deformation potentials at the conduction band edges of the $i$ valley respectively. The deformation potential constants can be derived using theoretical methods such as local density functional theory and ab-initio pseudopotentials [VdW89] or the non-local empirical pseudopotential method [FL96]. Starting from equation (3.1.2) the energy shifts can be expressed with respect

to an average value $\Delta E^i_{C,av}$.

$$\Delta E^i_{C,av} = \left(\Xi^i_d + \frac{1}{3}\Xi^i_u\right) Tr(\bar{\bar{\varepsilon}}) \tag{3.1.3}$$

$$\Delta E^{001}_C = \Delta E^{\Delta}_{C,av} + \frac{2}{3}\Xi^{\Delta}_u\left(\varepsilon_{zz} - \varepsilon_{xx}\right),\ \Delta E^{100,010}_C = \Delta E^{\Delta}_{C,av} - \frac{1}{3}\Xi^{\Delta}_u\left(\varepsilon_{zz} - \varepsilon_{xx}\right) \tag{3.1.4}$$

$$\Delta E^{111,11\bar{1}}_C = \Delta E^{\Lambda}_{C,av} + \frac{2}{3}\Xi^{L}_u\varepsilon_{xy},\ \Delta E^{\bar{1}11,1\bar{1}1}_C = \Delta E^{\Lambda}_{C,av} - \frac{2}{3}\Xi^{L}_u\varepsilon_{xy} \tag{3.1.5}$$

For the special case of [110] uniaxial mechanical stress which is of particular importance in this work, the strain induced shifts of the $\Delta$ and $\Lambda$ conduction band valleys are calculated and listed in table 3.1. Recalling the stress-strain relation described by equation (2.1.9), the strain $\varepsilon_{ij}$ is in linear dependence with the mechanical stress $\sigma_{ij}$. The exact strain tensor representation for an applied [110] uniaxial mechanical stress $\sigma$ is given in the Appendix.

### 3.1.2 Strain-Induced Conduction Band Degeneracy Lifting

Looking at the X point of the silicon energy band structure illustrated in figure 2.4, it can be observed that the lowest two conduction bands labeled $\Delta_1$ and $\Delta_{2'}$ are degenerate at this point. This effect arises from the fact that silicon has a diamond cubic crystal structure, which shows a special symmetry having three glide reflection planes. However, if the crystal is stressed along the [110] direction a shear strain component is present in the tensor, which lifts this degeneracy (the strained lattice belongs to an orthorhombic crystal system). Hence, shear strain $\varepsilon_{xy}$ lifts the degeneracy of the $\Delta_1$ and $\Delta_{2'}$ bands at the X point by creating a gap which has to be added to the conduction band shifts of the $\Delta_2$ valleys along the [001] direction [LPC71] presented in the previous subsection. The shear strain $\varepsilon_{xy}$ does not alter the $\Delta_4$ ([100] and [010] direction valleys) ellipsoids. It only deforms the $\Delta_2$ constant energy surfaces from prolate ellipsoids into scalene ellipsoids, which will affect the longitudinal and transversal effective masses as will be presented in the next subsections. The additional energy

***Table 3.1: Strain-induced shifts of the conduction band valleys along the $\boldsymbol{\Delta}$ and $\boldsymbol{\Lambda}$ axes under uniaxial [110] mechanical stress.*** *The coefficients $s_{11}^{(v)}$, $s_{12}^{(v)}$, $s_{44}^{(v)}$ are the elastic compliance coefficients of silicon and $\sigma$ the applied [110] uniaxial mechanical stress.*

| | Conduction band valley | Energy shift [eV] |
|---|---|---|
| $\Delta$ valleys | [001] | $\Delta E_C^{001} = \left(\Xi_d^{\Delta}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Delta} s_{12}^{(v)}\right)\sigma$ |
| | [100] | $\Delta E_C^{100} = \left(\Xi_d^{\Delta}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Delta}\left(\frac{s_{11}^{(v)} + s_{12}^{(v)}}{2}\right)\right)\sigma$ |
| | [010] | $\Delta E_C^{010} = \left(\Xi_d^{\Delta}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Delta}\left(\frac{s_{11}^{(v)} + s_{12}^{(v)}}{2}\right)\right)\sigma$ |
| $\Lambda$ valleys | [111] | $\Delta E_C^{111} = \left(\Xi_d^{\Lambda}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Lambda}\left(\frac{s_{11}^{(v)} + 2s_{12}^{(v)} + s_{44}^{(v)}}{3}\right)\right)\sigma$ |
| | $[11\bar{1}]$ | $\Delta E_C^{11\bar{1}} = \left(\Xi_d^{\Lambda}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Lambda}\left(\frac{s_{11}^{(v)} + 2s_{12}^{(v)} + s_{44}^{(v)}}{3}\right)\right)\sigma$ |
| | $[\bar{1}11]$ | $\Delta E_C^{\bar{1}11} = \left(\Xi_d^{\Lambda}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Lambda}\left(\frac{s_{11}^{(v)} + 2s_{12}^{(v)} - s_{44}^{(v)}}{3}\right)\right)\sigma$ |
| | $[1\bar{1}1]$ | $\Delta E_C^{1\bar{1}1} = \left(\Xi_d^{\Lambda}(s_{11}^{(v)} + 2s_{12}^{(v)}) + \Xi_u^{\Lambda}\left(\frac{s_{11}^{(v)} + 2s_{12}^{(v)} - s_{44}^{(v)}}{3}\right)\right)\sigma$ |

shift of the minimum $\Delta E_{shear}$ due to shear strain is given by:

$$\Delta E_{shear} = \begin{cases} -\frac{\Delta}{4}\eta^2, & |\eta| < 1 \\ -\frac{\Delta}{4}(2\,|\eta| - 1), & |\eta| > 1 \end{cases} \tag{3.1.6}$$

$$\eta = \frac{2\Xi_{u,sh}\varepsilon_{xy}}{\Delta} \tag{3.1.7}$$

where $\eta$ is a dimensionless strain, $\Delta$ equals 0.53 eV and $\Xi_{u,sh}$ is a higher order shear deformation potential. For the special case of [110] uniaxial mechanical stress can be written for $\eta$:

$$\eta = \frac{\Xi_{u,sh} s_{44}^{(v)} \sigma}{\Delta} \tag{3.1.8}$$

However, the presented nonlinear contribution on the conduction band shift is small in comparison with the energy shifts presented previously and thus can be ignored up to high strain levels [Sve11]. Readers interested in such higher order strain-induced effects are referred to [Sve11] and [STN07].

### 3.1.3 Strain-Induced Valence Band Splitting

The valence band degeneracy lifting and splitting induced by strain will be treated by means of the deformation potentials theory in conjunction with the $\boldsymbol{k} \cdot \boldsymbol{p}$ method [BP74]. In order to be able to calculate the valence band splitting analytically the spin-orbit interaction is neglected. Following Bir and Pikus [BP74] it can be written for the energy shift $\Delta E_V^i$ of the light hole (LH) and heavy hole (HH) valence bands:

$$\Delta E_V^i = aTr(\bar{\bar{\varepsilon}}) \pm \sqrt{E_\varepsilon} \tag{3.1.9}$$

$$E_\varepsilon = \frac{b^2}{2}\left[(\varepsilon_{xx}-\varepsilon_{yy})^2 + (\varepsilon_{xx}-\varepsilon_{zz})^2 + (\varepsilon_{yy}-\varepsilon_{zz})^2\right] + \frac{d^2}{4}(\varepsilon_{xy}^2 + \varepsilon_{xz}^2 + \varepsilon_{yz}^2) \tag{3.1.10}$$

where $a$, $b$, $d$ denote the deformation potentials at the valence band edges and the index $i \in \{lh, hh\}$ runs over the LH and HH bands, respectively.

For the special case of [110] uniaxial mechanical stress which is of particular importance in this work, the strain induced shifts of the LH and HH valence band valleys are calculated and listed in table 3.2.

***Table 3.2: Strain-induced shifts of the valence band LH and HH valleys under uniaxial* [110] *mechanical stress.*** *The coefficients $s_{11}^{(v)}$, $s_{12}^{(v)}$, $s_{44}^{(v)}$ are the elastic compliance coefficients of silicon and $\sigma$ the applied* [110] *uniaxial mechanical stress.*

| Valence band valley | Energy shift [eV] |
|---|---|
| LH | $\Delta E_V^{lh} = a(s_{11}^{(v)} + 2s_{12}^{(v)})\sigma + \frac{\sigma}{2}\sqrt{b^2(s_{11}^{(v)} - s_{12}^{(v)})^2 + \frac{d^2 {s_{44}^{(v)}}^2}{4}}$ |
| HH | $\Delta E_V^{hh} = a(s_{11}^{(v)} + 2s_{12}^{(v)})\sigma - \frac{\sigma}{2}\sqrt{b^2(s_{11}^{(v)} - s_{12}^{(v)})^2 + \frac{d^2 {s_{44}^{(v)}}^2}{4}}$ |

A more rigorous calculation of the valence band splitting taking into account the spin orbit interaction was performed by Manku and Nathan [MN93]. Due to its mathematical complexity the solution is not reproduced in this work. Here, it is worth to note that the valence bands, which resemble warped spheres in the unstrained lattice, get even more warped under [110] uniaxial stress, due to the lower crystal symmetry. Symmetry reduction induces coupling between the light and heavy hole bands (band mixing) which in turn warps the bands significantly. Readers interested in such higher order strain-induced effects are referred to [STN07].

### 3.1.4 Strain-Dependent Effective Mass Variations

The application of [110] uniaxial mechanical stress induces changes in the band structure of silicon, which have been modeled in the previous subsections. Assuming the parabolic band approximation and from band structure calculations the curvatures of the conduction energy bands also face changes under mechanical stress. This effect is attributed to the shear stress component of the [110] uniaxial mechanical stress. Applying [110] uniaxial stress lowers the $\Delta_2$ conduction valleys in energy, while inducing a warpage of their constant energy surfaces, leading to a change in the effective masses. The fourfold degenerate $\Delta_4$ valleys which are also shifted in energy do not face great change in their effective masses under the application of [110] uniaxial stress. The $\Delta_2$ constant energy surfaces deform from prolate ellipsoids into scalene ellipsoids as illustrated in figure 3.2b). Here, the transverse (in-plane) effective masses parallel $m^{\sigma}_{t,\parallel}$ and vertical $m^{\sigma}_{t,\perp}$ to the stress direction get mainly affected, exhibiting a linear dependence on the applied stress. The longitudinal (out-of-plane) effective masses $m^{\sigma}_{l}$ remain almost constant under stress under 1 GPa [UKSN05]. Hence, following the notation in [DUK+07] can be written:

$$m^{\sigma}_{t,\parallel} = m_t - \pi_{t,\parallel} \cdot \sigma \tag{3.1.11}$$

$$m^{\sigma}_{t,\perp} = m_t + \pi_{t,\perp} \cdot \sigma \tag{3.1.12}$$

$$m^{\sigma}_{l} = m_l + \pi_l \cdot \sigma^2 \tag{3.1.13}$$

where $m_t$ and $m_l$ the transverse and longitudinal effective mass under no stress, respectively, $m^{\sigma}_{t,\parallel}$, $m^{\sigma}_{t,\perp}$ the transversal (in-plane) effective masses under stress parallel

and vertical to the stress direction respectively, $m_l^\sigma$ the longitudinal (out-of-plane) effective mass under stress, $\sigma$ is the applied mechanical stress in Pa and $\pi_t$ and $\pi_l$ are the piezo-coefficients of the effective masses, which can be experimentally determined. Piezoresistive coefficients are in generally dependent on the doping level of the material, the crystallographic orientation and temperature. The symbols $\|$ and $\perp$ denote in-plane parallel and in-plane vertical directions with respect to the stress direction, respectively, while the superscript $\sigma$ denotes the existence of mechanical stress on the quantity. The density of states (DOS) effective mass for the conduction band can then be calculated as: $m_{C,DOS}^\sigma = (m_{t,\|}^\sigma m_{t,\perp}^\sigma m_l^\sigma)^{1/3}$ [SN10].

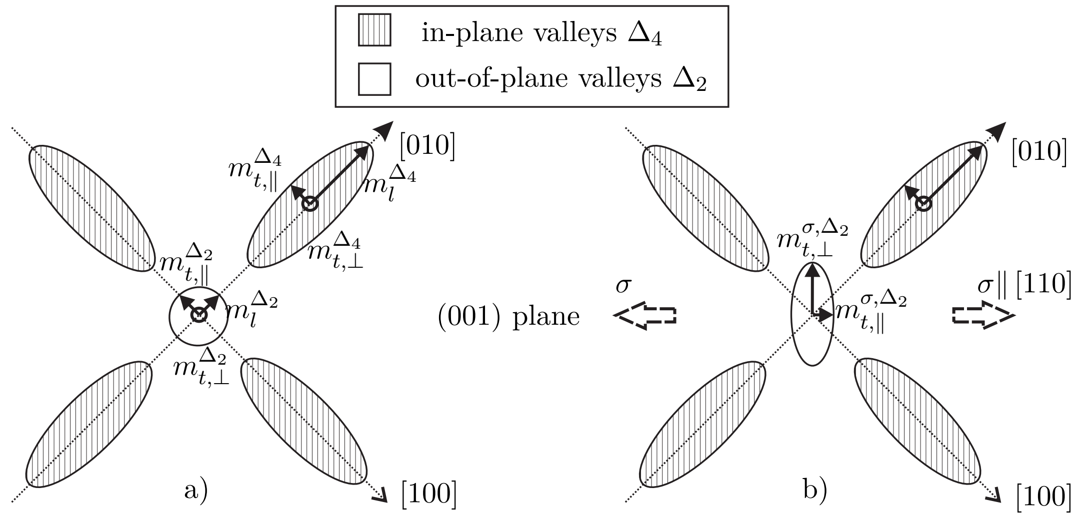


***Figure 3.2: Conduction band constant energy surfaces.*** *a) Relaxed condition. b) Under* [110] *uniaxial stress. Note how the prolate ellipsoids of the* $\Delta_2$ *valleys become scalene ellipsoids.*

Similarly, the valence band effective masses also face variations induced by the application of [110] uniaxial mechanical stress. Due to the more complicated nature of the valence bands (highly anisotropic and energy-dependent), variations of the DOS effective masses of the valence band have to be computed numerically by the help of a simulation program. It is found that mechanical stress narrows the gap between the DOS mass values between the heavy and light hole bands for a given energy [GM06]. Moreover, under high stress magnitudes the DOS effective masses of heavy and light hole bands become comparable [Mat04], as illustrated in figure 3.3.

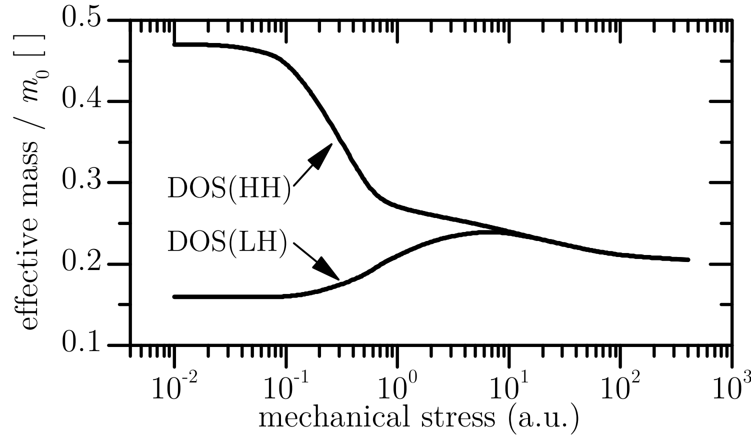


***Figure 3.3: Valence band DOS effective masses under* [110] *uniaxial mechanical stress.*** *Note how the DOS effective masses of heavy and light hole bands become comparable in the highly stressed region.(From* [Mat04]*).*

## 3.2 Strained p-n Junction Based Photodiode

The strain-induced effects on the band structure presented in the previous section, will be now used toward the modeling of the electrical and optical characteristics of a p-n junction based photodiode, which is the heart of a pixel in a modern CMOS image sensor. The discussion here will be limited on the types of photodiodes used throughout this work, which are n+/p and n-well/p photodiodes as shown in figure 3.4.

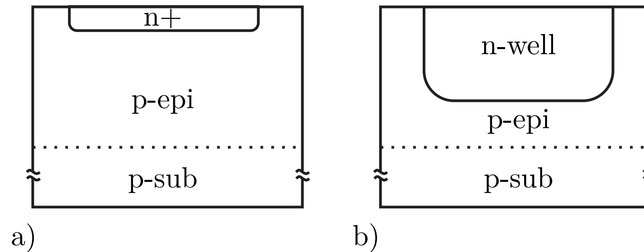


***Figure 3.4: p-n junction based photodiodes used in this work.*** *Note the highly doped shallow n-type region in the n+/p photodiode in a) and the deeper lighter doped n-type well in the n-well/p photodiode in b).*

Starting from electrical characteristics, a closer theoretical view on the dependence of the dark current on mechanical stress is put forward. The dark current of a photodiode under mechanical stress is a crucial parameter for the overall performance of the final CIS. The photodiode dark current has been already modeled using the diffusion current

coming outside of the depletion region and the generation/drift current from within the depletion region in section 2.2.3. Using the equations (2.2.28) and (2.2.33) the dark current $I_{dark}$ can be written:

$$I_{dark} = I_{diff} + I_{ge,V} + I_{ge,S} \tag{3.2.1}$$

$$I_{dark} = \frac{qAD_p n_i^2}{L_p N_D} + \frac{qAD_n n_i^2}{L_n N_A} + \frac{qn_i W_D (A_{hor} + Pd_{vert})}{\tau_g} + qn_i PW_{D,surf} s_g \tag{3.2.2}$$

The direct dependence on the intrinsic carrier concentration can be noticed in (3.2.2). Therefore, the dependence of the intrinsic carrier concentration $n_i$ on the mechanical stress will be analyzed next. Since $n_i^2 = n \cdot p$ the minority carrier concentrations $n$, $p$ will be modeled.

For the occupancy $n$ of the six ellipsoidal constant energy surfaces of the conduction band can be written:

$$n = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} \sum_{i=1}^{6} (m_{C,DOS}^i)^{3/2} \cdot \exp\left[-\frac{(E_C^i - E_F)}{kT}\right] \tag{3.2.3}$$

Note how the index $i$ on the summation runs up to six due to the six energy minima (six valleys) in the principal directions. However every two energy minima are affected by the same manner (are equivalent), thus the index can run up to three in the next steps. Identifying in the above equation the quantities, which depend on mechanical stress based on the discussion in section 3.1 i.e., the DOS effective masses $m_{C,DOS}^i$, the conduction band energy minima $E_C^i$ as well as the Fermi level $E_F$, it can be written under stressed conditions:

$$n^\sigma = \frac{n}{3} \exp\left(\frac{\Delta E_F}{kT}\right) \sum_{i=1}^{3} \left(\frac{m_{C,DOS}^{i,\sigma}}{m_{C,DOS}^i}\right)^{3/2} \exp\left(-\frac{\Delta E_C^i}{kT}\right) \tag{3.2.4}$$

where the superscript $\sigma$ denotes mechanical stress on the quantity, the index $i$ denotes the three principal directions for Si ([001], [101] and [100] directions), $\Delta E_C^i$ and $\Delta E_F$ denote the strain-induced energy shifts of the $i^{th}$ conduction band minimum and the Fermi level respectively.

Similarly, for the hole minority carrier concentration $p$ and accounting for the upper two (LH and HH) valence energy bands can be written:

$$p = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2}\left\{m_{lh}^{3/2}\exp\left[-\frac{\left(E_F - E_V^{lh}\right)}{kT}\right] + m_{hh}^{3/2}\exp\left[-\frac{\left(E_F - E_V^{hh}\right)}{kT}\right]\right\} \quad (3.2.5)$$

Here the split-off band (recall section 2.2.1) is not taken into consideration since it lies lower in energy than the HH and LH bands. Under stressed conditions it can be concluded:

$$p^{\sigma} = \frac{p}{m_{V,DOS}^{3/2}}\exp\left(-\frac{\Delta E_F}{kT}\right)\left[{m_{lh}^{\sigma}}^{3/2}\exp\left(\frac{\Delta E_V^{lh}}{kT}\right) + {m_{hh}^{\sigma}}^{3/2}\exp\left(\frac{\Delta E_V^{hh}}{kT}\right)\right] \quad (3.2.6)$$

where the superscript $\sigma$ denotes mechanical stress on the quantity, $m_{lh}$, $m_{hh}$ are the effective masses of light and heavy holes respectively and $m_{V,DOS}^{3/2} = {m_{lh}}^{3/2} + {m_{hh}}^{3/2}$ the DOS effective masses of the valence band.

Following the technique in [WHB64] the shift in the Fermi level $\Delta E_F$ of a p-type material can be calculated by setting equation (3.2.6) equal to the acceptor density $N_A$ and assuming that the impurity ionization energy is first order stress independent [Kan67]:

$$\exp\left(\frac{\Delta E_F}{kT}\right) = \left(\frac{m_{lh}^{\sigma}}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{lh}}{kT}\right) + \left(\frac{m_{hh}^{\sigma}}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{hh}}{kT}\right) \quad (3.2.7)$$

Substituting (3.2.7) in (3.2.4) the electron minority carrier concentration under stress $n^{\sigma}$ can be written as:

$$n^{\sigma} = \frac{n}{3}\left[\left(\frac{m_{lh}^{\sigma}}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{lh}}{kT}\right) + \left(\frac{m_{hh}^{\sigma}}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{hh}}{kT}\right)\right] \cdot \sum_{i=1}^{3}\left(\frac{m_{C,DOS}^{i,\sigma}}{m_{C,DOS}^{i}}\right)^{3/2}\exp\left(-\frac{\Delta E_C^{i}}{kT}\right) \quad (3.2.8)$$

Using $n_i^2 = n \cdot p$ and following the same procedure for computing the hole minority carrier concentration under stress $p^{\sigma}$, the intrinsic carrier concentration under mechan-

ical stress $n_i^\sigma$ is given by:

$$n_i^\sigma = \frac{n_i}{3}\left[\left(\frac{m_{lh}^\sigma}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{lh}}{kT}\right)+\left(\frac{m_{hh}^\sigma}{m_{V,DOS}}\right)^{3/2}\exp\left(\frac{\Delta E_V^{hh}}{kT}\right)\right]\cdot \sum_{i=1}^{3}\left(\frac{m_{C,DOS}^{i,\sigma}}{m_{C,DOS}^{i}}\right)^{3/2}\exp\left(-\frac{\Delta E_C^i}{kT}\right) \tag{3.2.9}$$

Applying the dictations of the deformation potential theory and the strain-induced changes of the effective masses as modeled in the previous section, the changes of the intrinsic carrier concentration under mechanical stress can be calculated using (3.2.9). The dependence of the intrinsic carrier concentration on the applied mechanical stress is made clear, since $\Delta E_V^{lh}$, $\Delta E_V^{hh}$ and $\Delta E_C^i$ are functions of the mechanical stress (recall tables (3.1) and (3.2)).

Returning back to the discussion on the dark current modeling under mechanical stress, it is worth to note the following: Under the application of non-zero reverse voltages on the photodiodes and before reaching the point where tunneling and impact ionization mechanisms cause the dark current to increase exponentially with the applied reverse voltage, the dominating part of the dark current is the generation current within the depletion region (both in the semiconductor volume as well as at the semiconductor surface). Furthermore, in this model it is assumed that the surface generation velocities of electrons ($s_{gn}$) and holes ($s_{gp}$) are stress independent. Similarly, the generation lifetimes $\tau_{gn}$ and $\tau_{gp}$ are also assumed to be first order stress independent. Therefore, the dark current strain-induced change $\Delta I_{dark}$ can be modeled with the use of (3.2.2) as:

$$\frac{\Delta I_{dark}}{I_{dark}} \approx \frac{\Delta n_i}{n_i} \tag{3.2.10}$$

where $\Delta I_{dark} = I_{dark}^\sigma - I_{dark}$ and $\Delta n_i = n_i^\sigma - n_i$.

Next to the dark current, the photodiode capacitance $C_{PD}$ needs to be modeled under the applied mechanical stress. For the PD depletion capacitance can be written:

$$C_{PD} = \epsilon_s/W_D = \sqrt{\frac{\epsilon_s q N_A}{2(\psi_B + V_R)}} \tag{3.2.11}$$

$$qV_R = E_{F,p} - E_{F,n}$$

where $V_R$ the applied reverse voltage ($V_R > 0$), $\psi_B$ the p-n junction built-in potential, $W_D$ is the width of the formed depletion region of the photodiode (which depends on the applied reverse voltage) and $E_{F,n}$, $E_{F,p}$ are the quasi-Fermi levels for electrons and holes, respectively [SN10]. Assuming that $E_{F,n}$ and $E_{F,p}$ are very close to the conduction band minimum $E_C$ (at the n-side of the photodiode junction) and to the valence band maximum $E_V$ (at the p-side of the photodiode junction) respectively, it can be written [SN10]:

$$q\psi_B \approx E_g/2 + kT\ln(N_D/n_i) \tag{3.2.12}$$

where $N_D$ the donor concentration level at the n-side of the junction. Combining the last two equations we arrive at:

$$C_{PD} \approx \sqrt{\frac{\epsilon_s q^2 N_A}{2qV_R + E_g + 2kT\ln(N_D/n_i)}} \tag{3.2.13}$$

The junction capacitance dependence on mechanical stress is elucidated using (3.2.13), due to its square root dependence on the bandgap $E_g$ and the logarithm of the intrinsic carrier concentration $n_i$. Based on the results of section 3.1 and as will be numerically shown in the next chapter, the bandgap of silicon narrows linearly under mechanical stress. Together with equation (3.2.9) the stress dependence of the PD capacitance can be expressed as:

$$\frac{1}{C_{PD}}\frac{\partial C_{PD}}{\partial \sigma} \approx -\frac{1}{2}\frac{1}{(2qV_R + E_g + 2kT\ln(N_D/n_i))}\left(\frac{\partial E_g}{\partial \sigma} - \frac{2kT}{n_i}\frac{\partial n_i}{\partial \sigma}\right) \tag{3.2.14}$$

where $\sigma$ the applied uniaxial mechanical stress. Both the stress dependence of the bandgap $E_g$ (distance from the valence band edge to the conduction band edge, which both face a strain-induced shift as discussed before) as well as the stress dependence of the intrinsic carrier concentration $n_i$ have been theoretically treated until this section, so that the strain-induced changes of the PD capacitance can be calculated with the help of equation (3.2.14).

Apart from the electrical characteristics, the optical characteristics of silicon p-n

junction based photodiodes under uniaxial mechanical stress are also of great importance. The strain-induced silicon bandgap shift, will have as a result the shift of the indirect absorption edge of silicon, which lies at absorption of wavelengths around 1.1 µm. However, in the visible spectrum of light (400 µm-800 µm) the optical characteristics of photodiodes are not expected to significantly change since the photons in the visible spectrum of light possess much larger energies in comparison with the bandgap of silicon, which under mechanical stress is getting narrower as stated above. Hence, the optical absorption takes place mostly through the help of phonons, which enable the indirect transitions from the valence to the conduction band. The phonons energy spectra though are reported to change slightly under mechanical uniaxial stress [EKP84] and therefore, slight, in fact negligible, changes are expected in the optical response in the visible range, where the photon energy is larger than the silicon bandgap. Due to that, the assumption that the optical response of a p-n junction based photodiode in the visible spectrum of light is stress independent, in respect to the greater changes observed on its electrical response, is reasonable.

## 3.3 Strained Capacitor

Next to the optoelectronic devices used in a CIS, passive devices such as on-chip integrated capacitors and resistors are used widely in the analog peripheral circuitry of the sensor. This subsection focuses only on the dependence of on-chip capacitors on mechanical strain. Resistors under mechanical stress have been thoroughly and extensively studied in the past based on the piezoresistance theory [Smi54] [JSR+00], which will be also used for the study of the inversion channels in MOSFETs in the next subsection. There are three major types of on-chip capacitor offered in a CMOS process namely: polysilicon-insulator-polysilicon (PIP) capacitors, metal-insulator-metal (MIM) capacitors and MOS based capacitors. The former two categories can be simply modeled by the parallel plate capacitor model, which states that the capacitance increases with increasing geometrical dimensions and decreases with increasing insulation thickness between the two conductive plates (in this case made of polysilicon or metal respectively). Assuming that under the application of moderate stress levels ($\ll 1$ GPa as used in this work) the geometrical dimensions of the device do not change, then it is reasonable to assume that the capacitance of the PIP or MIM capacitors is first order stress independent. Stress independence can be similarly assumed for the MOS based

capacitors offered in a CMOS process, since as discussed in section 2.2.4 capacitors of this type are manufactured to remain in accumulation condition (recall table 2.2) in the allowed voltage operation ranges. While in accumulation condition the total capacitance is equal to the oxide capacitance $C_{OX}$ and thus under the assumption of no geometry changes the total capacitance remains stress independent. For completeness, an ideal MOS capacitor would show a stress dependence, since its total capacitance is the series combination of a depletion capacitance and the oxide capacitance. The depletion capacitance is stress dependent, as also discussed in the previous section for the p-n junction. This so called piezocapacitance effect has been described and analyzed from Matsuda and Kanda in [MK03].

## 3.4 Strained MOS Transistor

The application of mechanical stress on semiconductors leads to the change of their resistance, which is widely referred to as piezoresistance effect. The inversion channels of MOS transistors can also be treated as equivalent resistors and be analyzed under stress using the piezoresistance theory. Here, a strong inversion (either in linear or saturation region) is assumed, where the transistor behavior is controlled by the resistive region of the channel and the piezoresistance coefficients are constant (opposite to weak inversion) [Mik81]. The goal of this section is to provide a phenomenological approach to the strain-induced effects on the characteristics of MOS transistors under strong inversion conditions. That means, that microscopic effects (i.e., effects discussed in section 3.1 such as band degeneracy liftings, band splittings and effective mass changes) will be opaque and included in the macroscopic quantity of the mobility $\mu$, which is connected to the resistance through an anti-proportional relation. Theoretical models - electron-mobility models - including these microscopic effects have been reported from different groups lately [EC93] [DUK$^+$07] [KIMT10].

At this point recall the equations governing the long channel MOSFET operation listed in table 2.3. Stress-induced changes on the drain current can be modeled by changes on the mobility $\mu$, geometrical changes of the device width $W$, gate length $L$ and oxide thickness $t_{OX}$. Since strain shifts the band structure and decreases the energy band gap, threshold voltage changes are additionally expected due to the decrease of the flatband voltage $V_{FB}$. Recalling the discussion in section 2.2.4, the figure 2.9 and equation (2.2.35) the threshold voltage $V_T$ under increasing uniaxial mechanical stress

is expected to decrease. Using the square-law equation for MOSFETs operating in the saturation region and assuming small variations the normalized $I_D$ variation $\frac{\Delta I_D}{I_D}$ is given by:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \mu}{\mu} - \frac{t_{OX}}{\Delta t_{OX}} + \frac{\Delta W}{W} - \frac{\Delta L}{L} - 2\frac{\Delta V_T}{V_T}\left(\frac{V_T}{V_{GS} - V_T}\right) + \frac{\Delta \lambda}{\lambda}\left(\frac{\lambda V_{DS}}{1 + \lambda V_{DS}}\right) \quad (3.4.1)$$

However, as was assumed in the previous section, due to the high Young modulus of silicon, geometrical changes are negligible when compared to mobility changes for stresses applied in this work ($<$ 500 MPa). According to [YLL+10] the threshold shifts under uniaxial mechanical stress are described with the help of the bandgap narrowing $\Delta E_g$:

$$\frac{\Delta V_T}{V_T} \approx -\chi_b \Delta E_g \quad (3.4.2)$$

where $\chi_b$ is the ratio of body- to gate-transconductance of the MOSFET ($\sim 0.3$). As explained in [LTF04] and [YLL+10] the threshold voltage faces much smaller shifts under uniaxial mechanical stress in comparison with the application of biaxial stress. Therefore, for the case of uniaxial mechanical stress the strain-induced threshold voltage shifts are neglected in the literature. Similarly, the changes of the channel length modulation parameter $\lambda$ under mechanical stress are assumed to be negligible and as will be shown in the experimental results of this work are $<$ 1 %. Under these considerations equation (3.4.1) the strain-induced normalized drain-current changes $\frac{\Delta I_D}{I_D}$ become:

$$\frac{\Delta I_D}{I_D} \approx \frac{\Delta \mu}{\mu} \quad (3.4.3)$$

In this work and in conjunction with most modern CMOS processes, the CMOS transistors are fabricated on (100) wafers and their channels are allowed to have two orientations: one along the [110] crystallographic direction and one along the [$\bar{1}$10] crystallographic direction. The uniaxial mechanical stress $\sigma$ is applied along the [110]

crystallographic direction and thus (3.4.3) can be rewritten as follows:

$$\left.\frac{\Delta I_D}{I_D}\right|_{[110]} \approx \left.\frac{\Delta\mu}{\mu}\right|_{[110]} = \frac{1}{2}(\pi_{11}^{(v)} + \pi_{12}^{(v)} + \pi_{44}^{(v)}) \cdot \sigma = \pi_L \cdot \sigma \tag{3.4.4}$$

$$\left.\frac{\Delta I_D}{I_D}\right|_{[\bar{1}10]} \approx \left.\frac{\Delta\mu}{\mu}\right|_{[\bar{1}10]} = \frac{1}{2}(\pi_{11}^{(v)} + \pi_{12}^{(v)} - \pi_{44}^{(v)}) \cdot \sigma = \pi_T \cdot \sigma \tag{3.4.5}$$

where $\pi_{11}^{(v)}$, $\pi_{12}^{(v)}$, $\pi_{44}^{(v)}$ the piezoresistance coefficients of silicon in the main crystallographic coordinate system, $\pi_L$ and $\pi_T$ the longitudinal ($\parallel$ [110] crystallographic direction) and transversal piezoresistance ($\perp$ [110] crystallographic direction) coefficients, respectively. For the exact calculation of the drain-current changes under the application of [110] uniaxial mechanical stress refer to the Appendix. The piezoresistance coefficients are strongly dependent on the transistor type, its crystallographic orientation, the doping concentration and temperature [CJS08]. In [Kan82] a model describing the change of the piezoresistive coefficients with temperature and doping level has been presented. In this model the piezoresistive coefficients of silicon vary with the Fermi level and are a function of the Fermi-Dirac Integral [Hul99]. Since the calculation of the piezoresistive coefficients at a certain temperature using the model in [Kan82] is a tedious task, the temperature coefficient of piezoresistance (TCP) is presented in table 3.3 [Hul99]. It is made clear that for both n-type and p-type silicon the piezoresistive coefficients decrease with increasing temperature.

***Table 3.3: Temperature coefficients of piezoresistance (TCP) for n- and p-type silicon as a function of doping concentration*** [Hul99]***.***

| Doping level [$cm^{-3}$] | n-type TCP [%/°C] | p-type TCP [%/°C] |
|---|---|---|
| $5 \cdot 10^{18}$ | -0.28 | -0.27 |
| $1 \cdot 10^{19}$ | -0.27 | -0.27 |
| $3 \cdot 10^{19}$ | -0.19 | -0.18 |
| $1 \cdot 10^{20}$ | -0.12 | -0.16 |

The piezoresistance coefficients are also influenced from the parasitic drain/source resistance $R_{SD}$. This is the reason of the observed differences in piezoresistance coefficients between short and long channel MOSFETs. This difference was sometimes

falsely interpreted as a dependence of the piezoresistance coefficients on the gate length, which however is not valid. Therefore, when analyzing short channel MOSFETs under stress, a correction of the measured data with the experimentally evaluated $R_{SD}$ has to be performed, as described in [KIMT10] and [BJSO01]. The interested reader in the piezoresistance theory should consult [STN07] and [SJ01].

In the last part of this section, the stress-induced changes on the drain current noise $S_{I_D}$ will be briefly presented. As presented in the previous chapter, the total drain current noise $S_{I,ges}$ can be described as:

$$S_{I,ges} = S_{I_D,th} + S_{I_D,1/f} \tag{3.4.6}$$

Since the drain current faces strain-induced changes attributed to stain-induced mobility changes, both terms in equation (3.4.6) are stress-dependent. Starting from the thermal noise component, equations (2.2.41) and ((2.2.42)) reveal a linear dependence on the gate transconductance $g_m$, which in turn is given by:

$$g_m = \sqrt{2(W/L)\mu C_{OX} I_D} \tag{3.4.7}$$

$$g_m = (W/L)\mu C_{OX} V_{ov} \tag{3.4.8}$$

Based on equation (3.4.3) and for the case that the transistor is biased by a constant gate overdrive, the stress-induced changes $\frac{\Delta S_{I_D,th}}{S_{I_D,th}}$ assuming :

$$\frac{\Delta S_{I_D,th}}{S_{I_D,th}} \approx \frac{\Delta g_m}{g_m} \approx \frac{\Delta \mu}{\mu} \approx \frac{\Delta I_D}{I_D} \tag{3.4.9}$$

For the case of a constant current biasing can be similarly written for $\frac{\Delta S_{I_D,th}}{S_{I_D,th}}$:

$$\frac{\Delta S_{I_D,th}}{S_{I_D,th}} \approx \frac{\Delta g_m}{g_m} \approx \frac{1}{2}\frac{\Delta \mu}{\mu} \approx \frac{1}{2}\frac{\Delta I_D}{I_D} \tag{3.4.10}$$

The $1/f$ noise component described by the unified model presented in section 2.2.5 using equation (2.2.43) is also a stress-dependent component. As shown in [LAT+09] the main contributor in the stress dependence of the magnitude of the $1/f$ noise characteristic are the strain-induced changes of the mobility $\mu$. The trap distribution $n_t(E_{F,n})$

is also a stress dependent parameter, which however is shown to be not significant when compared to strain-induced mobility changes. Therefore, the exponent $\alpha$ faces slight changes under the application of mechanical stress. The drain current $I_D$ under mechanical stress is given by equation (3.4.3) so that the total change of the magnitude of the $1/f$ characteristic at a low frequency (1 Hz) $\frac{\Delta S_{I_D,1/f}}{S_{I_D,1/f}}$ can be calculated to be equal to [LAT+09]:

$$\frac{\Delta S_{I_D,1/f}}{S_{I_D,1/f}} \approx 4\frac{\Delta I_D}{I_D} \tag{3.4.11}$$

## 3.5 Basic Analog Circuits under Mechanical Stress

After having modeled and explained the strain-induced effects on the semiconductor electronic structure as well as on diverse semiconductor devices, these models will be used in analyzing the strain-induced effects on analog circuitry. Focus of this section is on modeling strain-induced changes in basic integrated analog circuits and techniques encountered in almost every analog system-on-chip (SoC). This analysis will then extended to typical readout electronic circuitry of CMOS image sensors. Digital integrated circuits will not be considered in the following analysis. The reason for this is that the presented changes in the transistors IV-characteristics will not be noticeable at the output of digital circuits, where the signal swing and the noise margins are high, in addition to the fact that the output is determined only through two voltage levels (high (1) or low (0) corresponding to high or low voltage for a non-inverting logic). Analog ICs are much more sensitive to changes of the device characteristics, since the chosen operation point will be affected. As a result shifts in both DC as well as AC circuit characteristics are expected.

### 3.5.1 Current Mirrors and References

Assume the current mirror shown in figure 3.5a, where the transistor sizes are ratioed by a factor of $m$. For arbitrary transistor orientation and assuming operation in the saturation region (while neglecting the channel-length modulation), can be written for

the current of the reference branch $I_{ref}$:

$$I_{ref} = \frac{k}{2} \frac{W}{L}\bigg|_{M_1} \left( \overbrace{V_{GS,M_1} - V_T}^{V_{ov}} \right)^2 \tag{3.5.1}$$

$$I^{\sigma}_{ref} = (1 + \pi_{M_1}\sigma)\frac{k}{2} \frac{W}{L}\bigg|_{M_1} \left( \overbrace{V^{\sigma}_{GS,M_1} - V_T}^{V^{\sigma}_{ov}} \right)^2 = I_{ref} = \frac{I_{out}}{m} \tag{3.5.2}$$

where $I_{ref}$ is assumed to be a constant stress independent reference current at the moment. Similarly for the output current can be written a similar expression and using equations (3.5.1) and (3.5.2) can be concluded that:

$$\frac{I^{\sigma}_{out}}{I^{\sigma}_{ref}} = \frac{1 + \pi_{M_2}\sigma}{1 + \pi_{M_1}\sigma} \frac{I_{out}}{I_{ref}} \tag{3.5.3}$$

$$\frac{V^{\sigma}_{ov}}{V_{ov}} = \sqrt{\frac{1}{1 + \pi_{M_1}\sigma}} \tag{3.5.4}$$

From the above equations it is clear that if the transistors are placed on a silicon chip very close and exhibit the same orientation on the substrate so that $\pi_{M_1} = \pi_{M_2}$, the stress-induced change of the current ratio is minimized (under the assumption that uniaxial mechanical stress is applied). Note how the $V_{ov}$ of the transistors will change to accommodate the same current. Placing the transistors orthogonally to each other maximizes the influence, since $\pi_{M_1}/\pi_{M_2} \neq 1$, making this topology a good candidate for a stress sensor.

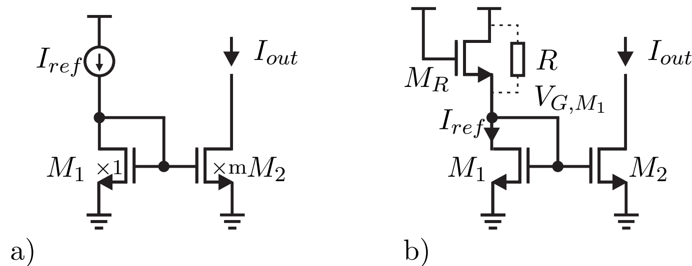


***Figure 3.5: Current mirror configurations.*** *a) An ideal current mirror (ratioed by a factor of m) biased by an external constant reference current. b) Here, the mirror is biased by an on-chip resistor $R$ or diode-connected transistor $M_R$.*

In the above analysis was assumed that $I_{ref}$ is stress independent, which is not totally realistic. This will be the case, if the reference current is externally supplied. Many times though, this reference current is generated on-chip. The simplest way is connecting an on-chip resistor or a diode-connected MOSFET at the drain of $M_1$, as shown in figure 3.5b). Since either the on-chip resistor or the diode-connected transistor show a piezoresistive behaviour, the reference current will not be constant in the general case. An illustrative way to show this change, is superimposing the load IV-characteristics on the $M_1$ IV-characteristics as illustrated in figure 3.6. If the goal is to minimize the influence of the applied uniaxial stress on the reference current, the piezoresistive coefficients of the load and the transistor of the current mirror need to have the same sign. The gate overdrive voltage will change in order to accommodate the same reference current, as illustrated in the figure below. In the case of opposite signs of the piezoresistive coefficients the current of the left branch will be influenced (see figure 3.6), causing a stress-induced output current change.

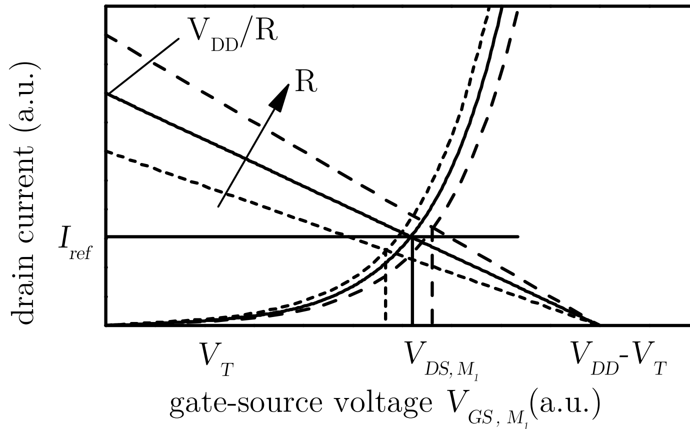


***Figure 3.6: Superimposing the resistor load line on the MOSFET IV-characteristic.*** *Note how the load line changes with the change of the effective resistance R under mechanical stress. In order for $I_{ref}$ to stay constant, the piezoresistive coefficients of the load and of the transistor of the current mirror need to have the same sign, which will lead to the adaptation of the gate overdrive $V_{ov}$. In case that the designer opts for a constant $V_{ov}$, then piezoresistive coefficients of the opposite sign will lead to adaptation of the current to a new value $I_{ref}^{\sigma}$.*

## 3.5.2 Single- and Multiple-Transistor Amplifiers

While current mirrors are essential circuit blocks in analog design, single transistor amplifiers represent fundamental building blocks as well. In this subsection the common drain (source follower) and common source circuit configurations will be analyzed under mechanical stress from a DC as well as AC standpoint. Let the analysis start from the DC analysis of a source follower in the configurations depicted in figures 3.7a) and 3.7b). Here, it is worth to note that the reference transistor $M_{bias}$ sets the current through $M_{SF}$ and can be controlled either via a constant reference voltage source or via a current-mirror circuit. The effects on stress on the two topologies are different, but lead to a similar result; namely, the strain-induced DC shift of the output voltage.

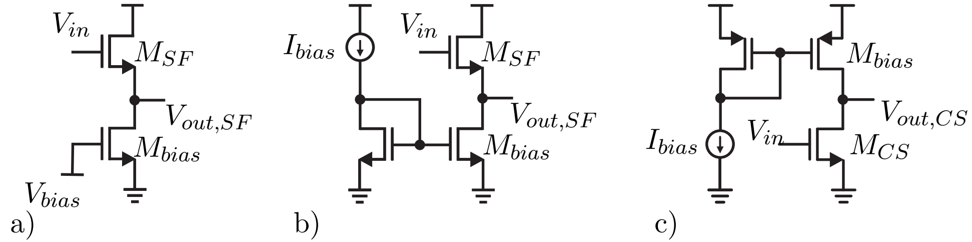


***Figure 3.7: Common drain and common source circuit (source follower) configurations.*** *Biasing the SF by a) a current source using a MOSFET with a constant gate-source reference voltage b) a current source using a current mirror biased by a constant reference current. c) A common source circuit using a current mirror biased by a constant reference current.*

The large signal DC transfer characteristics of the SF can be derived as follows:

$$V_{in} = V_{out,SF} + V_T + V_{ov,M_{SF}} \tag{3.5.5}$$

Using the square law equation for modeling the drain-source current of the transistors (recall table 2.3) and neglecting the channel length modulation, it can be written for the drain current of both $M_{SF}$ and $M_{bias}$:

$$I_{SF} = \frac{k_{M_{SF}}}{2} \frac{W}{L}\bigg|_{M_{SF}} (V_{ov,M_{SF}})^2 = I_{bias} \tag{3.5.6}$$

$$I_{bias} = \frac{k_{M_{bias}}}{2} \frac{W}{L}\bigg|_{M_{bias}} (V_{bias} - V_T)^2 \tag{3.5.7}$$

$$V_{ov,M_{SF}} = V_{GS,M_{SF}} - V_T = V_{in} - V_{DS,M_{bias}} - V_T \tag{3.5.8}$$

$$V_{DS,M_{bias}} = V_{out,SF} \tag{3.5.9}$$

The above equations are valid provided that both transistors operate in the saturation region and that the output resistance of the lower transistor is large. Moreover, body-effect is at this point not included in the analysis and the threshold voltage is assumed to be constant under mechanical stress, after the discussion in the previous subsection. Of great importance is to calculate the minimum input voltage $V_{in}$ or the minimum overdrive $V_{ov,M_{SF}}$, which still maintains $M_{bias}$ in saturation under the unstressed and the stressed states. When the lower transistor is at the verge of saturation the following equations hold:

$$V_{out,SF}\big|_{sat} = V_{DS,sat,M_{bias}} = V_{bias} - V_T = V^{\sigma}_{DS,sat,M_{bias}} = V^{\sigma}_{out,SF}\big|_{sat} \tag{3.5.10}$$

$$V_{ov,M_{SF}}|_{min} = V_{in}|_{min} - V_{bias} \tag{3.5.11}$$

Assuming the general situation of different channel orientations of $M_{SF}$ and $M_{bias}$ can be concluded for the stressed condition:

$$I^{\sigma}_{SF} = I^{\sigma}_{bias} \tag{3.5.12}$$

$$I^{\sigma}_{bias} = \frac{k^{\sigma}_{M_{bias}}}{2} \frac{W}{L}\bigg|_{M_{bias}} (V_{bias} - V_T)^2 = (1 + \pi_{M_{bias}}\sigma) I_{bias} \tag{3.5.13}$$

Setting the two currents equal, a relation between the needed minimum input voltage or the minimum overdrive in the stressed and unstressed condition in order maintain $M_{bias}$ in saturation can be derived:

$$V^{\sigma}_{ov,M_{SF}}\big|_{min} = \sqrt{\frac{1 + \pi_{M_{bias}}\sigma}{1 + \pi_{M_1}\sigma}}\, V_{ov,M_{SF}}|_{min} \tag{3.5.14}$$

$$V^{\sigma}_{in}|_{min} = \sqrt{\frac{1 + \pi_{M_{bias}}\sigma}{1 + \pi_{M_1}\sigma}}\, V_{in}|_{min} + \left(1 - \sqrt{\frac{1 + \pi_{M_{bias}}\sigma}{1 + \pi_{M_1}\sigma}}\right) V_{bias} \tag{3.5.15}$$

The next step is to analyze the small-signal AC characteristics of this configuration. First the change of the source follower small-signal voltage gain under stress is calculated, when both transistors are working in the saturation regime. The changes of the transistors transconductances under stress are calculated with the help of (3.5.6), (3.5.7) (3.5.12) and (3.5.13):

$$g^{\sigma}_{m,M_{bias}} = \sqrt{2\mu^{\sigma}_{M_{bias}} C_{OX} \left.\frac{W}{L}\right|_{M_{bias}} I_{bias}} = \left(1 + \pi_{M_{bias}}\sigma\right) g_{m,M_{bias}} \tag{3.5.16}$$

$$g^{\sigma}_{m,M_{SF}} = \sqrt{2\mu^{\sigma}_{M_{SF}} C_{OX} \left.\frac{W}{L}\right|_{M_{SF}} I_{SF}} = \sqrt{\left(1 + \pi_{M_{SF}}\sigma\right)\left(1 + \pi_{M_{bias}}\sigma\right)} g_{m,M_{SF}} \tag{3.5.17}$$

Similarly the output conductances $g_{ds}$ of the transistors are calculated, assuming that the channel length modulation parameter $\lambda$ is a stress-independent quantity (as was discussed earlier and will be verified in the experimental results chapter):

$$g^{\sigma}_{ds,M_{bias}} \approx \lambda I^{\sigma}_{bias} = \lambda(1 + \pi_{M_{bias}}\sigma) I_{bias} = (1 + \pi_{M_{bias}}\sigma) g_{ds,M_{bias}} \tag{3.5.18}$$

$$g^{\sigma}_{ds,M_{SF}} \approx \lambda I^{\sigma}_{SF} = \lambda(1 + \pi_{M_{bias}}\sigma) I_{bias} = (1 + \pi_{M_{bias}}\sigma) g_{ds,M_{SF}} \tag{3.5.19}$$

Substituting these results in the well known formula for the source follower small signal gain $A_{SF}$ [GHLM01] gives:

$$A^{\sigma}_{SF} = \frac{g^{\sigma}_{m,M_{SF}}}{g^{\sigma}_{m,M_{SF}} + g^{\sigma}_{mb,M_{SF}} + g^{\sigma}_{ds,M_{SF}} + g^{\sigma}_{ds,M_{bias}}} \tag{3.5.20}$$

$$A^{\sigma}_{SF} = \frac{g_{m,M_{SF}}}{g_{m,M_{SF}} + \chi_b g_{m,M_{SF}} + \sqrt{\frac{1+\pi_{M_{bias}}\sigma}{1+\pi_{M_{SF}}\sigma}} (g_{ds,M_{SF}} + g_{ds,M_{bias}})} \approx A_{SF} \tag{3.5.21}$$

where $\chi_b$ the ratio of body- to gate-transconductance of a MOSFET. The above equations allow us to claim, that the source follower small signal gain is a mechanical stress independent quantity, if the channel orientations of both transistors $M_{bias}$ and $M_{SF}$ are kept the same on the silicon substrate (thus $\pi_{M_{SF}} = \pi_{M_{bias}}$). If the channel orientations are different ($\pi_{M_{SF}} \neq \pi_{M_{bias}}$) the source follower small signal gain is a mechanical stress independent quantity only if the output conductances $g_{ds,M_{bias}}$ and $g_{ds,M_{SF}}$ are very low compared to the transconductances ($g_m$).

For the second configuration shown in figure 3.7b), a similar analysis can be performed. Using the results of section 3.5.1 and assuming no channel-length modulation can be shown for $M_{bias}$ at the verge of saturation that:

$$V_{GS,M_{bias}} - V_T = V_{DS,sat,M_{bias}} \tag{3.5.22}$$

$$V^{\sigma}_{DS,sat,M_{bias}} = \sqrt{\frac{1}{1+\pi_{M_1}\sigma}} V_{DS,sat,M_{bias}} \tag{3.5.23}$$

$$A^{\sigma}_{SF} = \frac{\sqrt{1+\pi_{M_{SF}}\sigma}\, g_{m,M_{SF}}}{\sqrt{1+\pi_{M_{SF}}\sigma}(g_{m,M_{SF}} + g_{mb,M_{SF}}) + (g_{ds,M_{SF}} + g_{ds,M_{bias}})} \approx A_{SF} \tag{3.5.24}$$

For the second configuration the source follower small signal gain is a mechanical stress independent quantity, as long as the output conductances $g_{ds,M_{bias}}$ and $g_{ds,M_{SF}}$ are very low compared to the transconductances ($g_m$). Using the above equations the DC shift of the source follower output can be written:

$$V^{\sigma}_{out,SF} = V_{out,SF} - A_{SF}\Delta V^{\sigma}_{DS,sat,M_{bias}} = V_{out,SF} - \delta_{SF} \tag{3.5.25}$$

Figure 3.8 illustrates the above presented results. The voltage transfer characteristic faces a stress-induced shift, while the slope of the characteristic (i.e., small signal voltage gain $A_{SF}$) is not affected through the application of mechanical stress.

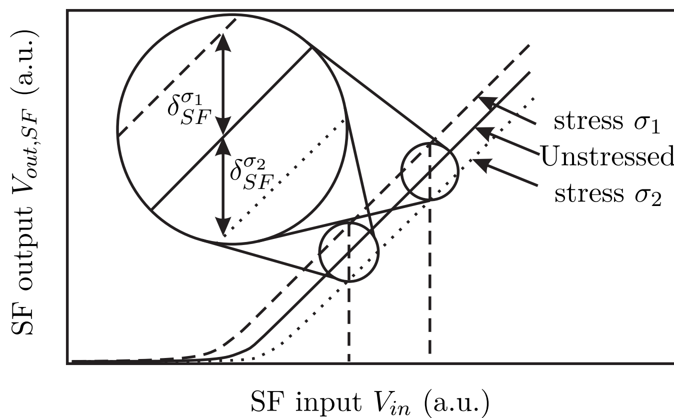


***Figure 3.8: Common drain circuit (source follower) voltage transfer characteristics.*** *Note how the transfer characteristic may shift with applied mechanical stress $\sigma_1$ or $\sigma_2$, without however changing its slope. $\delta_{SF}$ denotes the stress-induced shift of the source follower output voltage $V_{out,SF}$.*

In the following, the results of a common source (CS) circuit stage (figure 3.7c)) with a current source load will be analyzed with the same technique. Following the same procedure as before and using the square-law equation for describing both MOS transistors and accounting for channel length modulation, the large signal (DC) analysis reveals:

$$I_{CS} = \frac{k_{M_{CS}}}{2} \frac{W}{L}\bigg|_{M_{CS}} (V_{in} - V_T)^2 (1 + \lambda V_{out}) = I_{bias} \tag{3.5.26}$$

$$I_{bias} = \frac{k_{M_{bias}}}{2} \frac{W}{L}\bigg|_{M_{bias}} (V_{DD} - V_{bias} - V_T)^2 (1 + \lambda |V_{out} - V_{DD}|) \tag{3.5.27}$$

Rewriting equations (3.5.26) and (3.5.27) under mechanical stress using the piezoresistive coefficients $\pi_{M_{CS}}$ and $\pi_{M_{bias}}$ and taking into consideration that the output voltage will face a shift $\Delta V_{out} = V_{out}^{\sigma} - V_{out}$ the following equations can be written. Here the currents will be set equal $I_{CS} = I_{bias}$ and the unstressed equations will be divided with the stressed ones:

$$\frac{1 + \pi_{M_{CS}}\sigma}{1 + \pi_{M_{bias}}\sigma} \frac{k'_{M_{CS}}}{k'_{M_{bias}}} \left( \frac{V_{in} - V_T}{V_{DD} - V_{bias} - V_T} \right)^2 = \frac{1 + \lambda (V_{out}^{\sigma} - V_{DD})}{1 + \lambda V_{out}^{\sigma}} \tag{3.5.28}$$

$$\xrightarrow{\lambda V_{out}^{\sigma} \ll 1} \frac{1 + \pi_{M_{CS}}\sigma}{1 + \pi_{M_{bias}}\sigma} \frac{k'_{M_{CS}}}{k'_{M_{bias}}} \left( \frac{V_{in} - V_T}{V_{DD} - V_{bias} - V_T} \right)^2 = (1 + \lambda (V_{DD} - V_{out}^{\sigma})) (1 - \lambda V_{out}^{\sigma}) \tag{3.5.29}$$

$$\xrightarrow{\lambda V_{out} \ll 1} \frac{1 + \pi_{M_{CS}}\sigma}{1 + \pi_{M_{bias}}\sigma} (1 + \lambda (V_{DD} - V_{out})) (1 - \lambda V_{out}) = (1 + \lambda (V_{DD} - V_{out}^{\sigma})) (1 - \lambda V_{out}^{\sigma}) \tag{3.5.30}$$

$$\xrightarrow{(\lambda V_{out})^2 \ll 1} \frac{1 + \pi_{M_{CS}}\sigma}{1 + \pi_{M_{bias}}\sigma} (1 + \lambda (V_{DD} - 2V_{out})) = 1 + \lambda (V_{DD} - 2V_{out}^{\sigma}) \tag{3.5.31}$$

$$\tag{3.5.32}$$

$$\Rightarrow \Delta V_{out} = V_{out}^{\sigma} - V_{out} = \left( 1 - \frac{1 + \pi_{M_{CS}}\sigma}{1 + \pi_{M_{bias}}\sigma} \right) \left( \frac{1}{2\lambda} + \frac{V_{DD}}{2} - V_{out} \right) \tag{3.5.33}$$

For the small signal (AC) analysis of the circuit, similarly as for the source follower,

can be written:

$$g^{\sigma}_{m,M_{CS}} = \sqrt{2\mu^{\sigma}_{M_{CS}} C_{OX} \left.\frac{W}{L}\right|_{M_{CS}} I_{bias}} = \sqrt{(1+\pi_{M_{CS}}\sigma)\,(1+\pi_{M_{bias}}\sigma)}\, g_{m,M_{CS}} \quad (3.5.34)$$

$$g^{\sigma}_{ds,M_{bias}} \approx \lambda I^{\sigma}_{bias} = (1+\pi_{M_{bias}}\sigma) g_{ds,M_{bias}} \quad (3.5.35)$$

$$g^{\sigma}_{ds,M_{CS}} \approx \lambda I^{\sigma}_{CS} = (1+\pi_{M_{bias}}\sigma) g_{ds,M_{CS}} \quad (3.5.36)$$

$$A_{CS} = \frac{g_{m,M_{CS}}}{g_{ds,M_{CS}} + g_{ds,M_{bias}}} \quad (3.5.37)$$

$$A^{\sigma}_{CS} = \frac{\sqrt{1+\pi_{M_{CS}}\sigma}}{\sqrt{1+\pi_{M_{bias}}\sigma}} A_{CS} \quad (3.5.38)$$

It is made clear, that contrary to a SF, the small signal voltage gain of the common source configuration $A_{CS}$ might be affected under the application of mechanical stress. Recall from figure 3.7c) that transistors $M_{CS}$ and $M_{bias}$ are of different types (n-type and p-type or p-type and n-type respectively). If the minimization of the stress-induced effects is wished, then transistors of different types should exhibit matched piezoresistive coefficients. Following the presented techniques, the designer can analyze any single-transistor configuration under stress, so as to estimate the expected stress-induced shifts on the DC characteristics as well as on AC parameters, such as the small-signal voltage gain or the input and output impedance. Before closing this subsection, the analysis of the useful and commonly-used differential amplifier is presented next. The topology to be analyzed is depicted in figure 3.9 and the tail current source is biased using either a current mirror or a constant voltage at the gate of $M_{tail}$. The circuit will be treated in the general case, where the tail current source is stress-dependent, thus $I^{\sigma}_{tail} = (1+\pi_{M_{tail}\sigma})I_{tail}$. The analysis becomes here more complicated and therefore, we will make a realistic assumption, that the output DC level in the unstressed state (output offset), with the inputs on a constant DC level driving $M_1$ and $M_2$ in saturation, is set midway between the supply voltages to maximize output swing, i.e, $V_{out,DC} = V_{DD}/2 = |V_{GS,M_4}|$. Moreover, it is assumed that all transistors of the same type have the same orientation on the chip, thus exhibiting same piezoresistive coefficients. i.e., $\pi_{M_1} = \pi_{M_2} = \pi_{M_{tail}}$ and $\pi_{M_3} = \pi_{M_4}$. The coefficient $k$ is defined as before, namely $k = \mu C_{OX}$, while its primed version includes the transistor geometry, i.e., $k' = \mu C_{OX} {}^{W}/_{L}$. For the current of the transistors in the left

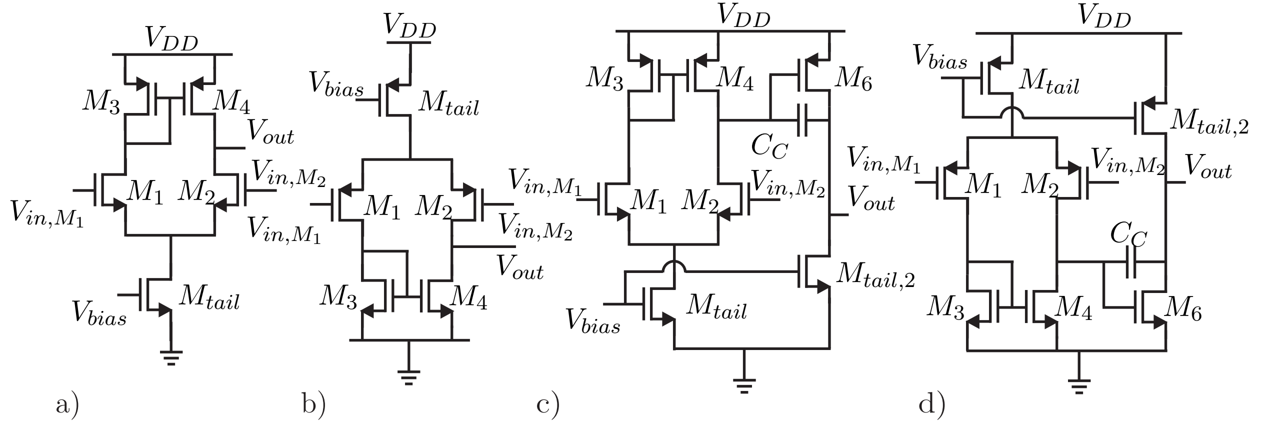


***Figure 3.9: Differential and two-stage Miller amplifier topologies under analysis.*** *a)-b) Differential amplifier with n-type and p-type input transistors respectively. c)-d) Two-stage Miller amplifier with n-type and p-type input transistors respectively. The tail current sources can be biased using either a current mirror or a constant reference voltage.*

branch under unstressed and stressed state, can be written:

$$I_{M_1} = I_{M_3} = \frac{k_{M_3}}{2} \frac{W}{L}\bigg|_{M_3} \left(|V_{GS_{M_3}}| - |V_T|\right)^2 \left(1 + \lambda |V_{DS_{M_3}}|\right) \tag{3.5.39}$$

$$I^{\sigma}_{M_1} = I^{\sigma}_{M_3} = (1 + \pi_{M_3}\sigma)\frac{k_{M_3}}{2} \frac{W}{L}\bigg|_{M_3} \left(|V^{\sigma}_{GS_{M_3}}| - |V_T|\right)^2 \left(1 + \lambda |V^{\sigma}_{DS_{M_3}}|\right) \tag{3.5.40}$$

$$\Delta V_{DS_{M_3}} = |V^{\sigma}_{DS_{M_3}}| - |V_{DS_{M_3}}| \tag{3.5.41}$$

$$I^{\sigma}_{M_3} = I^{\sigma}_{tail}/2 = (1 + \pi_{M_{tail}}\sigma) I_{tail}/2 = (1 + \pi_{M_{tail}}\sigma) I_{M_3} \tag{3.5.42}$$

Assuming that the stress-induced shift $\Delta V_{DS_{M_3}}$ is very small under the application of moderate stress levels, all terms $\lambda \Delta V_{DS_{M_3}} \ll 1$ and all terms of $\Delta V_{DS_{M_3}}{}^2 \ll 1$ can be neglected.

$$\frac{1 + \pi_{M_{tail}}\sigma}{1 + \pi_{M_3}\sigma} I_{M_3} = \frac{k'_{M_3}}{2} \left(|V_{GS_{M_3}}| + \Delta V_{DS_{M_3}} - |V_T|\right)^2 \left(1 + \lambda |V_{DS_{M_3}}|\right) \tag{3.5.43}$$

$$\Rightarrow \frac{1 + \pi_{M_{tail}}\sigma}{1 + \pi_{M_3}\sigma} I_{M_3} \approx I_{M_3} + 2\Delta V_{DS_{M_3}} \frac{I_{M_3}}{\left(|V_{GS_{M_3}}| - |V_T|\right)} \tag{3.5.44}$$

$$\Rightarrow \Delta V_{OS} = -\Delta V_{DS_{M_3}} = -\frac{1}{2} \frac{(\pi_{M_{tail}} - \pi_{M_3})\sigma}{1 + \pi_{M_3}\sigma} (|V_{GS_{M_3}}| - |V_T|) \tag{3.5.45}$$

Similarly, for the small-signal analysis the transconductances and output conductances under stress under the previous assumptions need to be calculated. Afterward the voltage gain shift, the −3dB bandwidth $f_{-3dB}$ and other AC characteristics can be calculated.

$$g^{\sigma}_{m,M_1} = g^{\sigma}_{m,M_2} = \sqrt{2\mu^{\sigma}_{M_1} C_{OX} \left.\frac{W}{L}\right|_{M_1} I^{\sigma}_{tail}/2} = (1 + \pi_{M_1}\sigma)\, g_{m,M_1} \tag{3.5.46}$$

$$g^{\sigma}_{ds,M_2} = \frac{\lambda I^{\sigma}_{M_2}}{1 + \lambda V^{\sigma}_{DS,M_2}} = \frac{\lambda I^{\sigma}_{M_2}}{1 + \lambda(V_{DD}/2 + \Delta V_{DS,M_2})} \tag{3.5.47}$$

$$g^{\sigma}_{ds,M_4} = \frac{\lambda I^{\sigma}_{M_4}}{1 + \lambda|V_{DS,M_4}|} = \frac{\lambda I^{\sigma}_{M_4}}{1 + \lambda(V_{DD}/2 - \Delta V_{DS,M_2})} \tag{3.5.48}$$

$$A_d = \frac{g_{m,M_2}}{g_{ds,M_2} + g_{ds,M_4}} \tag{3.5.49}$$

Keeping in mind that $I^{\sigma}_{M_2} = I^{\sigma}_{M_4}$ and $V_{DS_{M_2}} = V_{DD}/2$, while neglecting all terms $\lambda\Delta V_{DS_{M_2}} \ll 1$ and all terms of $\Delta V_{DS_{M_2}}{}^2 \ll 1$:

$$g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4} = \frac{2\lambda I^{\sigma}_{M_2}(1 + \lambda V_{DS,M_2})}{(1 + \lambda V_{DS,M_2})^2 + (\lambda\Delta V_{DS_{M_2}})^2} \tag{3.5.50}$$

$$\Rightarrow g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4} \approx (1 + \pi_{M_{tail}}\sigma)\frac{2\lambda I_{M_2}}{1 + \lambda V_{DS,M_2}} \tag{3.5.51}$$

$$\Rightarrow g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4} \approx (1 + \pi_{M_{tail}}\sigma)(g_{ds,M_2} + g_{ds,M_4}) \tag{3.5.52}$$

$$A^{\sigma}_d = \frac{g^{\sigma}_{m,M_2}}{g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4}} \approx \frac{(1 + \pi_{M_{tail}}\sigma)g_{m,M_2}}{(1 + \pi_{M_{tail}}\sigma)(g_{ds,M_2} + g_{ds,M_4})} = A_d \tag{3.5.53}$$

$$f^{\sigma}_{-3dB} = \frac{g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4}}{C_L} \approx (1 + \pi_{M_{tail}}\sigma)f_{-3dB} \tag{3.5.54}$$

From the above equations, it is evident that the small signal voltage gain of the presented differential amplifier, when transistors exhibit equal piezoresistive coefficients are utilized, will not be affected under the application of mechanical stress. However, the -3dB bandwidth of the amplifier is stress-dependent, as well as the DC offset of the output. If the minimization of the stress-induced effects is wished, then transistors with matched piezoresistive coefficients should be used. Moreover, choosing channel

orientations exhibiting low piezoresistive coefficients is advantageous.

### 3.5.3 Two-Stage Operational Amplifier

In this subsection the fundamental two-stage Miller amplifier will be analyzed under mechanical stress, using the procedure utilized throughout this chapter. First the shifts in the DC characteristics will be derived and then the AC characteristics under stress will be calculated. The transistor schematic of the amplifier is shown in figure 3.9 and the tail current source can be biased using either a current mirror or a constant reference voltage. Using the results of the previous subsections regarding the differential amplifier at the input as well as the tail current source under mechanical stress, can be written for the bias current of the second stage:

$$I_{M_{tail,2}} = I_{M_6} = \frac{k_{M_6}}{2} \left.\frac{W}{L}\right|_{M_6} \left(|V_{GS_{M_6}}| - |V_T|\right)^2 \left(1 + \lambda |V_{DS_{M_6}}|\right) \tag{3.5.55}$$

$$I^{\sigma}_{M_{tail,2}} = I^{\sigma}_{M_6} = (1 + \pi_{M_6}\sigma) \frac{k_{M_6}}{2} \left.\frac{W}{L}\right|_{M_6} \left(|V^{\sigma}_{GS_{M_6}}| - |V_T|\right)^2 \left(1 + \lambda |V^{\sigma}_{DS_{M_6}}|\right) \tag{3.5.56}$$

$$I^{\sigma}_{M_{tail,2}} = (1 + \pi_{M_{tail,2}}\sigma) I_{M_{tail,2}} \tag{3.5.57}$$

Rewriting the above equations for $\Delta V_{DS_{M_6}} = |V^{\sigma}_{DS_{M_6}}| - |V_{DS_{M_6}}|$, neglecting all terms of ${\Delta V_{DS_{M_6}}}^2 \ll 1$ can be shown for the shift of the output offset of the amplifier:

$$\Delta V_{OS} = -\Delta V_{DS_{M_6}} = \frac{\left[\frac{(\pi_{M_{tail,2}} - \pi_{M_6})\sigma}{1 + \pi_{M_6}\sigma} (|V_{GS_{M_6}}| - |V_T|) - 2\Delta V_{DS_{M_3}}\right]}{\lambda(|V_{GS_{M_6}}| - |V_T| - 2\Delta V_{DS_{M_3}})} (1 + \lambda |V_{DS_{M_6}}|) \tag{3.5.58}$$

Next, a quick overview of the small signal AC characteristics of the presented amplifier will be put forward. Utilizing $I^{\sigma}_{M_{tail}} = (1 + \pi_{M_{tail}}\sigma) I_{M_{tail}}$ can be written for the transconductances $g_m$ and output conductances $g_{ds}$:

$$g^{\sigma}_{m,M_2} = (1 + \pi_{M_{tail}}\sigma) g_{m,M_2} \tag{3.5.59}$$

$$g^{\sigma}_{m,M_6} = \sqrt{(1 + \pi_{M_{tail,2}}\sigma)(1 + \pi_{M_6}\sigma)}\, g_{m,M_6} \tag{3.5.60}$$

$$g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4} \approx (1 + \pi_{M_{tail}}\sigma)(g_{ds,M_2} + g_{ds,M_4}) \tag{3.5.61}$$

$$g^{\sigma}_{ds,M_{tail,2}} + g^{\sigma}_{ds,M_6} \approx (1 + \pi_{M_{tail,2}}\sigma)(g_{ds,M_{tail,2}} + g_{ds,M_6}) \tag{3.5.62}$$

Looking at the small signal AC voltage gain $A_d$ and gain-bandwidth product $GBW$ of the amplifier and using the above equations and the results of the previous section can be written:

$$A^{\sigma}_d = \frac{g^{\sigma}_{m,M_2} g^{\sigma}_{m,M_6}}{(g^{\sigma}_{ds,M_2} + g^{\sigma}_{ds,M_4})(g^{\sigma}_{ds,M_{tail,2}} + g^{\sigma}_{ds,M_6})} \tag{3.5.63}$$

$$\Rightarrow A^{\sigma}_d \approx \frac{(1 + \pi_{M_{tail}}\sigma) g_{m,M_2} \sqrt{(1 + \pi_{M_{tail,2}}\sigma)(1 + \pi_{M_6}\sigma)} g_{m,M_6}}{(1 + \pi_{M_{tail}}\sigma)(g_{ds,M_2} + g_{ds,M_4})(1 + \pi_{M_{tail,2}}\sigma)(g_{ds,M_{tail,2}} + g_{ds,M_6})} \tag{3.5.64}$$

$$\Rightarrow A^{\sigma}_d \approx \sqrt{\frac{1 + \pi_{M_6}\sigma}{1 + \pi_{M_{tail,2}}\sigma}} A_d \tag{3.5.65}$$

$$GBW^{\sigma} \approx \frac{g^{\sigma}_{m,M_2}}{C_C} = (1 + \pi_{M_{tail}}\sigma) GBW \tag{3.5.66}$$

From the above equations, it is evident that the small signal voltage gain of the two-stage operational amplifier, when same type transistors exhibit equal piezoresistive coefficients are utilized, may be affected under the application of mechanical stress. Recall from figure 3.9 that transistors $M_6$ and $M_{tail}$ are of different types (n-type and p-type or p-type and n-type respectively). If the piezoresistive coefficient of the transistor $M_6$ is not matched to the one of transistor $M_{tail}$ then small signal voltage gain $A_d$ will face a change, as equation (3.5.66) is dictating. However, the -3dB bandwidth of the amplifier is stress-dependent, as well as the DC offset of the output. If the minimization of the stress-induced effects is wished, then transistors with matched piezoresistive coefficients should be used. Moreover, choosing channel orientations exhibiting low piezoresistive coefficients is advantageous.

## 3.6 CIS Readout Circuits under Mechanical Stress

In the last subsection of this chapter and using the knowledge gained in the previous subsections, the entire structure of the readout circuitry of an image sensor can be put under the microscope. Our goal is to design a readout circuit, which remains mechanical stress-independent. In section 2.3 diverse pixel designs were presented and the CDS technique was put forward. Here, the great importance of negative feedback towards a mechanical stress independence will be first emphasized and then the effects of mechanical stress on the proposed pixel readout circuits will be analyzed. Let us consider the circuit shown in figure 3.10, implementing a CDS amplifier employing negative feedback.

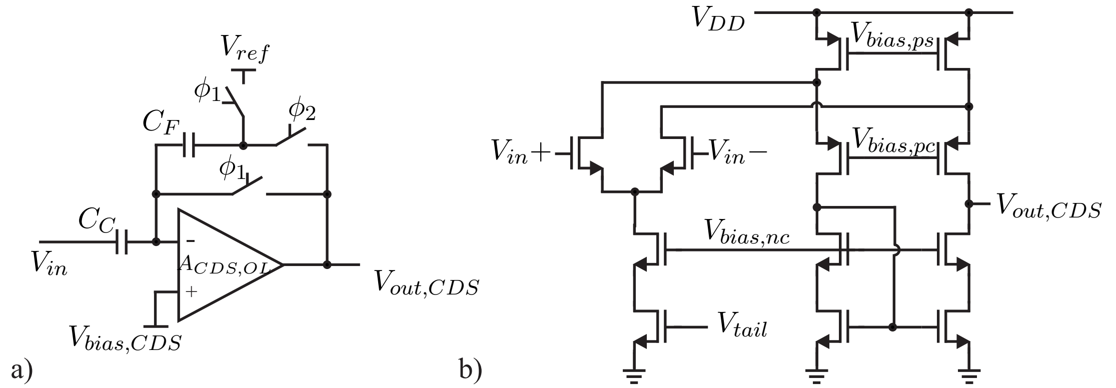


***Figure 3.10: Correlated double sampling amplifier topology under analysis employing negative feedback.*** *a) System overview. The reference voltages $V_{ref}$ and $V_{bias,CDS}$ are assumed to be supplied by stress-independent voltage sources. b) Employed folded cascode amplifier. The reference voltages $V_{tail}$, $V_{bias,ns}$, $V_{bias,nc}$, $V_{bias,ps}$ and $V_{bias,pc}$ are provided from a bias network not shown in the figure.*

The operational amplifier can be a two-stage Miller amplifier as presented in the previous subsection or a simpler one-stage folded cascode amplifier. The circuit operates as a switched-capacitor amplifier and uses two-phase ($\phi_1$ and $\phi_2$) non-overlapping clock signals for the switch control. As presented before, a shift of the open loop gain $A_{CDS,OL}$ of the amplifier is expected, since the input stage transconductance $g_m$ is subject to change under stress. Similarly, the output offset voltage $V_{OS}$ will change under mechanical stress. However, examination of the closed loop system with negative feedback yields, that the dependence of the CDS circuit on mechanical stress is much

lower than its open-loop counterpart. If the open loop system voltage gain remains high enough the use of the negative feedback results in a closed loop system gain $A_{CDS}$ equal to $A_{CDS} = |{}^{C_C}/{}_{C_F}|$. Mathematically stated, small stress-induced changes of the open loop gain $\Delta A_{CDS,OL}$ are suppressed, when observing the closed loop gain of the system. This effect can be elucidated by differentiating equation (3.6.1):

$$A_{CDS} = \frac{|{}^{C_C}/{}_{C_F}|}{1 + {}^{1}/{}_{A_{CDS,OL}}} \approx \left|\frac{C_C}{C_F}\right| \tag{3.6.1}$$

$$\frac{\Delta A_{CDS}}{A_{CDS}} = \frac{1}{1 + A_{CDS,OL}{}^{C_F}/{}_{C_C}} \frac{\Delta A_{CDS,OL}}{A_{CDS,OL}} \ll \frac{\Delta A_{CDS,OL}}{A_{CDS,OL}} \tag{3.6.2}$$

$$\Rightarrow A^{\sigma}_{CDS} \approx A_{CDS} \tag{3.6.3}$$

Stating this in a different way, the sensitivity of the closed loop system gain to variations of the open loop gain is very low. Thus the use of feedback in stressed circuits is highly recommended in order to decrease the circuit sensitivity to parameter variations resulting from the applied mechanical stress and thus avoiding the need of compensating mechanisms (or circuit concepts) in order to retain a stress-independent operation. Under mechanical stress the capacitance of $C_C$ and $C_F$ is considered in our analysis constant, since PIP on-chip capacitors can be used, which under moderate stress levels are stress-independent as explained in section 3.3. Next, the switches, typically realized using MOSFETs, will show some change of their charging characteristic under stress, as we described in section 3.4. The increase (decrease) of the drain current under stress will impact their charging ability and hence a change of the charging or discharging time of the capacitors is expected, without observing, however, a change on the final charge stored it the capacitors. Two non-overlapping clocks $\phi_1$ and $\phi_2$ control the reset and sampling periods of the circuit. During $\phi_1$ the CDS output voltage is reset to $V^{\phi_1}_{OUT,CDS} = V_{bias,CDS}$. The input voltage is sampled during $\phi_1$ $V^{\phi_1}_{in}$ in the capacitor $C_C$. Later on, the clock $\phi_1$ is lowered to logical 0 and $\phi_2$ is raised to logical 1. During $\phi_2$ the input voltage is sampled again during $\phi_2$ $V^{\phi_2}_{in}$. Assuming a change of the $V_{in}$ between $\phi_1$ and $\phi_2$ the difference of these values (i.e., $V^{\phi_1}_{in} - V^{\phi_2}_{in}$ ) is stored at the capacitors during $\phi_2$. This difference multiplied by the amplification factor of the stage $A_{CDS}$, will then determine the output voltage of the circuit. Formulating these observations mathematically by utilizing the charge conservation law, we obtain for the output of

the CDS circuitry:

$$V_{OUT,CDS}^{\phi_2} = V_{ref} + A_{CDS}\left(V_{in}^{\phi_1} - V_{in}^{\phi_2}\right) \tag{3.6.4}$$

$$+ (1 + A_{CDS}^{\sigma})(V_{bias,CDS}^{\phi_2} - V_{bias,CDS}^{\phi_1})$$

$$V_{OUT,CDS}^{\sigma,\phi_2} = V_{ref}^{\sigma} + A_{CDS}^{\sigma}\left(V_{in}^{\phi_1} - V_{in}^{\phi_2}\right) = V_{OUT,CDS}^{\phi_2} + \Delta V_{ref} \tag{3.6.5}$$

where $\Delta V_{ref}$ denotes small potential variations of the used reference voltage $V_{ref}$, which are, however, stress-independent (i.e., due to noise, drift etc.). Moreover, this configuration suppresses any input referred amplifier offsets, suppresses low-frequency amplifier noise and $V_{bias,CDS}$ voltage reference noise.

Keeping in mind that employing feedback reduces the circuit sensitivity to strain-induced changes, a pixel readout circuit concept that behaves mechanical stress independent is presented next. The proposed signal chain is illustrated in figure 3.11. Starting from the photodiode and ending at the sample and hold amplifier, the readout chain can be analyzed step-by-step. Here a 4T-pixel configuration is being used

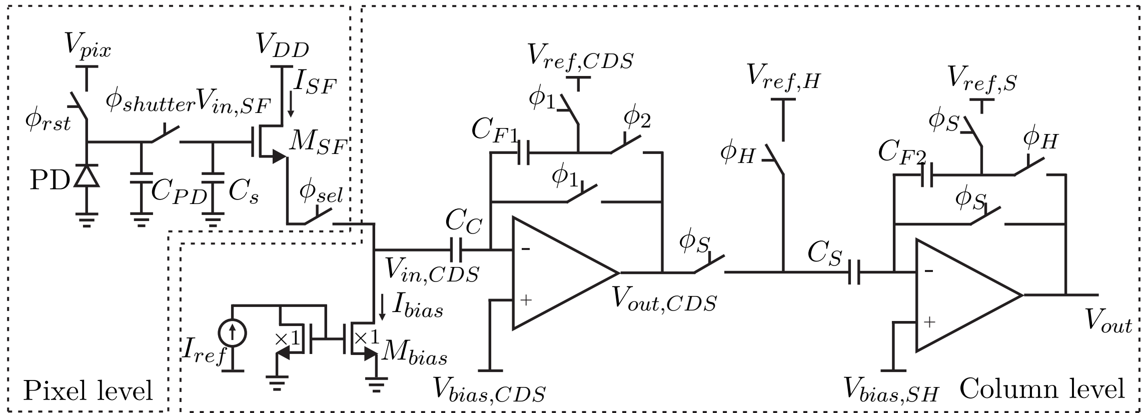


***Figure 3.11: Proposed pixel readout circuitry for mechanical stress independence.*** *The reference voltages/currents are assumed to be fed through external stress-independent voltage/current sources.*

and analyzed as shown in figure 3.11. Pixel arrays are read out columnwise, after connecting one row of the array to the column electronics using the select transistor. During the reset phase of the pixel array both the photodiode with its capacitance $C_{PD}$ and the storage capacitor $C_s$ are reset to the voltage $V_{pix}$ through the reset transistor $M_{RST}$, while holding the shutter transistor on. The resulting value is fed via

the source follower transistor $M_{SF}$ to the column readout circuitry. Subsequently an exposure period $t_{int}$ occurs during which charge is generated in the photodiode causing the voltage drop at its cathode. After setting the shutter transistor off, the reached voltage level $V_{PD}$ at the photodiode, which equals the input voltage $V_{in,M_{SF}}$ at the SF transistor $M_{SF}$ is given by:

$$V_{in,SF} = V_{PD} = V_{pix} - \frac{t_{int}\left(I_{PD} + I_{dark}\right)}{C_s + C_{PD}} \tag{3.6.6}$$

Taking into account the dependence of the photodiode characteristics (recall section 3.2) on uniaxial mechanical stress equation 3.6.6 can be rewritten for the stressed state:

$$V_{PD}^{\sigma} = V_{pix} - \frac{t_{int}\left(I_{PD}^{\sigma} + I_{dark}^{\sigma}\right)}{C_S + C_{PD}^{\sigma}} \tag{3.6.7}$$

$$V_{pix} - V_{PD}^{\sigma} = \alpha_{PD}\left(V_{pix} - V_{PD}\right) \tag{3.6.8}$$

where $\alpha_{PD}$ the coefficient which incorporates the changes caused by an applied mechanical stress on the dark current $I_{dark}^{\sigma}$ , as well as the capacitance $C_{PD}^{\sigma}$. The reached voltage level is being fed into the column readout circuits via the in-pixel source follower (SF), operation of which is also stress dependent as shown in subsection 3.5.2:

$$V_{out,SF}^{\sigma} = A_{SF}\left(V_{in,SF} - V_T - V_{DS,sat,M_{bias}}^{\sigma}\right) \tag{3.6.9}$$

$$V_{out,SF}^{\sigma} = V_{out,SF} - A_{SF}\Delta V_{DS,sat,M_{bias}}^{\sigma} = V_{out,SF} - \delta_{SF} \tag{3.6.10}$$

Utilizing the result of the CDS circuit output shown in equation (3.6.5):

$$V_{OUT,CDS}^{\sigma,\phi_2} = V_{ref,CDS}^{\sigma} + A_{CDS}^{\sigma}\left(V_{in,CDS}^{\phi_1} - V_{in,CDS}^{\phi_2}\right) \tag{3.6.11}$$

Observing now the whole signal chain starting from the photodiode and ending to the sample and hold amplifier we can write for the output signal in the stressed and unstressed condition using (3.6.5), (3.6.8), (3.6.10) and (3.6.11):

$$V_{OUT,CDS}^{\sigma,\phi_2} = V_{ref,CDS}^{\sigma} + (1 + \alpha_{PD})\frac{C_C}{C_F}A_{SF}\left(V_{pix} - V_{PD}\right) \tag{3.6.12}$$

$$\Rightarrow V^{\sigma,\phi_2}_{OUT,CDS} - V_{ref,CDS} = (1+\alpha_{PD})\left(V^{\sigma}_{OUT,CDS} - V_{ref,CDS}\right) + \Delta V_{ref,CDS} \quad (3.6.13)$$

where $\Delta V_{ref,CDS} = V^{\sigma}_{ref,CDS} - V_{ref,CDS}$ a small potential variation of the reference voltage source in the CDS circuitry, which are, however, stress-independent (i.e., due to noise, drift etc.) Equation (3.6.13) reveals five major facts: a) the use of the CDS technique suppresses the shift of the in-pixel SF output $\delta_{SF}$, which is caused due to the piezoresistive behavior of MOS transistors, b) amplification factors are based on ratios of device geometries, so that the overall strain-induced amplification changes are minimized in spite of potential larger strain-induced changes on device level (i.e. $C_C/C_F$) c) deploying negative feedback throughout the entire readout signal chain decreases the sensitivity on any parameter variations due to the application of mechanical stress and d) the employed SC-amplifier suppressed any input referred amplifier offsets and its strain-induced changes and e) any variations of the photodiode characteristics will appear at the output signal.

Taking into consideration the sample and hold circuit, which is also based on ratios of device geometries (sampling and holding capacitors), it can be shown that:

$$\begin{aligned} V^{\sigma}_{OUT} &= V_{ref,S} + A_{S/H}\left(V^{\phi_S}_{out,CDS} - V^{\phi_H}_{ref,H}\right) \\ &\quad + (1+A^{\sigma}_{S/H})(V^{\phi_H}_{bias,SH} - V^{\phi_S}_{bias,SH}) \\ V^{\sigma}_{OUT} &= V_{ref,S} + A_{S/H}\left[V_{ref,CDS} + (1+\alpha_{PD})A_{CDS}A_{SF}\left(V_{PD} - V_{pix}\right)\right. \\ &\quad \left. - V_{ref,H}\right] + \underbrace{A_{S/H}\left(\Delta V_{ref,H} + \Delta V_{ref,CDS}\right) + \Delta V_{ref,S}}_{stress-independent} \end{aligned} \quad (3.6.14)$$

where $\Delta V^{S}_{ref}$ and $\Delta V^{H}_{ref}$ are variations of the reference voltage sources (i.e., due to noise or drift) in the S/H circuitry, $A_{CDS} = C_C/C_{F1}$ and $A_{S/H} = C_S/C_{F2}$ is the closed loop CDS and S/H system gain respectively.

## 3.7 Synopsis

In this chapter, the strain-induced effects on the band structure of silicon have been modeled. Strain-induced energy band shifts as well as variations of the carrier effective masses have been theoretically treated. A model describing the intrinsic carrier

concentration under mechanical stress taking into account both these effects has been presented and the exponential dependence of dark current change of p-n junction based photodiodes has been shown. In the following, the piezoresistance theory on MOSFETs has been briefly presented and employed toward the modeling of analog circuits under mechanical stress. Fundamental analog circuits have been analyzed under the application of uniaxial mechanical stress and strain-induced changes on DC or AC characteristics (such as open-loop gain, $GB$ product, output DC voltage offset). The importance and benefits of negative feedback in analog circuits under stress has been underlined. A readout circuit which operation is designed to exhibit a minimized dependence on mechanical stress is proposed. The last section of the chapter has been dedicated to the analysis of the proposed CIS readout circuit.

# Chapter 4 - Simulation of Strain-Induced Effects on Devices and Circuits

In the following sections the strain-induced effects on the band structure of silicon will be simulated. Towards this goal, the mathematical description of the strain-induced changes of the energy band levels, the carrier effective masses and the carrier concentrations as presented in the previous section will be programmed using MATLAB®. Thereby, the strain-induced changes in the band structure of silicon and in the dark current of p-n junction based photodiodes will be elucidated through informative graphs and figures. In the following, the presented phenomenological model for uniaxially strained MOSFETs will be introduced into Cadence® IC Design tools using the intrinsic SKILL scripting language [Bar90] and a new, simple but accurate simulation technique will be employed. The technique will be first explained and results from its implementation on device level will be shown. The proposed simulation technique is published by the author in [DHG12] and [DHG13]. Next, basic analog circuit configurations as well as elaborate analog circuits deployed in CIS readout electronics will be simulated under mechanical stress deploying the presented technique. Goal of these investigations is the development of design guidelines for circuits operating mechanical stress independently.

## 4.1 Band Structure of Strained Silicon

Starting from the conduction band under mechanical stress, equations (3.1.3)-(3.1.5) are utilized for the computation of the shifts of the conduction band energy minima. The values used in this work are summarized in table 4.1. Figure 4.1 illustrates the linear shifts of the energy band minima under mechanical stress. Here the lifting of the star degeneracy along the $\Delta$ axes as mentioned in subsection 3.1.1 is made clear. The $\Delta_4$ valleys minima face a larger shift under uniaxial [110] mechanical stress. The results plotted in the upper figure do not contain the non-linear component of equation (3.1.6). As mentioned in subsection 3.1.2 this term is negligible in comparison with the energy shifts presented and thus can be ignored. To support this assumption the energy minima shifts of the $\Delta_2$ valleys with and without the non-linear component are plotted in figure 4.1c), verifying the validity of the assumption for moderate stress levels.

Next, equations (3.1.9) and (3.1.10) are used to compute the shifts of the valence band minima. The results are plotted in figure 4.1b). Here, only the two upper valence bands are taken into account as described in the previous chapter, namely the HH and

the LH bands. The splitting of the band minima under stress is elucidated through figure 4.1b). The HH (LH) band minimum increases (decreases) in energy under uniaxial [110] mechanical tensile stress, while the HH (LH) band minimum decreases (increases) in energy under compressive stress.

***Table 4.1: Deformation potential constants used in this work.*** *All values are given in eV* [FL96].

| Deformation potential | $\Xi_u^\Delta$ | $\Xi_u^L$ | $\Xi_d^\Delta$ | $\Xi_d^L$ | $a$ | $b$ | $d$ |
|---|---|---|---|---|---|---|---|
| Value [eV] | 10.5 | 18.0 | 1.1 | -7.0 | 2.1 | -2.33 | -4.75 |

Using the previous results, the strain-induced bandgap shift can be calculated as schematically shown in figure 4.1. The minimum distance between the conduction and valence band energy minima is computed, which underlines the fact that the bandgap narrows under uniaxial [110] mechanical stress independently of the stress direction (compression or tension) as shown in figure 4.1. The exact bandgap narrowing for moderate stress levels is shown in figure 4.2. The lower part of the figure shows the percentage change of the bandgap. For compressive stresses the bandgap narrows with 0.042 meV/MPa, while for tensile stresses it narrows with 0.044 meV/MPa.

Next to be introduced in the simulation model are the changes of the effective masses as described in the previous chapter. Equations (3.1.11)-(3.1.13) have been utilized to describe the strain-induced change of the $\Delta_2$ transverse (in-plane) effective masses with the piezo-coefficients obtained in [DUK$^+$07] and listed in table 4.2. Figure 4.3 illustrates the behaviour of the $\Delta_2$ effective masses. As discussed in the previous chapter (recall figure 3.3) the valence band DOS effective masses $m_{lh}$ and $m_{hh}$ tend to reach the same value for higher stresses. Due to the complexity of the valence band there is no unique representation for the DOS effective masses under stress known in literature. For our model we approximate the strain-induced shifts of the valence band DOS effective masses with a linear function as schematically shown in figure 4.4. Here the highly stressed region as reported in [Mat04] is assumed to be in the region $1 - 10$ GPa.

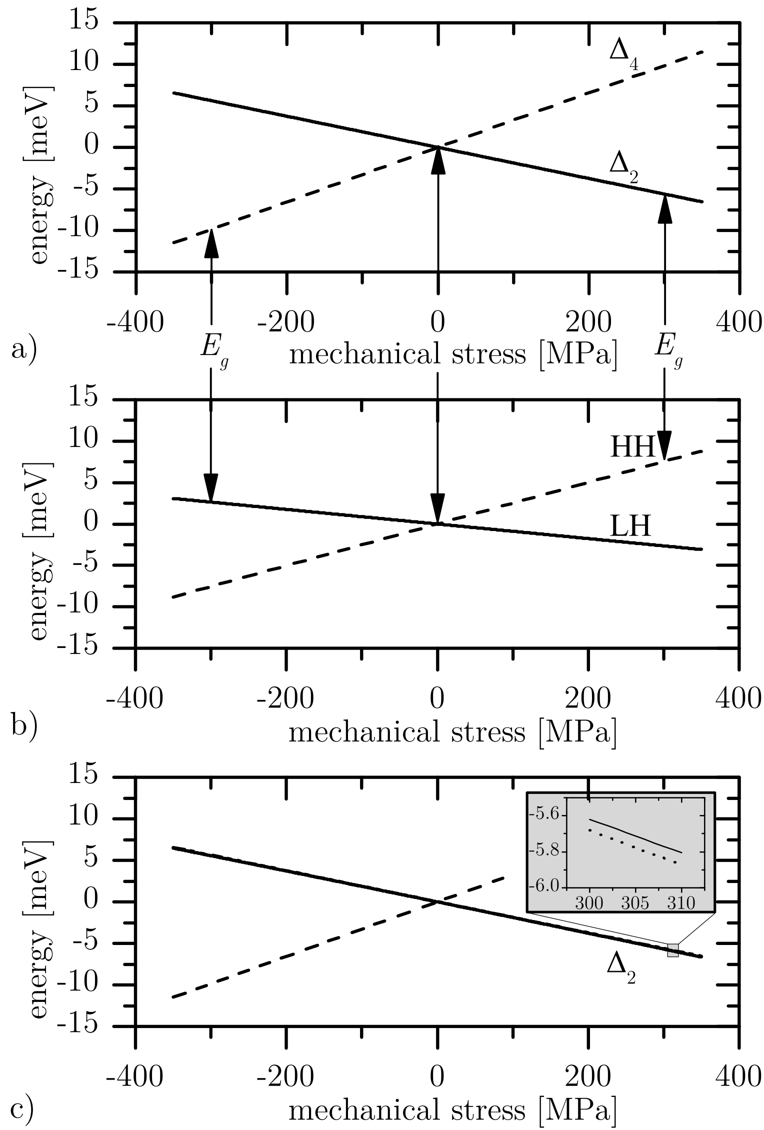


***Figure 4.1: Strain-induced shifts of the conduction and valence band minima.*** *a) Shift of the conduction band minima. The conduction band minima along the* $\Delta$ *axis are sixfold degenerate under relaxed conditions. Under the application of mechanical stress the sixfold degenerated minima split into a fourfold degenerated* $\Delta_4$ *and a twofold degenerated* $\Delta_2$ *minima. Note how the* $\Delta_4$ *(dashed line) minima face a larger shift in comparison to the* $\Delta_2$ *(solid line) minima under the application of* [110] *mechanical stress. b) Shift of the valence band minima. HH denote the heavy hole while LH denote the light hole band. c) Shift of the conduction band minima* $\Delta_2$ *with and without neglecting the non-linear shift (for comparison purposes). Positive stresses denote tension, while negative stresses denote compression. Note how the gap between the two bands (bandgap)* $E_g$ *is influenced.*

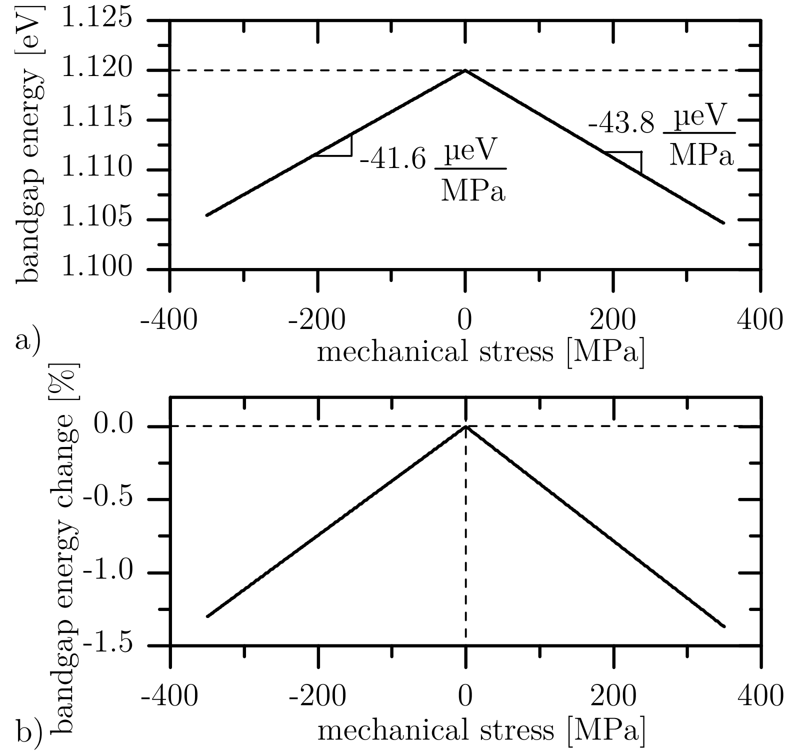


***Figure 4.2: Strain-induced narrowing of silicon bandgap.*** *a) Narrowing of silicon energy bandgap $E_g$ for both compressive and tensile uniaxial* [110] *mechanical stress. b) Percentage change of the bandgap energy. Positive stresses denote tension, while negative stresses denote compression.*

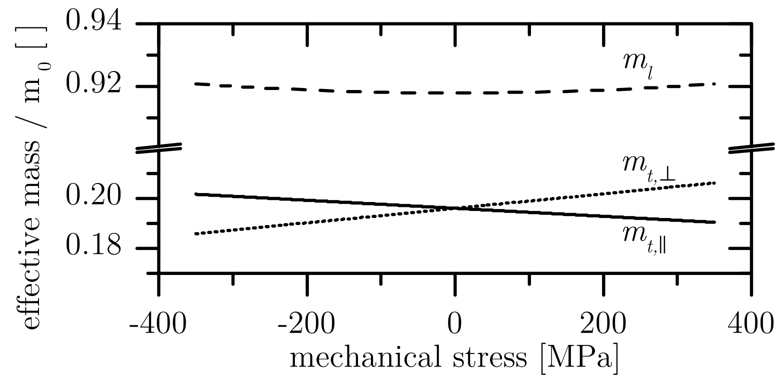


***Figure 4.3: Conduction band $\Delta_2$ effective masses under* [110] *uniaxial mechanical stress.*** *Note the larger shifts of $m_{t,\|}$ and $m_{t,\perp}$ and the slight change of the longitudinal (out-of-plane) $m_l$ effective mass under mechanical stress.*

***Table 4.2: $\Delta_2$ transverse and longitudinal effective masses piezoresistive coefficients used in this work.*** *Transverse masses are given in values of $m_0/GPa$, while for the longitudinal mass in $m_0/GPa^2$, where $m_0$ is the electron rest mass in kg.*

| Piezo-coefficient | $\pi_{t,\parallel}$ | $\pi_{t,\perp}$ | $\pi_l$ |
|---|---|---|---|
| Value | 0.016 | 0.029 | 0.0236 |

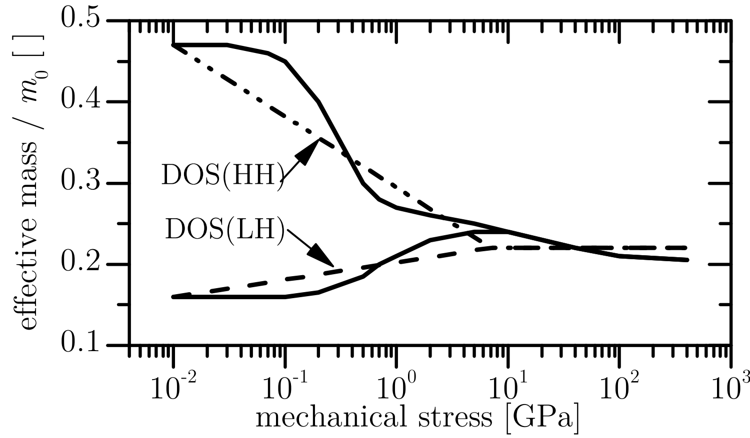


***Figure 4.4: Valence band DOS effective masses under [110] uniaxial mechanical stress.*** *The highly stressed region has been modeled around 1-10 GPa. The dashed lines represent the strain-induced change of the effective masses as included in the model.*

## 4.2 Strained p-n Junction Based Photodiode

After having introduced in the simulation platform the strain-induced changes of the band structure, the next step is to calculate the changes in the carrier concentrations. Using equation (3.2.9) the intrinsic carrier concentration change under mechanical stress can be computed. The results of the numerical computation are presented in figure 4.5. The figure elucidates the exponential change of the intrinsic carrier concentration. Very important to note here is the fact that $n_i$ faces larger changes for tensile stresses in our region of interest (±350 MPa). For compressive stresses the changes are significantly lower and also of the opposite sign. This is a very informative result, which will be used later while performing the experiments to support this theory.

The outcomes of the calculations will be used next towards the modeling of the dark current of a strained p-n junction based photodiode. First the assumption will be verified, that for higher reverse voltages the dominant part of the dark current is the is

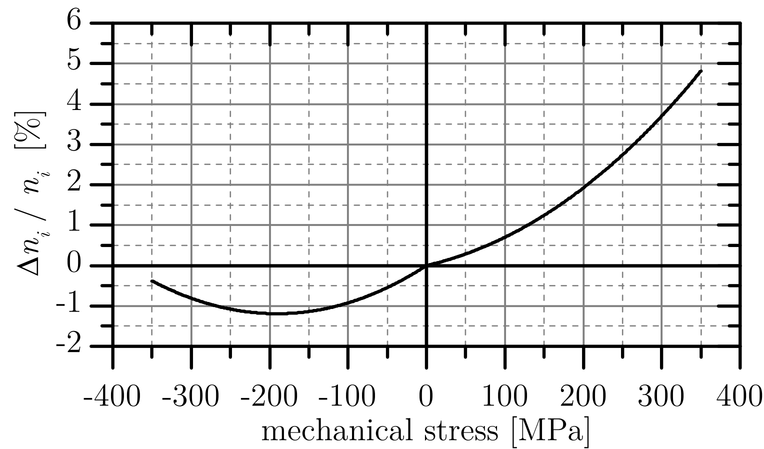


***Figure 4.5: Intrinsic carrier concentration under* [110] *uniaxial mechanical stress.*** *Note the exponential increase in the tensile region and the significantly smaller negative changes in the compressive region.*

the generation current within the depletion region. Using the values given in [Dur09] for the diodes of the same CMOS process used in this work, the diverse dark current components are calculated. The results are depicted in figure 4.6 and verify the fact that the generation current is the dominating mechanism. This verification will also take place experimentally in section 6.1.

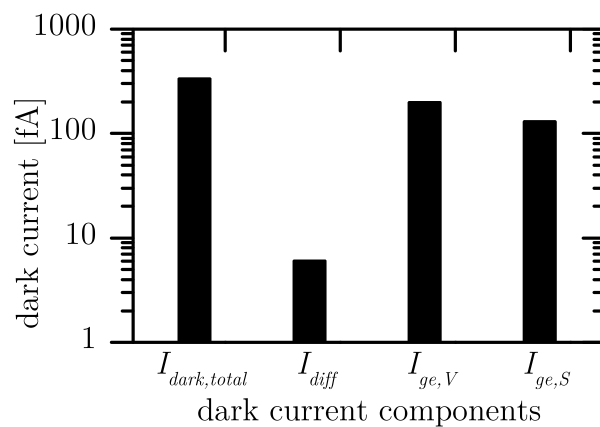


***Figure 4.6: Dark current components of an n-well/p square-shaped photodiode used in this work.*** *All data under reverse voltage $V_R = 2$ V. $I_{ge,V}$ and $I_{ge,S}$ denote the generation dark current components in the volume and at the surface of the semiconductor, respectively. $I_{diff}$ denotes the diffusion dark current component. Note that the dominating part is the total generation dark current $I_{ge,V} + I_{ge,S}$.*

Therefore, utilizing equation (3.2.10) the dark current of a p-n junction based photodiode under [110] uniaxial mechanical stress can be calculated and is depicted in

figure 4.7. Similarly, employing equation (3.2.14) the strain-induced changes of the p-n junction based photodiode capacitance under [110] uniaxial mechanical stress can be simulated and are depicted in figure 4.8.

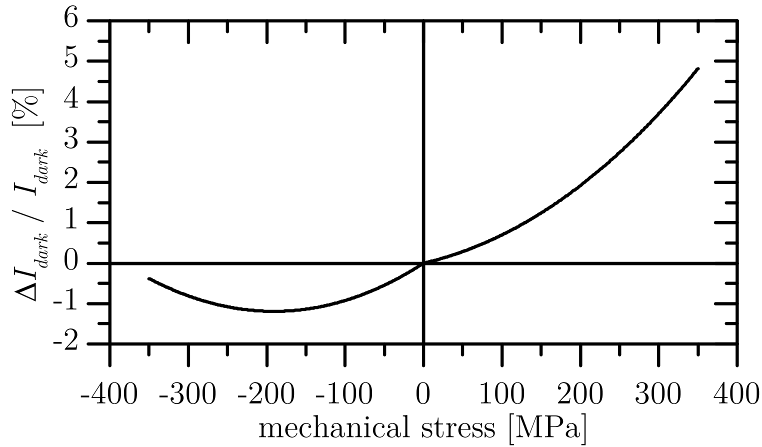


***Figure 4.7: Strain-induced dark current changes of p-n junction based photodiodes under [110] uniaxial mechanical stress.***

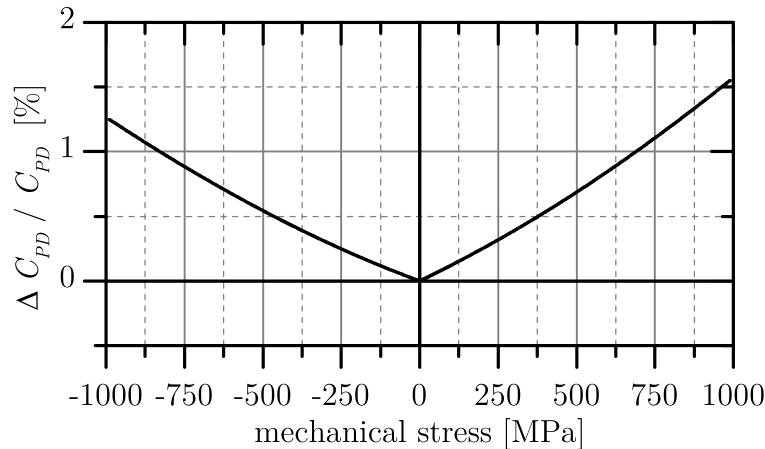


***Figure 4.8: Strain-induced changes of p-n junction based photodiodes under [110] uniaxial mechanical stress.***

## 4.3 Simulation Technique

It is of great importance for the analog IC designer to be able to simulate the designed circuits under different mechanical stresses and different channel orientations of the

transistors relative to the applied stress. In this section a novel, simple, but powerful simulation technique is presented that enables the simulation of mechanical stress on MOSFETs and circuits into Cadence® IC Design tools providing satisfying results when compared with the theoretical calculations.

As described in section 3.4 and using (3.4.3)-(3.4.5) a drain-source current change should be introduced by changing the mobility of the carriers, which in turn is linearly dependent on the applied mechanical stress through the piezoresistive coefficients (recall equation (3.4.4)). The technique proposed here is based on the observation that, in terms of figures as shown in equation (4.3.2), an equal change of the drain-source current of a MOS transistor can be achieved by changing the width of the transistor for the same amount as equation (3.4.3) dictates, instead of changing its effective mobility. The advantage of this approach is that the designer has a direct access to the geometrical dimensions of the device through the properties window of the simulator itself. Therefore, it is not needed to change the equations of the simulator computing the effective carrier mobility, which is not trivial and of course time-consuming. Moreover, callback routines programmed into the simulator using the intrinsic SKILL scripting language intervene and change automatically the user-defined transistor geometrical dimensions. The developed callback routines need two parameters to calculate the change of the width that has to be applied: a) the magnitude of the applied uniaxial stress $\sigma$ and b) the orientation of the transistor channel relative to the applied uniaxial stress. Thus the simulator is fed with a slightly changed width value, which virtually includes the effects of mechanical stress on the transistor DC characteristics. In other words, an extra virtual transistor $M_{sim}$ is connected in parallel to the one designed $M_{layout}$, in order to induce the current change observed under mechanical stress (figure 4.9a).

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{4.3.1}$$

$$\Rightarrow \frac{dI_D}{I_D} = \frac{d\mu}{\mu} = \frac{dW}{W} \tag{4.3.2}$$

As already mentioned in the previous chapter the strain-induced current changes are small for moderate stress levels ($< 10$ %) and hence the added transistor dimensions are much smaller in comparison to the real transistor widths. However, adding even a relatively small transistor in parallel to the real one (drawn / layouted), intro-

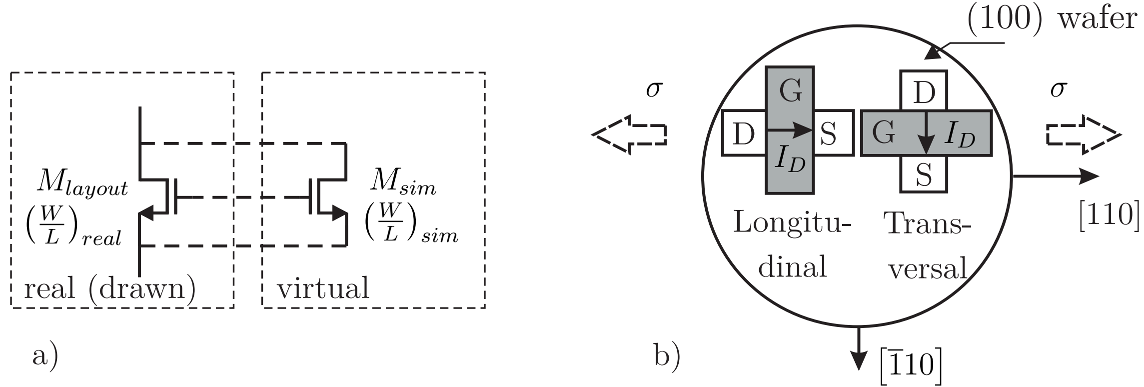


***Figure 4.9: Concept of the simulation technique.*** *a) Elucidation of the simulation concept. b) Typical layout orientations of on-chip MOS transistors.*

duces extra parasitic resistance and capacitance at its terminals, thus affecting its AC characteristics as well; a rather not desired situation. To resolve this issue, another callback routine is introduced, which actually stores the real width of the transistor $W_{layout}$. This value is then used for the calculation of the source/drain perimeter and area coefficients, which in turn are used to compute the parasitic capacitance of the device. Thus, two different widths are passed to the simulator: One (the real width of the device $W_{layout}$) used for the calculation of parasitic components and the other (a virtual width $W_{sim}$) used for the drain current calculations. As a result the parasitics are not scaled along with the change of the width of the device. Furthermore, the changed parasitic resistance due to the increased width could also introduce some errors. However, for long channel transistors (which are typical in analog design), the parasitic resistance change of the MOSFET is much smaller than its channel resistance and thus not significantly affecting its performance.

It is in general typical for a designer to layout transistors on-chip having either a 0° (longitudinal) or 90° (transversal) channel orientation relative to the main crystallographic direction of the wafer, as shown in figure 4.9b. Moreover, applying a uniaxial mechanical stress using either a 4-point bending apparatus or a cylindrical apparatus as the one used in this work, has as a result that the direction of the applied uniaxial stress is either parallel to or vertical to the channel orientation (current flow) of the layouted transistor on-chip. Therefore, we have two possible orientations and two transistor types, thus in total four different piezoresistive coefficients, which need to be determined experimentally and then introduced into the callback routines.

## 4.4 Basic Analog Circuits under Mechanical Stress

Using the described technique, the strain-induced drain current changes for the two different orientations (longitudinal-0° and transversal-90°) can be simulated as shown in figure 4.10. The slopes of the lines are the piezoresistive coefficients for each orientation and transistor type. Employing these transistors in circuits, the circuit operation under different stress levels can be simulated. In this section simulation results of a source follower (SF), of a differential and of a two-stage Miller amplifier are presented, which will be encountered in the final design of the developed CMOS image sensor. Based on these results optimization measures and design guidelines are discussed. For all coming graphs in this section the following convention is followed: a) Plots of the same column are results of the same circuit. b) T stands for a 90° (Transversal) channel orientation, while L stands for a 0° (Longitudinal) channel orientation w.r.t. the applied stress direction. An intuitive way to examine if the plotted parameter can become stress independent by adjusting the transistor orientations, is to spot if lines with the same color have opposite slopes. That way they will cross each other at the origin and will create a clearly visible "X" form on the plot. This technique can be used in the figure below, which reveals that a parallel connection of three pMOFETs, one longitudinal and two transversal, leads to less strain-induced current changes.

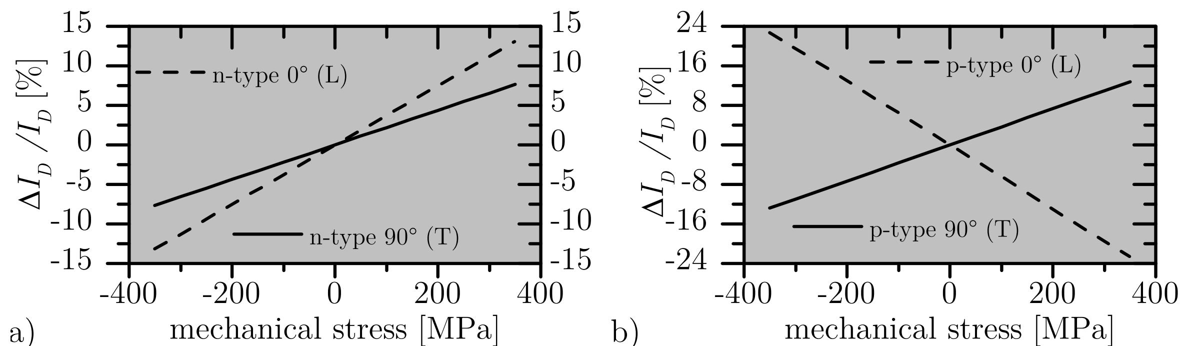


***Figure 4.10: Simulation of strain-induced drain current changes of MOS transistors under uniaxial* [110] *mechanical stress in two orientations.*** *a) n-type MOSFETs. b) p-type MOSFETs. L stands for longitudinal (0°) channel orientation, while T for transversal (90°) channel orientation w.r.t. the applied mechanical stress direction.*

The SF has been simulated for the two different configurations of figure 3.7. The

reference transistor $M_{bias}$ is set always in a transversal orientation (T-90°) setting the current on the SF transistor $M_{SF}$, which will be simulated for both orientations (L-0° and T-90°). Figure 4.11 shows the simulation results. The notation followed in the legend (TT or LT) stands for the orientations of the $M_{SF}$ and the $M_{bias}$ transistors respectively. The presented results are following the equations (3.5.5)-(3.5.25). Briefly,

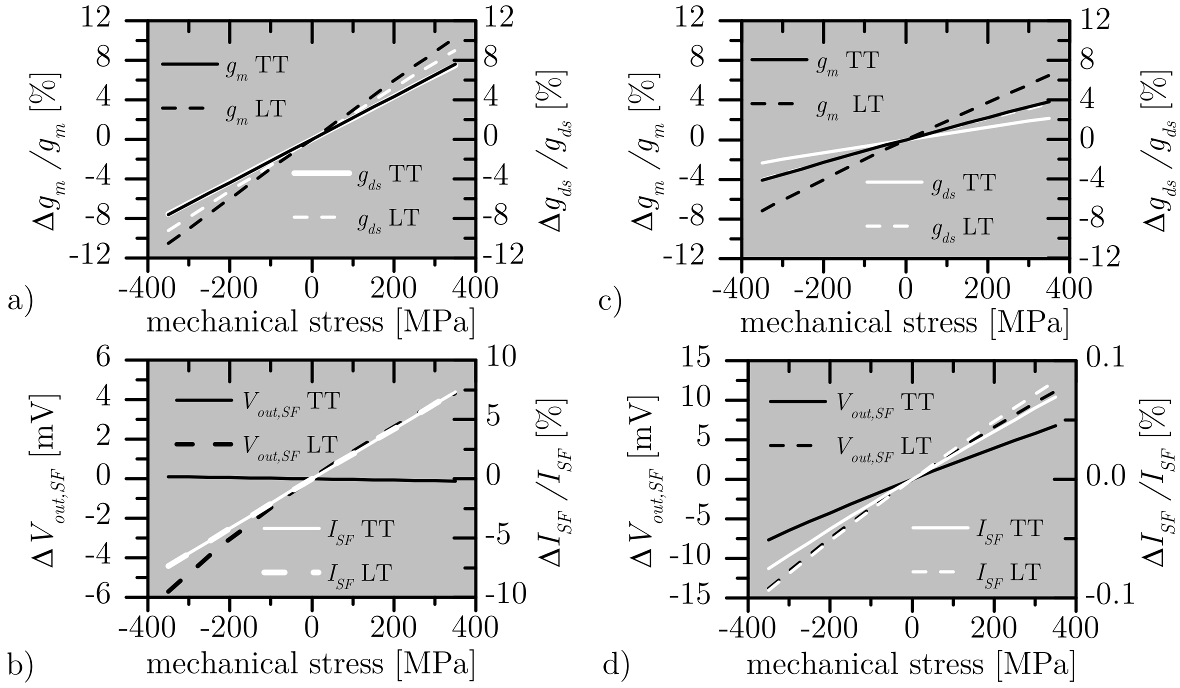


***Figure 4.11: Source follower simulation under mechanical stress.*** *a)-b) Constant voltage biasing. In a) transconductance $g_m$ and output-conductance $g_{ds}$ of $M_{SF}$ are shown. In b) the output voltage $V_{out,SF}$ and the current through $M_{SF}$ are shown. c)-d) Current mirror biasing. Same parameters are presented. Note that TT (LT) stands for transversal-transversal (longitudinal-transversal) orientations of $M_{SF}$ and $M_{bias}$ respectively.*

since the current is set constant in the second configuration a smaller change of $g_m$ and $g_{ds}$ of $M_{SF}$ is expected (compare figure 4.11a) and c)). However, while the current is constant for the current mirror biasing configuration the voltage shifts are larger compared to the constant voltage biasing configuration (compare figure 4.11b) and d)).

The differential amplifier has been simulated for the two different configurations of figure 3.9. Namely with n-type input MOSFETs and with a p-type input MOSFETs. All nMOSFETs of the circuits are kept in a transversal orientation (T-90°) while pMOSFETs will be simulated for both orientations (L-0° and T-90°). Figure

4.12 shows the simulation results. The notation followed in the legend (TT or LT) stands for the orientations of the pMOSFETs and the nMOSFETs.

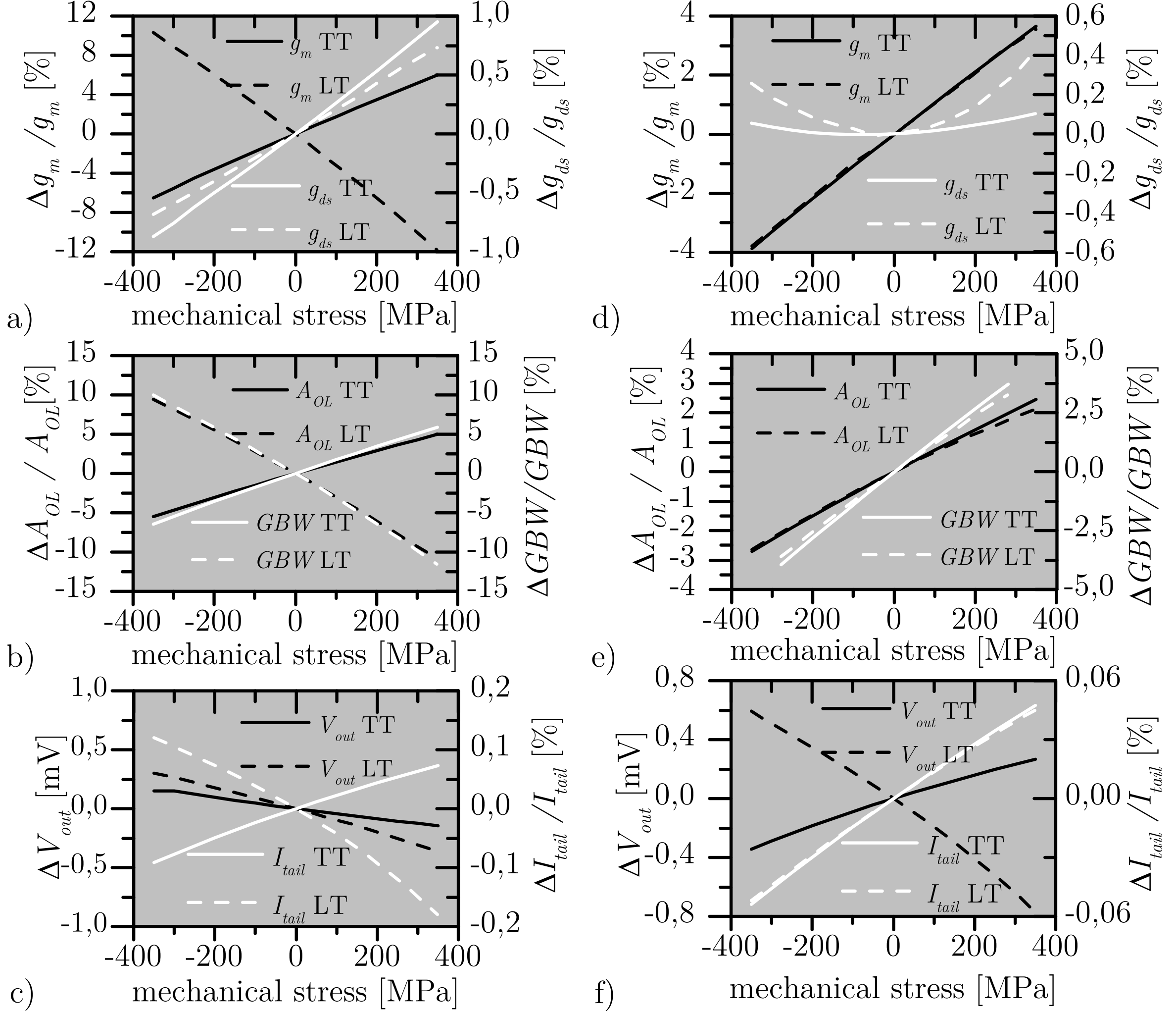


***Figure 4.12: Differential amplifier simulation under mechanical stress.*** *a)-c) With p-type input MOSFETs. In a) transconductance $g_m$ of $M_1$ and output conductance $g_{ds}$ of $M_4$ are shown. In b) the open-loop voltage gain $A_{OL}$ and the gain-bandwidth product (GBW) of the amplifier are shown. In c) the output voltage $V_{out}$ and the current through $M_{tail}$ are shown. d)-f) With n-type input MOSFETs. Same parameters are presented. Note that TT (LT) stands for transversal-transversal (longitudinal-transversal) orientations of pMOSFETs and nMOSFETs, respectively.*

In the presented results and employing the intuitive comprehension way described in the beginning of the section, it is clear that several parameters of the p-type input MOSFETs differential amplifier (figure 4.12a)-c)) can be optimized to be stress independent. Therefore, the designer can target a stress independent $A_{OL}$, $GBW$ or $I_{tail}$

by utilizing parallel connections of differently oriented p-type transistors. For the case of the n-type input MOSFETs differential amplifier (figure 4.12d)-f)) this optimization can be performed only for the DC output level shift $\Delta V_{out}$. In accordance with equation (3.5.46) if we set $I_{tail}$ as a stress independent quantity the strain-induced changes of the transconductance $g_m$ of $M_{in}$ show a square root dependence on the piezoresistive change $(1 + \pi_{M_1}\sigma)$ (figure 4.12a) and d)). The output load conductances $g_{ds,M_4}$ (figure 4.12a) and d)) in this case are almost constant since the current $I_{tail}$ through the differential amplifier is constant and is provided through a current mirror. By the pMOSFET input case, the open loop gain $A_{OL}$ and GBW face larger shifts when the pMOSFETs are designed in a longitudinal (0°) orientation due to their increased piezoresistive coefficient in that orientation (following the result of equation 3.5.53).

In the following the fundamental two-stage Miller amplifier has been simulated under mechanical stress, for the two different configurations of figure 3.9. Namely with n-type input MOSFETs and with a p-type input MOSFETs. Both circuits are utilizing two tail current mirrors for setting the current in each stage. All nMOSFETs of the circuits are kept in a transversal orientation (T-90°) while pMOSFETs will be simulated for both orientations (L-0° and T-90°). Both the stress-induced shifts in the DC and AC characteristics will be presented. Figure 4.13 shows the simulation results. The notation followed in the legend (TT or LT) stands for the orientations of the pMOSFETs and the nMOSFETs.

In the presented results and employing the intuitive comprehension way described before, it is clear that several parameters of the p-type as well as the n-type input MOSFETs Miller amplifier can be optimized to be stress independent. Therefore, the designer can target a stress independent $A_{OL}$ or $V_{out}$ by utilizing parallel connections of differently oriented p-type transistors. The transconductance $g_m$ of $M_1$ and output conductance $g_{ds}$ of $M_4$ face the same shifts as in the differential amplifier case and thus are not repeated here. Instead the transconductance $g_{m,M6}$ and output conductance $g_{ds,M6}$ of the second stage amplifying transistor are shown (figure 4.13a) and d)). Similarly as in the first stage, the $g_{m,M6}$ exhibits a square root dependence on the piezoresistive change $(1+\pi_{M_6}\sigma)$ (figure 4.12a) and d)). Worth to note is that the closed loop voltage amplification shows an extremely decreased sensitivity on the mechanical stress (figure 4.13b) and e)) . This result was anticipated after the discussion in section 3.6 described by equation (3.6.3). Hence, by utilizing feedback the strain-induced changes at device level are suppressed and the sensitivity of the overall circuit operation on mechanical stress is decreased. Utilizing these observations for optimizing the circuit towards

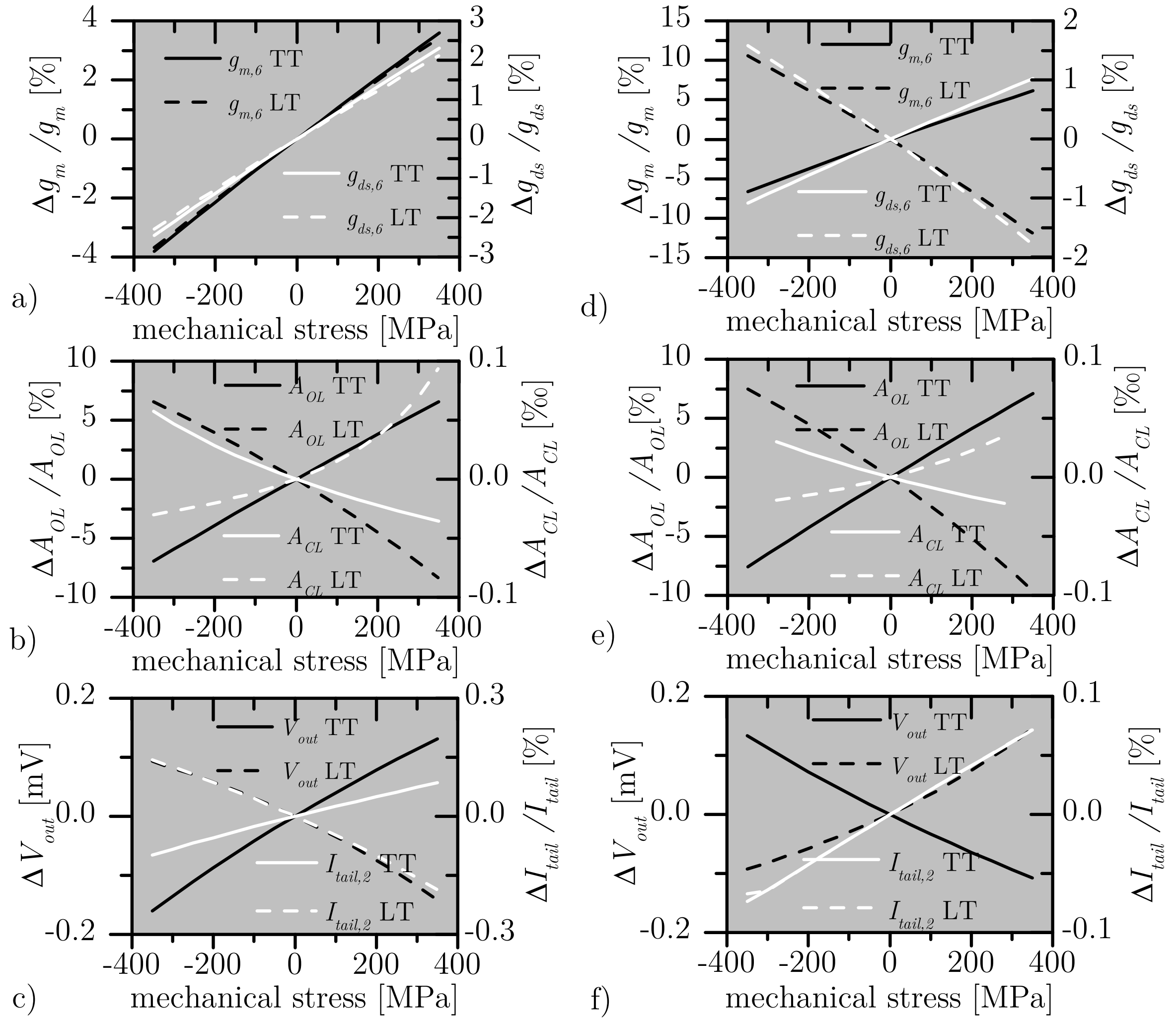


***Figure 4.13: Two-stage Miller amplifier simulation under mechanical stress.*** *a)-c) With p-type input MOSFETs. In a) transconductance $g_m$ of $M_6$ and output conductance $g_{ds}$ of $M_6$ are shown. In b) the open-loop $A_{OL}$ and closed loop $A_{CL}$ voltage gain of the amplifier are shown. In c) the output voltage $V_{out}$ and the current through $M_{tail,2}$ are shown. d)-f) With n-type input MOSFETs. Same parameters are presented. Note that TT (LT) stands for transversal-transversal (longitudinal-transversal) orientations of pMOSFETs and nMOSFETs, respectively.*

a stress independent operation, pMOSFETs can be placed in optimized orientations so as to reduce the stress-induced changes in the open-loop characteristics. The new optimized version has been simulated and the results are shown in figure 4.14. It is clear, that both current $I_{tail,2}$ as well $A_{OL}$ have become less stress-sensitive after the optimization step. Note the per mille scale on the graphic for tail current changes.

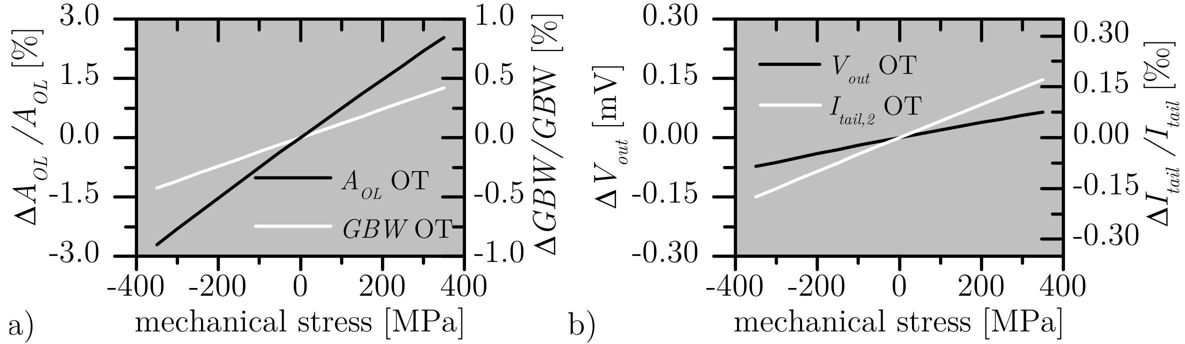


***Figure 4.14: Two-stage Miller amplifier simulation under mechanical stress after the optimization step.*** *With p-type input MOSFETs. a) The open-loop voltage gain $A_{OL}$ and the $GBW$ of the amplifier are shown. b) The output voltage shift $\Delta V_{out}$ and the current changes through $M_{tail,2}$ are shown. Note that OT stands for the optimized (O) orientations of pMOSFETs and transversal (T) orientation of nMOSFETs respectively.*

## 4.5 CIS Readout Circuits under Mechanical Stress

In order to verify the theoretical considerations of the compensating nature of the correlated double sampling circuit the proposed readout circuit has been simulated under different bending configurations. First, the stand-alone operation of the CDS amplifier itself has been investigated under stress. The amplifier designed here is a n-type input stage folded cascode, shown in figure 3.10. Similarly as before, shifts of both DC and AC characteristics are shown under stress in figure 4.15. Again here, it has been verified that the folded cascode amplifier in a negative feedback configuration (closed loop) under mechanical stress can be assumed a stress independent circuit. Note the per mille scale on the graphic for closed-loop gain changes. Moreover, the chosen orientation of the transistors forming the amplifier itself does not alter significantly its stress independence (compare black with white lines).

In the following, the CDS topology of figure 3.10 incorporating the folded cascode amplifier has been simulated. The CDS circuit is being first reset at 1.65 V and then its output evaluates at around 670 mV since the difference between the two applied input samples lies at 1 V. Both under tension or compression, the output level of the circuit does not change significantly as shown in figure 4.16b)-d). The simulation results presented in figure 4.16 verify our design guideline, that negative feedback applied to the CDS circuit renders the circuit less sensitive to mechanical stress according to equation (3.6.3).

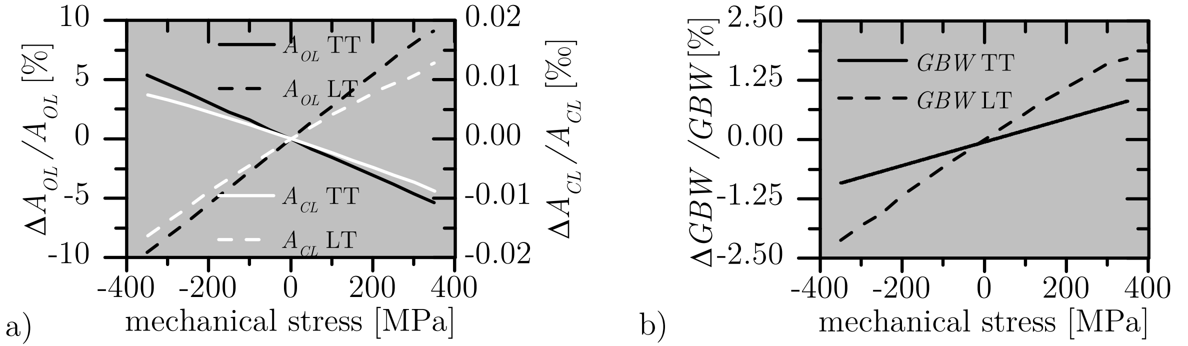


***Figure 4.15: Folded cascode amplifier simulation under mechanical stress.*** *a) The open-loop gain changes $\Delta A_{OL}$ and the closed loop voltage gain changes $\Delta A_{CL}$ under mechanical stress are shown. b) The strain-induced changes of the $GB$ of the amplifier are shown. Note that TT (LT) stands for transversal-transversal (longitudinal-transversal) orientations of pMOSFETs and nMOSFETs, respectively.*

Next, the image sensor readout electronics chain, has been also simulated with and without utilizing the CDS concept. That way the design guideline on the compensation of the strain-induced effects on the in-pixel source follower through the CDS technique can be investigated. Figure 4.17 illustrates the simulation results. In figure 4.17a) the overall response is shown, where the pixel PD and the readout electronics are reset ($t_{reset}$), thus both the in-pixel SF as well as the CDS circuit output are brought to a reference constant level (reset level). Then the exposure time (or integration time $t_{int}$) follows, where the PD is discharged and thus the in-pixel SF output is decreasing. Note that the CDS circuit inverts the output signal when compared to the SF output. A $t_{shutter}$ period where the value is held at the output follows at the end. The zoom-in figures reveal the fact that the stress-induced changes directly after the SF reach up to 8-9 mV for moderate stress levels, while after the CDS circuit the strain effects are compensated. The CDS output faces $< 0.5$ mV shifts as shown in figure 4.17c). Figure 4.17c) validates the compensation mechanism for for both tensile as well compressive

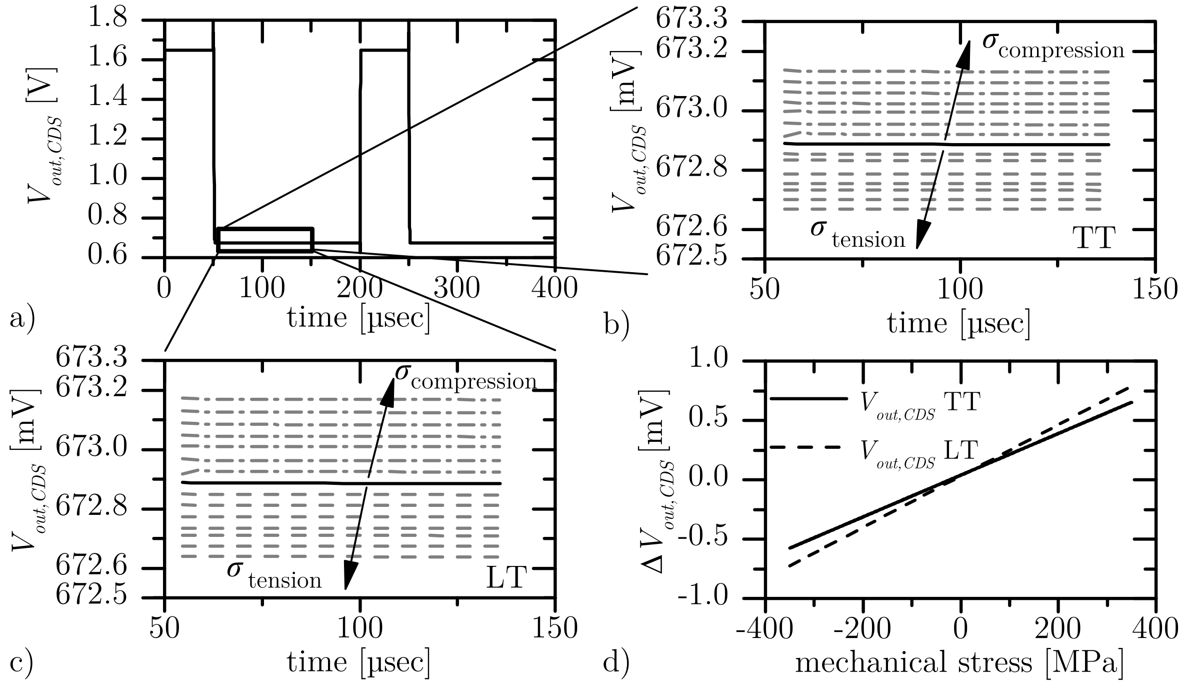


***Figure 4.16: CDS circuit simulation under mechanical stress.*** *a) Transient CDS response $V_{out,CDS}$ under mechanical stress. b) Zoom-in: Strain-induced shifts of the $V_{out,CDS}$ of the amplifier in a TT configuration. c) Zoom-in: Strain-induced shifts of the $V_{out,CDS}$ of the amplifier in a LT configuration. d) Strain-induced changes of $V_{out,CDS}$. Note that TT (LT) stands for transversal-transversal (longitudinal-transversal) orientations of pMOSFETs and nMOSFETs respectively.*

stress, verifying our proposed design guideline i.e., the use of a CDS amplifier to readout the pixel allows a partial compensation of the strain-induced shifts on the in-pixel source follower.

Having verified the compensation techniques for stress minimization in the readout electronics for image sensors using the proposed simulation technique, another vital circuit for any CMOS image sensor to be simulated is a bandgap reference (BGR). In general a bandgap reference combines the complementary-to-absolute-temperature (CTAT) behavior of a diode forward voltage drop with the proportional-to-absolute-temperature (PTAT) behavior of a resistor voltage to form a constant voltage reference (a bandgap reference) that does not vary much with temperature [Bak10]. A widely used bandgap topology shown in figure 5.4 utilizes a self-biased amplifier to hold the voltage at nodes A and B equal by regulating the currents in both branches. The circuit has been simulated under mechanical stress and the results are presented in figure 4.18. Here the mismatch of the input transistors of the deployed transimpedance amplifier

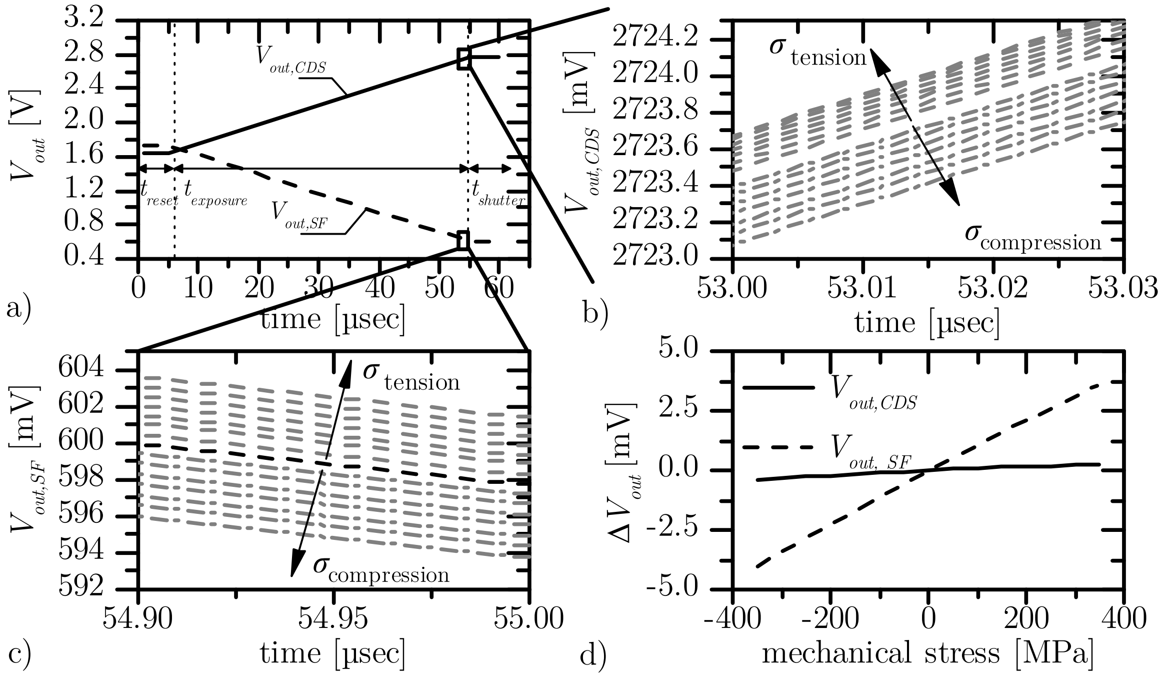


***Figure 4.17:*** *Image sensor readout circuit simulation under mechanical stress. a) Transient in-pixel SF $V_{out,SF}$ and CDS $V_{out,CDS}$ response under mechanical stress. b) Zoom-in: Strain-induced shifts of the pixel output $V_{out,SF}$ (before CDS is performed). c) Zoom-in: Strain-induced shifts of the readout circuit output $V_{out,CDS}$ after CDS is performed . d) Strain-induced changes of the pixel output $V_{out,SF}$ and the readout circuitry output $V_{out,CDS}$ after CDS is performed. Note the compensation of strain-induced shifts after the CDS circuit.*

plays a critical role in the reference voltage of the circuit, since the input offset voltage $V_{offset}$ of the amplifier will corrupt the loop around the diodes and the resistor $R_{PTAT}$. Thus the simulation is performed for positive and negative mismatches on the input transistors i.e., positive and negative offset voltages $V_{offset}$. As the simulation reveals, the application of mechanical stress actually amplifies the mismatch-induced drain-current difference in the two main branches. That way, the application of mechanical stress does not shift the temperature characteristic in a predefined manner, but depends on the initial mismatch on the input transistor of the utilized operational amplifier. Moreover, the absolute change of the output voltage for different mismatches is different under the two cases (18 mV vs. 35 mV).

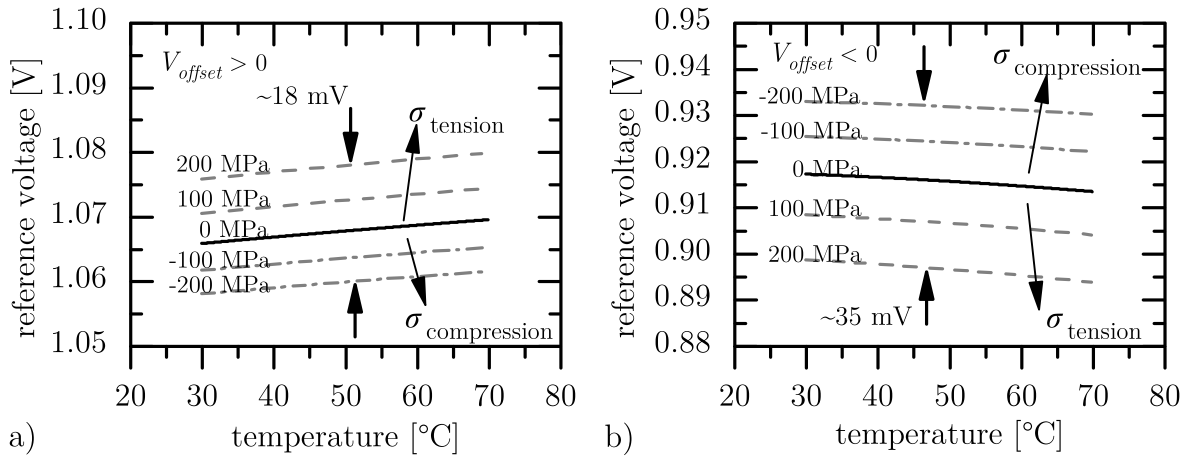


***Figure 4.18: Simulation of strain-induced changes of the bandgap voltage reference circuit under uniaxial* [110] *mechanical stress, varying temperature and different input offset voltage* $\mathbf{V_{offset}}$ *of the amplifier.*** *Solid black lines represent data under relaxed conditions, while dashed gray lines represent data under uniaxially strained conditions. Note the different trends of the shift of the characteristic among the two simulations for the same mechanical stress direction but for different mismatches.*

## 4.6 Synopsis

In this chapter, the strain-induced effects on the band structure of silicon have been simulated. Strain-induced energy band shifts as well as variations of the carrier effective masses have been introduced in the simulation. The model presented in chapter 3 describing the intrinsic carrier concentration under mechanical stress has been introduced in the simulation platform and the strain-induced dark current changes of p-n junction based photodiodes has been calculated. In the following, the piezoresistance theory on uniaxially strained MOSFETs has been introduced into Cadence® IC Design tools utilizing the presented simple but accurate simulation technique. Next, fundamental analog circuit configurations as well as elaborate analog circuits deployed in CIS readout electronics have been simulated under mechanical stress deploying the presented technique. The proposed readout circuit which operation is designed to exhibit a minimized dependence on mechanical stress is simulated and its stress independence is verified. The importance and benefits of negative feedback in analog circuits under stress has been verified. The development of design guidelines for circuits operating mechanical stress independently has been the goal of this chapter. These guidelines will be verified experimentally in chapter 6 and will be all listed in chapter 7.

# Chapter 5 - Experimental Methods

In this chapter the hardware and software methods utilized in this work will be briefly presented. In section 5.1 the designed test structures featuring integrated devices and circuits to investigate the presented theory will be put forward. The thinning and encapsulation process of the fabricated silicon chips appear in section 5.2. Section 5.3 introduces the diverse measurement setups used throughout the experimental part of this work. Both the mechanical setups utilized for bending of the flexible silicon chips-in-foil as well as the measurement setups for electrical and electro-optical measurements will be shown. Section 5.4 summarizes and closes this chapter. The presented methods have been published by the author in [DHG13] and [HMD+12].

## 5.1 Fabricated Test Chips

Before presenting the experimental results in the next chapter, an overview of the fabricated chips will be given first. Table 5.1 summarizes the designed chips along with a description of the integrated devices and circuits as well as the purpose to be served by each chip. The IC design was performed using Cadence® IC Design and the test chips were fabricated using the in-house 0.35 µm CMOS process of the Fraunhofer Institute IMS, Duisburg.

The test chips T95265A and T95265C incorporate MOSFETs, capacitors and p-n junction based photodiodes, which will be electrically and optically characterized under mechanical stress. Figure 5.1 illustrates the geometries of the MOS transistors integrated on the chips. Both short-channel as well as long-channel MOSFETs have been fabricated and the presented geometries hold for both n- as well as pMOSFETs. The transistors on each chip share the same gate and source connections, which allows us to save area through reduction of the number of the chip pads needed. All transistors have been drawn in two orientations, namely 0° (longitudinal) and 90° (transversal) with respect to the [110] crystallographic direction. The designation convention followed for MOSFETs states first the type of the transistor, then its $W/L$ ratio and at last its 0° or 90° orientation w.r.t. the stress direction.

The photodiodes integrated on these test chips are of two types, as already mentioned in section 3.2 in figure 3.4, namely the n+/p and n-well/p photodiodes. Figure 5.2 shows the different shapes of the photodiodes designed. Next to the square- and the array-shaped photodiodes, photodiodes with a large number of parallel stripes (or fingers) are drawn. The latter allow us to investigate potential orientation dependence

of the strain-induced effects on the photodiode characteristics. Table 5.2 lists the areas and the perimeters of each photodiode. The naming convention followed for the photodiodes states first the type of the photodiode and then its geometry (Square, Array, Finger with 0° or 90° orientation w.r.t. stress direction respectively).

***Table 5.1: Overview of the fabricated test chips used in this work.***

| Chip ID | Integration | Investigation purpose |
|---|---|---|
| T95265A | n-and pMOSFETs<br>p-n junction based PDs<br>MOS capacitors | Piezoresistivity in MOSFETs<br>Strain-induced effects on photodiodes<br>Strain-induced effects on capacitors |
| T95265B | Pixel matrix based on nMOSFETs<br>CDS circuits vs. orientation | Strain-induced effects on image test sensors<br>Strain-induced effects on readout circuits |
| T95265C | n-and pMOSFETs<br>p-n junction based PDs | Piezoresistivity in MOSFETs<br>Strain-induced effects on photodiodes |
| T95265D | Bandgap reference | Strain-induced effects on reference circuits |
| T95265E | Pixel matrix based on pMOSFETs with the proposed readout circuitry | Test of the proposed readout circuitry before integrating in the final image sensor design |
| T95265F | CMOS image sensor | Demonstration purposes |

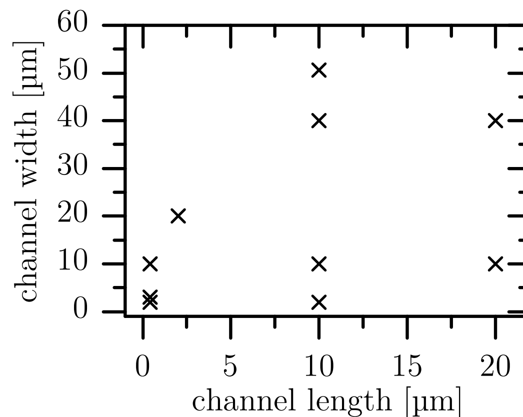


***Figure 5.1: Overview of the fabricated MOSFET channel geometries.*** *Both n- as well as pMOSFETs with the presented geometries have been fabricated.*

The capacitors integrated on T95265A test chip are MOS based capacitors with a heavily doped n+ polysilicon gate. However, capacitors of this type in the process,

***Table 5.2: Overview of the geometry characteristics of the fabricated photodiodes.***

| PD Type | Area [µm²] | | | Perimeter [µm] | | |
|---|---|---|---|---|---|---|
| | Square | Array | Finger | Square | Array | Finger |
| n+/p | 122500 | 90000 | 125333 | 1400 | 18000 | 246725.6 |
| n-well/p | 122500 | 89820 | 131516 | 1400 | 17982 | 124610.2 |

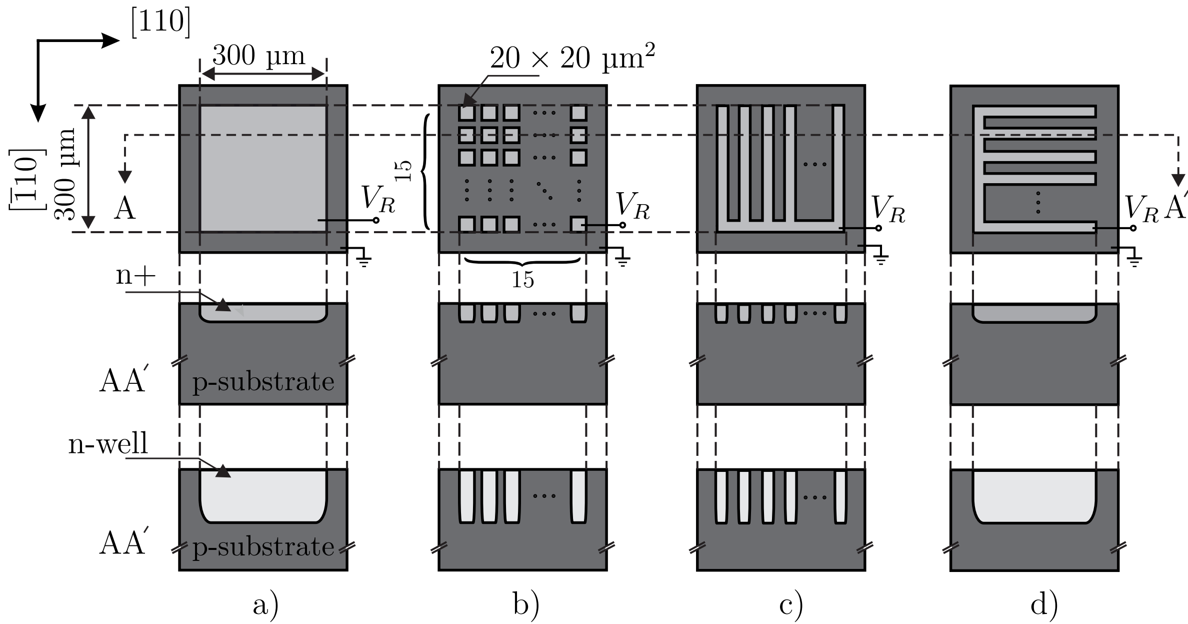


***Figure 5.2: Overview of the fabricated p-n junction based photodiodes.*** *a) Square-shaped photodiode* 300 × 300 *µm*². *b)* 15 × 15 *array-shaped photodiode. Each photodiode element has an area of* 20 × 20*µm*² *c) Finger-shaped photodiode with a* 90° *substrate orientation. d) Finger-shaped photodiode with a* 0° *substrate orientation. Both n+/p as well as n-well/p photodiodes with the presented shapes have been fabricated.* $V_R$ *denotes the terminal where the reverse voltage is applied. Note the different depths of the n-type doping implantations.*

deviate from the ideal case, as was mentioned in section 2.2.4. Their response is nearly voltage independent, since their operation remains over the applied voltage ranges in the accumulation region (recall table 2.2). The drawn geometries and the naming convention followed for integrated capacitors are similar to the photodiodes ones (Square, Array, Finger with 0° or 90° orientation w.r.t. stress direction respectively).

Chip T95265B is the first fabricated chip integrating a test CMOS image sensor and analog circuits to be characterized under mechanical stress. For this reason, an SC-

amplifier configured as a correlated double sampling circuit similar to the one shown in figure 3.10 has been designed and layouted on-chip with four combinations of pMOSFET and nMOSFET orientations. All nMOSFETs were drawn with the same orientation and were either vertical or horizontal to the channels of pMOSFETs. The test CIS incorporated in the T95265B test chip features a $15 \times 15$ pixel array (pixel matrix). However only the middle part is light sensitive, which consists of a $4 \times 5$ active pixel array as illustrated in figure 5.3a). Each pixel features different photodiode geometries to investigate potential dependencies of strain-induced effects on photodiode shape or orientation. The remaining dummy pixels around the active pixel matrix serve the purpose of etch guards [Has01], while maximizing matching. The active pixels are being readout through column readout circuits based on two different readout paths. The first is based on the CDS circuit shown before. The second is a p-type source follower based column readout scheme and serves for comparison purposes of the stress sensitivity among the two readout ways. The outputs of the two readout chains are multiplexed to an output buffer, which drives the chip pad. The complete circuit schematic is shown in figure 5.3b. Both amplifiers utilized are based on a folded cascode topology [Bak10], but with different drive capability and slew rate.

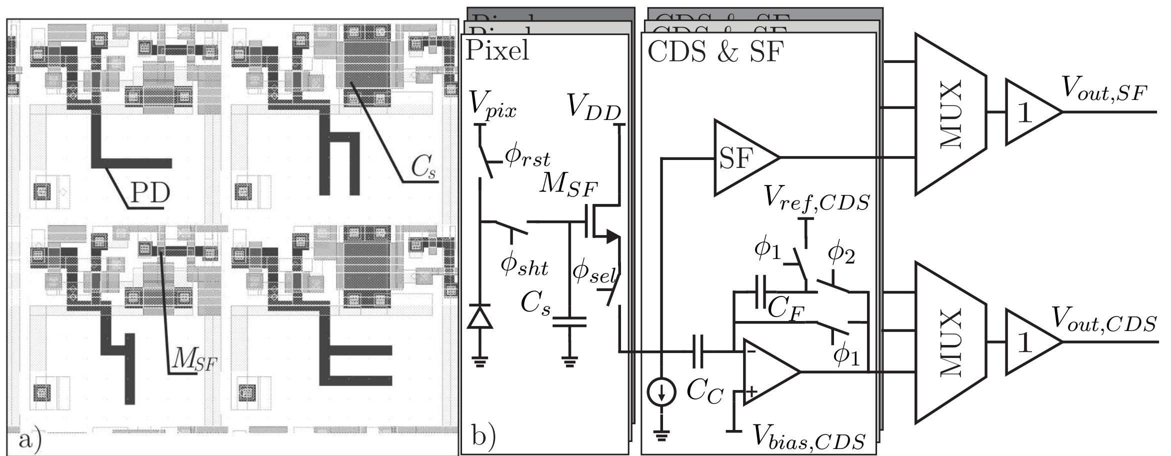


***Figure 5.3: Overview of T95265B test chip.*** *a) Layout of the $4 \times 5$ active pixel matrix. Note the different shapes, orientations and photodiodes types drawn. All in-pixel storage nodes $C_s$ have been implemented using an n-type MOSFET based capacitor. b) Complete schematic of the deployed readout circuits. The two readout ways are multiplexed and fed into a unity-gain negative feedback operational amplifier. $\phi_1$, $\phi_2$, $\phi_{sel}$, $\phi_{sht}$ and $\phi_{rst}$ are digital signals controlling the exposure and readout process.*

Chip T95265C integrates MOS transistors with round gate shapes. The idea of round gate MOS transistors is to achieve a lower piezoresistive dependence of the drain current of pMOSFETs, as will be presented and explained in the next chapter. There are two layout types of circular transistors, one is a donut-shaped and one a circle-shaped transistor, as illustrated in figure 5.4. The rest of the area was covered with photodiodes, similar to T95265A, so as obtain more samples for the forthcoming experiments.

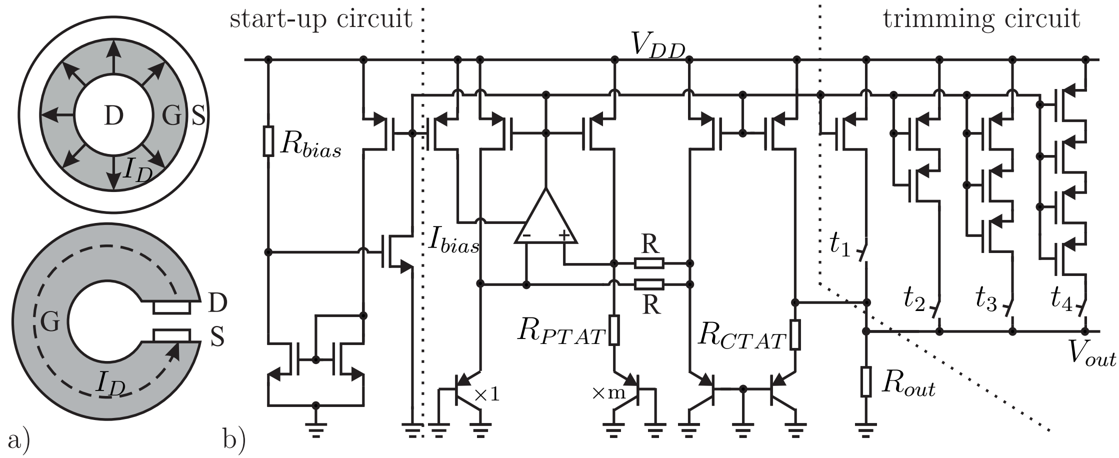


***Figure 5.4: Devices and circuits integrated in the T95265C and T95265D test chips.*** *a) Layout of a donut-shaped and a circle-shaped pMOSFET on the T95265C chip. b) Bandgap reference (BGR) schematic integrated in T95265D chip.*

Chip T95265D integrates a voltage reference circuit based on a BGR topology, shown in figure 5.4. Moreover, for this topology a start-up circuit shown on the left of figure 5.4 is required. To improve the accuracy of the circuits over all process corners, a trimming circuit is additionally needed, shown on the right part of the figure.

Chip T95265E incorporates two $12 \times 10$ pixel arrays (pixel matrices). However, only the middle part of each matrix, similar to T95265A, is light sensitive, which consists of a $4 \times 6$ active pixel array. Each pixel features a p-type reset and a p-type shutter transistor. The one pixel matrix features an in-pixel MOS capacitor, while the other a nMOSFET based capacitor. The remaining dummy pixels around the active pixel matrix serve the purpose of etch guards [Has01], while improving matching. The active pixels are being readout using column readout circuits. The first stage is a CDS circuit, as presented before, followed by a S/H SC amplifier ($2^{nd}$ stage) as shown in figure 3.11. The outputs of the two pixel arrays are each multiplexed using a shift-register to an output buffer, which drives the chip output pads. The complete circuit schematic is

shown in figure 5.5. All amplifiers utilized are based on a folded cascode topology [Bak10], but with different drive capability and slew rate. The purpose of this test chip was to evaluate the functionality of the proposed readout chain, which should be used in the final design of the CMOS image sensor designed within the scope of this work. This test chip is designed using all guidelines for minimizing mechanical stress dependence of the readout circuits, as they will be presented in chapter 7.

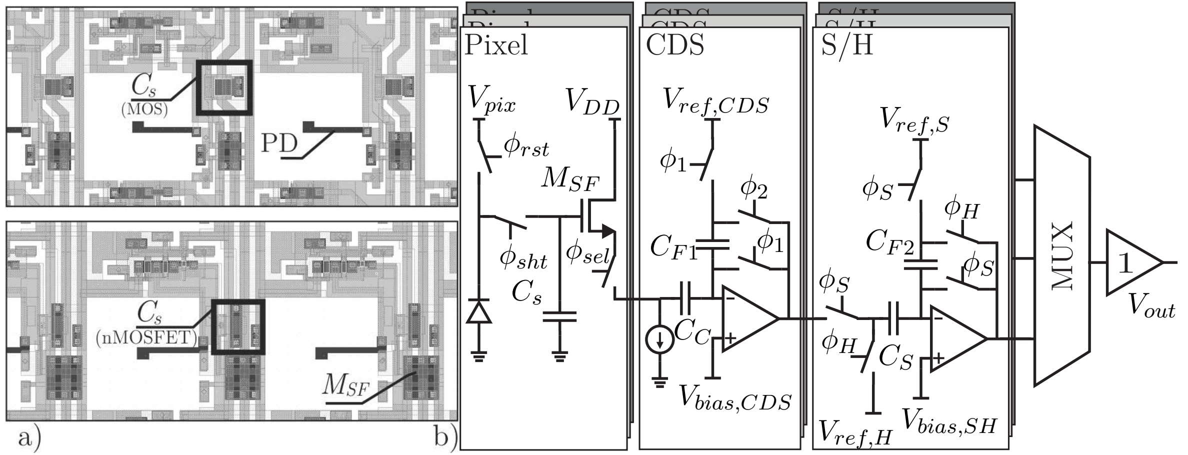


***Figure 5.5: Overview of T95265E test chip.*** *a) The in-pixel storage node $C_s$ is based on a MOS capacitor for the one pixel matrix (upper pixel layout), while on a nMOSFET based capacitor for the other (lower pixel layout). b) Complete schematic of the deployed readout circuits.*

Chip T95265F incorporates a full design of a CMOS image sensor to be used in bendable applications. The image sensor features the verified and tested pixel design and the readout chain of T96265E test chip. The T95265F CIS employs vertical and horizontal access circuitry and can implement both rolling as well as global shutter readout. The pixel matrix consists of $1200 \times 200$ light-sensitive pixels. Additional pixel rows and columns are designed around the pixel matrix as dummy blocks. Moreover, the CIS features metal covered pixel rows (light-shielded) to be used for calibration purposes and FPN removal. A differential SC output buffer with high slew rate and active cascodes for gain enhancement is employed for driving the output pads at a minimum of a 20 MHz data clock. This CMOS image sensor chip is designed using all guidelines for minimizing mechanical stress dependence of the readout circuits, as they will be presented in chapter 7. Closer information about the design and layout of the CIS developed within the scope of this work for demonstration purposes will be given in chapter 7, while detailed information can be found in [Kle12].

## 5.2 Thinning and Encapsulation Processes

In this section the dicing by thinning (DbyT) process is briefly described and the encapsulation process of the produced ultra-thin chips in PI foil is presented. In order to circumvent the traditional wafer dicing techniques based on wafer sawing, the DbyT process first introduced by [LKSA01] is employed in this work. Here, dry-etched trenches are opened around every die in the silicon substrate. Next, the wafer backside is thinned down until the point of reaching the trenches and thus singulating each die. Thus, dicing is performed avoiding any wafer sawing, which leads to a tremendous increase in the die strength (w.r.t. die fracture stresses) when compared with other dicing techniques as presented in [SBE+05]. In order to be able to perform the DbyT process with higher yield as well as for easier mechanical handling of the final ultra-thin chips, the minimum chip area is kept at around 5 mm × 5 mm.

During the first step of the thinning process, 25 µm deep and 100 µm wide trenches are etched into the wafer around the 5 mm × 5 mm chip area by means of Reactive Ion Etching. Afterwards, a glass carrier substrate is attached to the wafer front side using wax. Backside thinning is carried out by lapping with variable removal rates. Chemical mechanical polishing (CMP) for surface planarization follows and the process ends with a wet etching step in a mixture of hydrofluoric acid, nitric acid and acetic acid (HNA mixture) for surface damage removal. The latter stress relief step is essential, so as to remove any surface defects introduced by CMP, since micro cracks present on the die surface with dramatically lower its breaking strength. By removing the backside volume of the silicon wafer the trenches are reached and opened. At this point the etching step is stopped, therefore the initial trench depth defines the final chip thickness. Now, the thin chips are singulated and can be detached from the glass carrier substrate by dissolving the wax in heated isopropanol. The process steps are depicted in figure 5.6 and have been carried out in the Central Technology Laboratory of the Institute of Materials in Electrical Engineering (IWE1) in RWTH-Aachen.

In order to mechanically support the ultra-thin silicon chips as well to provide the necessary electrical connections on the chip, a flexible encapsulation is needed. The encapsulation process of the chip in very thin and thus flexible foils based on a spin-on PI (PI2611 from HD Microsystems) is illustrated in figure 5.7. During the first step, a 5 µm thin PI layer is spun on a four inch carrier wafer with a deposited aluminum-titanium sacrificial layer. The PI layer is subsequently patterned by photolithography and wet etching and cured. Thereafter, a 1 µm thin PI layer is spun on. The layer is

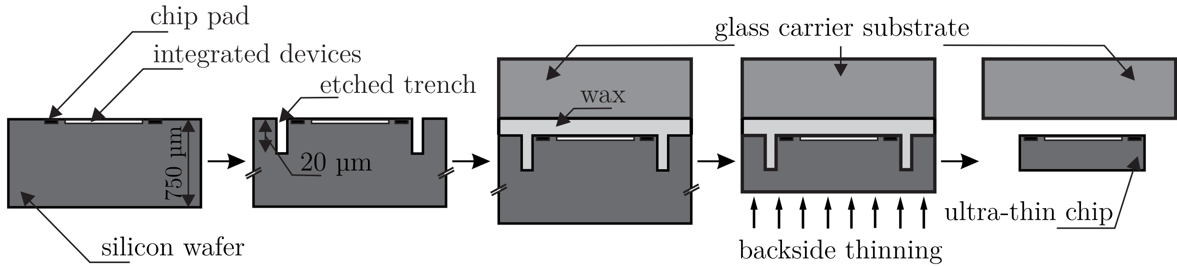


***Figure 5.6: Dicing by thinning process steps.*** *Starting from a traditional silicon wafer with integrated circuits, dry-etched trenches are opened around every die in the silicon substrate. A glass carrier substrate is attached on the wafer using wax. The wafer containing the chips is thinned until the trenches are reached. The last step is the detachment of the chip by wax dissolution in heated isopropanol.*

dried on a hotplate at 50 °C for 10 minutes so that most of the solvent has evaporated, since it will serve the purpose of an adhesive layer. At this point, the chip is manually placed on the sticky PI layer. Another 1 µm thin PI layer is spun on the wafer, patterned and cured. A chromium-gold plating base is evaporated followed by an electroplating step of 5 µm gold for patterning the gold conductors providing electrical connection on-chip. A third 5 µm thin PI layer is spun on the wafer in order to encapsulate and isolate the conducting paths. In the last step of the process the flexible ultra-thin chip-in-foil can be obtained by wet etching of the sacrificial layer. Both the deployed thinning process as well as the encapsulation process are being fully described in [HMD+12].

The final result after thinning and encapsulating the several test chips developed within the scope of this work is illustrated in figure 5.8. Chip microphotographs using an optical microscope have been taken and included in the figure.

## 5.3 Experimental Setups and Techniques

In order to experimentally characterize the fabricated chips under mechanical stress several measurement setups have been realized. Before presenting the setups, the technique to bend the ultra-thin chips-in-foil is presented.

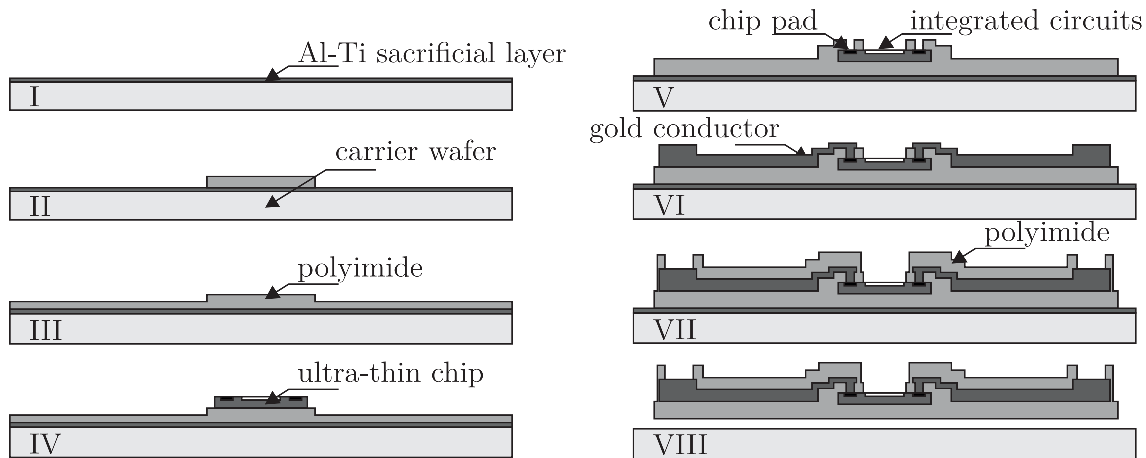


***Figure 5.7: Chip-in-foil encapsulation process.*** *Starting from an aluminum-titanium coated silicon wafer (I), the first PI layer is spun on (II) followed by the second adhesive PI layer (III). The chip is subsequently placed (IV) and a third PI layer is spun on, patterned and cured (V). Electroplating of gold conductors follows (VI) and the last layer of PI finalizes the process (VII). The PI layer is then detached from the carrier wafer by wet etching the sacrificial layer (VIII).*

## 5.3.1 Bending Apparatus

Looking back in the literature one can find several bending apparati for applying uniaxial stress on bulk silicon wafer stripes [GRG+03]. However, bending of ultra-thin silicon chips has not extensively been studied yet. In [WRSB08] the authors report a bending machine for ultra-thin chips, based on cylindrical deformation. However, the fact that shear force has to be applied on the foil substrate to stretch the chip on the cylindrical bending machine is for our work unfortunately not applicable for the following two reasons. Firstly, the thin chips are directly encapsulated and contacted within the polyimide foil substrate, as described in the previous subsection. This means that any shear force application on the foil substrate would directly transfer to the contact bumps, which might then get ripped off the chip pads. Secondly, the application of that kind of force could superimpose a tensile stress on the uniaxial stress applied on the chip due to the cylindrical deformation on the bending apparatus. The bending machine used in this work was designed and built in-house and is depicted in figure 5.9a) together with the interface PCB. In this design a cylindrical part and its cylindrical counterpart are used to force the chip to deform on the cylindrical surface of the lower part. The upper part features also an opening, in order not to superimpose any hydrostatic stress on the chip, which could also result to its breakage. Moreover,

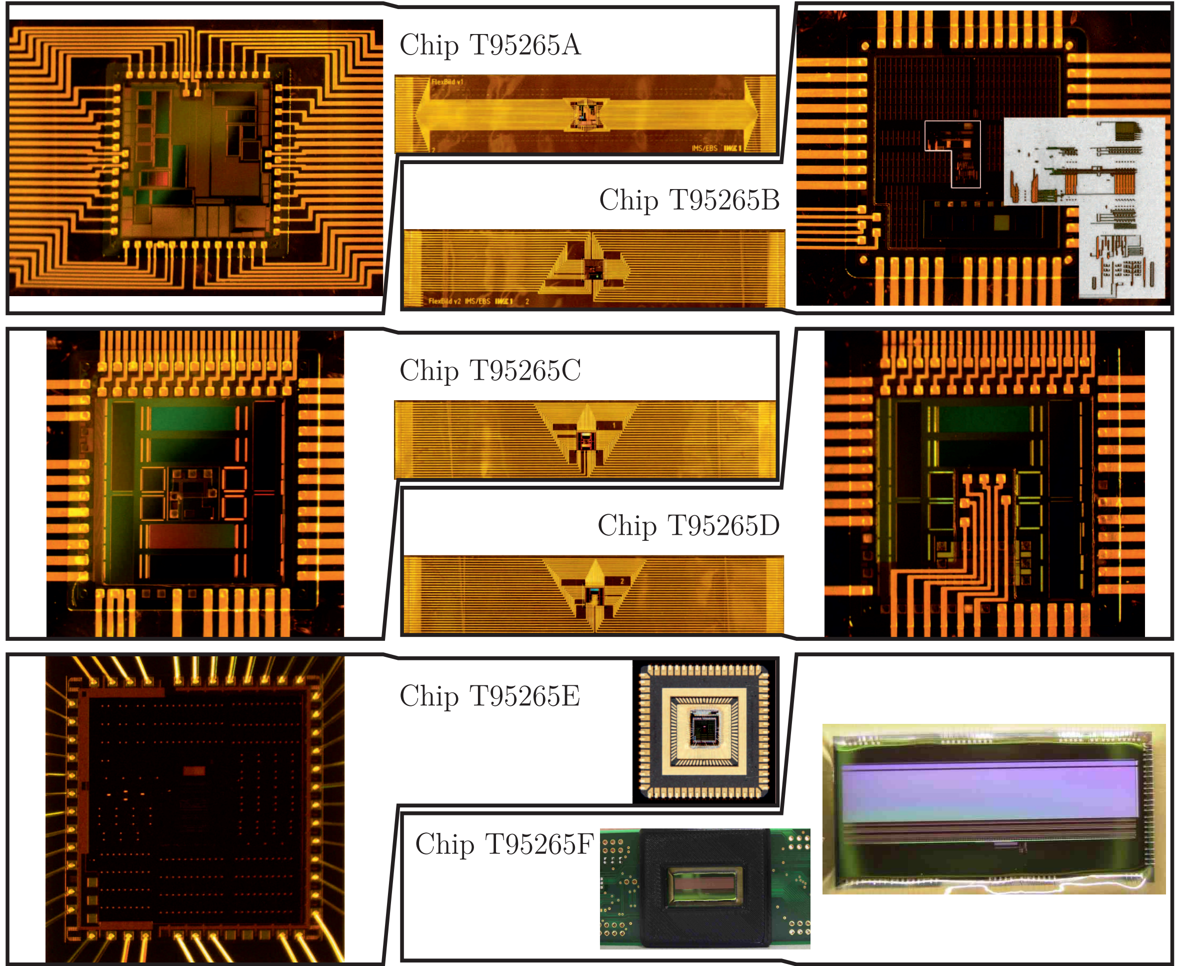


***Figure 5.8: Chips-in-foil fabricated in this work.*** *a) T95265A chip-in-foil. Note the large area integrated photodiodes on the microphotograph. b) T95265B chip-in-foil integrating a* $15 \times 15$ *test image sensor. c) T95265C chip-in-foil. Note the large area integrated photodiodes on the microphotograph. d) T95265D chip-in-foil. Note the electrical connections on the bandgap reference chip shown in the center of the microphotograph. e) T95265E test chip. f) Image sensor T95265F chip.*

it keeps the top surface of the chip uncovered for the optical measurements. Such parts have been constructed in different radii $R$ and for both tensile and compressive configurations, as shown in figure 5.9b).

The calculation of the applied uniaxial stress is based on the employed bending radius $R$, the silicon chip thickness $d_c$, the underlying PI layer thickness $d_{PI}$ and their young moduli $Y_{Si}$ and $Y_{PI}$ respectively. For a two-layer structure similar to the one depicted in figure 5.10, the neutral plane (where the stress equals zero) $h_n$ lies within the silicon chip volume and is given by equation (5.3.1), where $i$ denotes the layer. The

uniaxial mechanical stress $\sigma$ at an arbitrary height $h$ can be expressed by equation (5.3.2). The chips used in this work are thinned down to thicknesses ranging from $12-26$ µm. Employing equation (5.3.1) the uniaxial mechanical stress is calculated for several bending radii and chip thicknesses and is listed in table 5.3. Uniaxial tensile mechanical stresses hold throughout this work positive values, while compressive ones hold negative values.

$$h_n = \frac{\sum_i Y_i d_i h_{m,i}}{\sum_i Y_i d_i} \tag{5.3.1}$$

$$\sigma = Y_i(h - h_n) \cdot R^{-1} \tag{5.3.2}$$

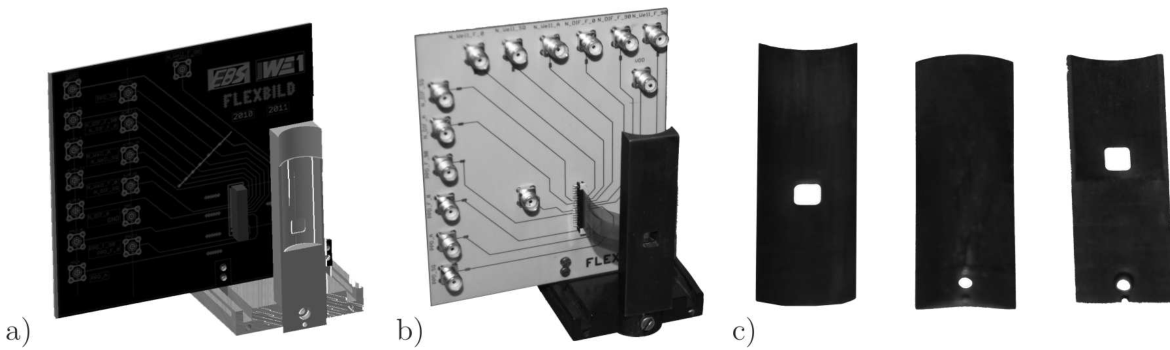


***Figure 5.9: Bending apparatus used in this work based on cylindrical deformation.*** *a) Model from the computer aided design (CAD) program in a compressive bending configuration. b) Manufactured apparatus with the interface PCB and a chip-in-foil in a tensile bending configuration. c) Parts used for applying tensile and compressive stress.*

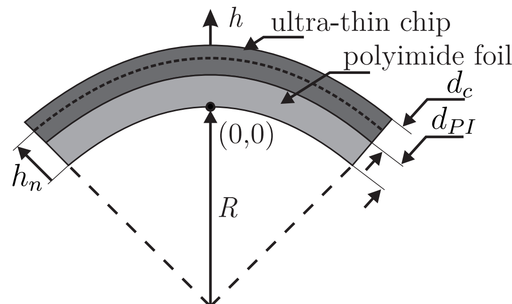


***Figure 5.10: Two-layer structure for mechanical stress calculation.*** *Note that the neutral stress plane lies within the silicon chip volume. Adding more layers on the structure, will move the neutral stress plane according to equation (5.3.1).*

***Table 5.3: Uniaxial mechanical stress $\sigma$ calculation for diverse chip thicknesses $d_c$ and bending radii $R$.*** *All mechanical stress values stated are given in* [MPa].

| Thickness $d_c$ [µm] | Bending radius $R$ [mm] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 20 | 15 | 10 | 9 | 8 | 7 | 6 | 5 |
| 8 | 36 | 48 | 72 | 80 | 90 | 103 | 121 | 145 |
| 10 | 44 | 59 | 89 | 99 | 111 | 127 | 148 | 178 |
| 12 | 53 | 70 | 106 | 117 | 132 | 151 | 176 | 211 |
| 14 | 61 | 82 | 123 | 136 | 153 | 175 | 204 | 245 |
| 16 | 70 | 93 | 139 | 155 | 174 | 199 | 232 | 279 |
| 18 | 78 | 104 | 156 | 174 | 195 | 223 | 261 | 313 |
| 20 | 87 | 116 | 173 | 193 | 217 | 248 | 289 | 347 |
| 22 | 95 | 127 | 190 | 211 | 238 | 272 | 317 | 380 |
| 24 | 104 | 138 | 207 | 230 | 259 | 296 | 345 | 414 |
| 26 | 112 | 149 | 224 | 249 | 280 | 320 | 374 | 448 |

## 5.3.2 Electrical and Optical Measurement Setups

The measurement setups used for the electrical measurements of MOSFETs are schematically shown in figure 5.11. For both setups the temperature is controlled and regulated. In the setup of figure 5.11a) both wafer-level, chip-level as well as chip-in-foil-level measurements can be performed. Up to 48 input/output signals can be connected simultaneously in the low-leakage switching matrix (HP E5250A), which permits continuous automated measurements of an entire chip under mechanical stress. The entire measurement procedure is assisted by an optical microscope, which allows the accurate placement of measurement probe needles in case of wafer-level measurements. The setup is fully automated and is controlled by a custom programmed LabVIEW® software interface, which controls the wafer positioning system, the semiconductor parameter analyzer (HP 4155C) as well as the switching matrix. Utilizing the setup of figure 5.11b) chip-in-foil-level measurements have been performed. Similarly, the setup is controlled by a custom programmed LabVIEW® software interface. The exact measurement procedures, electrical connections as well as measurement techniques (such as shielding and calibration) have been documented in [Lor12] and [HDW13].

The noise measurement setup utilized for noise measurements is schematically shown in figure 5.12. The $\mu$-metallic box exhibits a high permeability therefore allowing shielding against static and low-frequency magnetic fields, while the Faraday shielding provided by the grounded aluminum box yields shielding from external electrical fields.

The entire measurement setup is battery operated in order to avoid noise components coming from the 50 Hz main power line. For more information about the measurement setup refer to [Bro09].

Using the measurement setup of figure 5.13 the characteristics of the photodiodes under illumination and under diverse bending radii have been measured (sensitivity and quantum efficiency) and analyzed to examine the dependence of these characteristics on uniaxial tensile and compressive mechanical stress. Optical measurements are carried out under controlled room temperature (± 0.5 °C) and take place in a black box to prevent background light from illuminating the device under test (DUT). Chopping and filtering techniques are employed as illustrated using an optical chopper and two lock-in amplifiers (Perkin Elmer 5210). This allows modulating the light beam and recovering the signal (converted into current in the photodiode) from the modulated frequency,

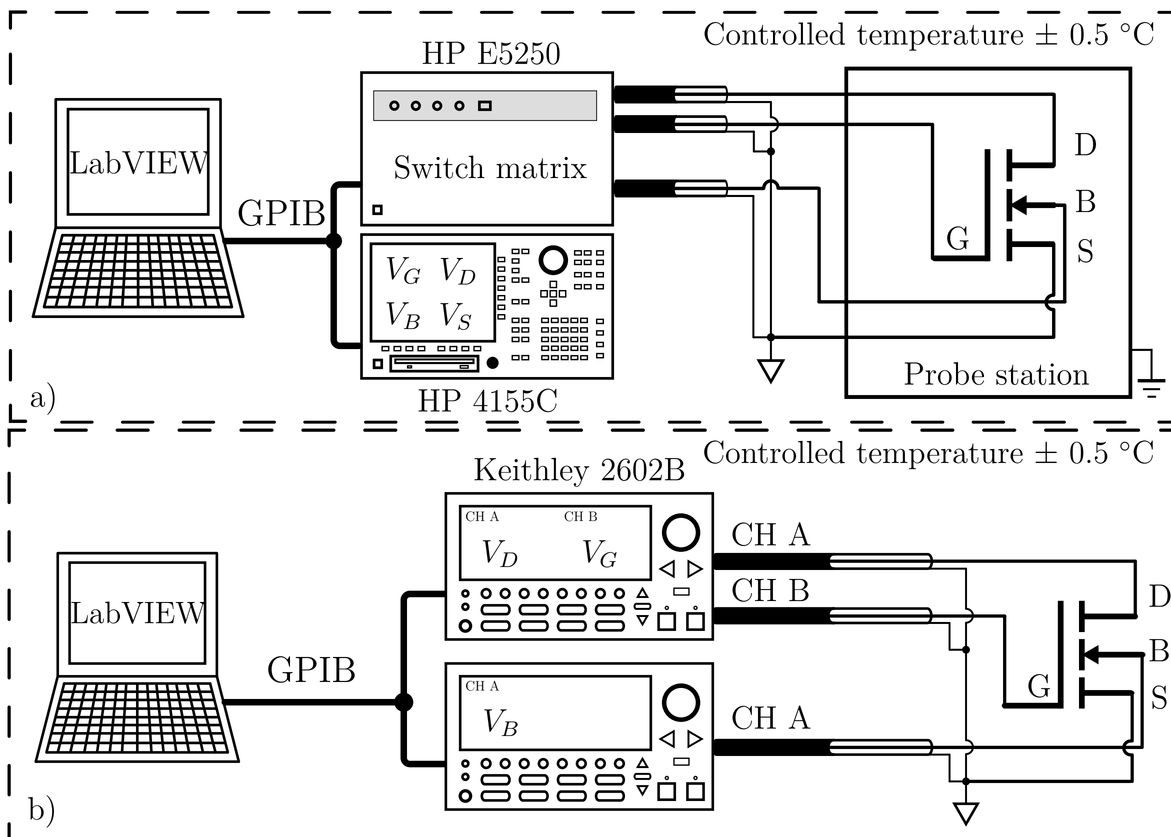


***Figure 5.11: MOSFET electrical measurement setup.*** *a) Wafer-level, chip-level as well as chip-in-foil-level measurements can be performed utilizing this setup. b) This setup is used for chip-in-foil-level measurements. In both setups the bending apparatus can be additionally accommodated.*

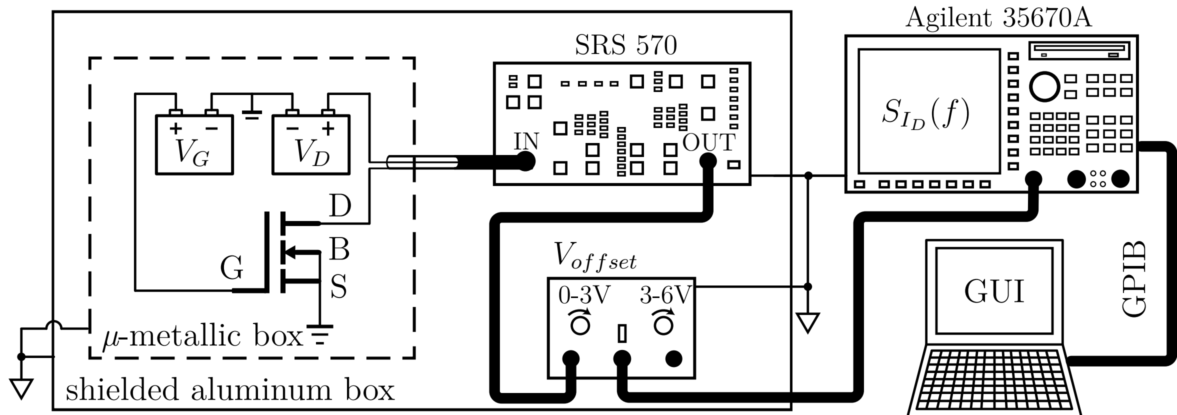


***Figure 5.12: MOSFET electrical noise measurement setup.*** *The setup deploys a low noise SRS 570 amplifier, an Agilent 35670A spectrum analyzer and an offset voltage $V_{offset}$ correction circuit. In the setup the bending apparatus can be additionally accommodated.*

therefore achieving increased signal-to-noise ratio (SNR). Additionally, calibration of the optical path is being performed using a calibrated photodiode from Hamamatsu Photonics. The setup is fully automated and is controlled by a custom programmed LabVIEW® software interface.

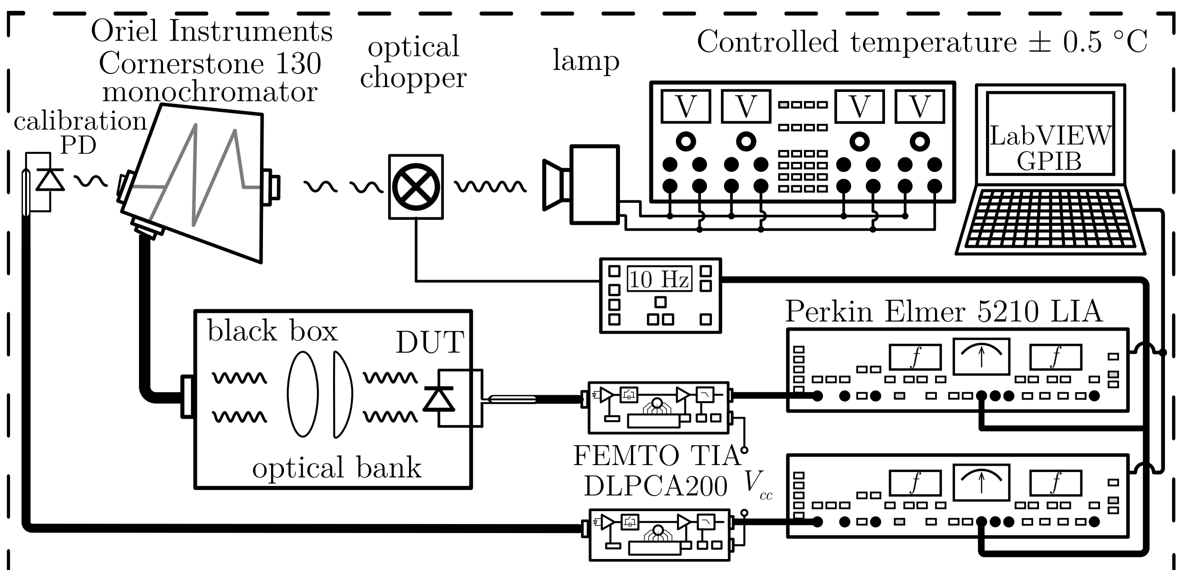


***Figure 5.13: Photodiode optical measurement setup.*** *The setup deploys two lock-in Perkin Elmer 5210 amplifiers (LIA), two low noise FEMTO DLPCA200 transimpedance amplifiers (TIA), a monochromator, a lamp and an optical chopper all from Oriel Instruments. Note the optical chopping controller setting at 10 Hz. In the setup the bending apparatus can be additionally accommodated.*

The dark current measurements of the fabricated p-n junction based photodiodes are performed using the measurement setup shown in figure 5.14. Here, a Keithley 2636A SourceMeter instrument capable of current measurements with fA resolution and accuracy is put into use. The dark current signal is measured under increased temperature (40 °C - 75 °C) and under different bending radii. The measurements are carried out in a climate chamber with an accuracy of ± 0.05 °C. The measurement of the dark current under increased temperature (and not under room temperature) has its roots in two reasons: a) The dark current almost doubles every 6 °C - 9 °C allowing the shift of the absolute signal value in the pA range where accurate and reproducible measurements, in comparison with the fA range under room temperature, can be performed and b) strain-induced dark current variations in the range of 1 - 10 % can be now reproducibly detected since their absolute value is in the higher fA or lower pA range.

Integrated capacitors are characterized utilizing the measurement setup of figure 5.15. Measurements are carried out under controlled room temperature (± 0.5 °C) and take place in a black box to prevent background light from illuminating the device under test (DUT). Capacitance measurements are performed at a frequency of 100 kHz. Calibration of the measurement setup is performed employing the inherent calibration functions offered by the Agilent 4294A Impedance Analyzer. The exact measurement procedures, electrical connections as well as measurement techniques (such as shielding and calibration) have been documented in [Lor12] and [HDW13].

The fabricated image test sensors are measured under illumination (or dark conditions) and under diverse bending radii utilizing the measurement setup illustrated in figure 5.16. Constant voltage and current references as well as digital control signals are required for readout of the sensors, as shown in figures 5.3 and 5.5. For this purpose, a custom made PCB has been designed, which supplies the test sensor with programmable voltage and current references. The programming of the references follows over a common serial peripheral interface bus (SPI) implemented in an field programmable gate array (FPGA). Moreover, the FPGA has been programmed to generate the needed synchronized digital control signals. Additionally, on the same PCB a low noise 16-bit analog-to-digital converter (ADC) digitizes the analog output signal of the test sensors. Both the digital data acquisition from the ADC as well as its control are taken over the FPGA. On the computer side, a tailor made software implemented in C++ communicates with the FPGA over a common serial connection. A graphical user interface (GUI) has been programmed allowing the user a) to setup

a custom digital control sequence for reading out the test sensor b) to configure the levels of the voltage and current references c) to configure the sampling rate of the ADC and d) to acquire the measured data in the computer with accurate timestamps. The presented software and FPGA programs have been documented in detail in [NX12].

It is also important to mention, that measuring dark current strain-induced changes of a photodiode is not a trivial task, since the signal to be measured lies in the higher

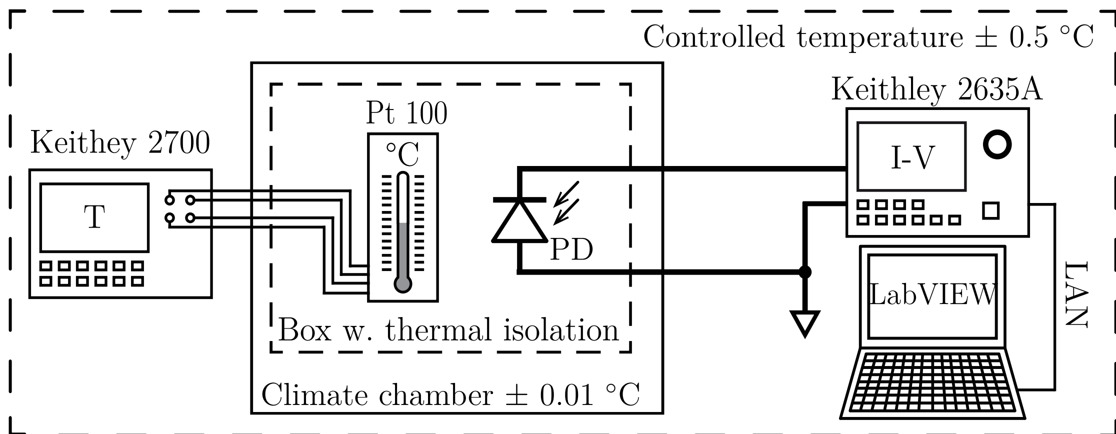


***Figure 5.14: Photodiode dark current measurement setup.*** *The setup deploys a Keithley 2636A SourceMeter instrument and an accurate temperature control within the climate chamber. The DUT is placed in a box with thermal isolation and the temperature is monitored through a Pt 100 thermometer. In the setup the bending apparatus can be additionally accommodated.*

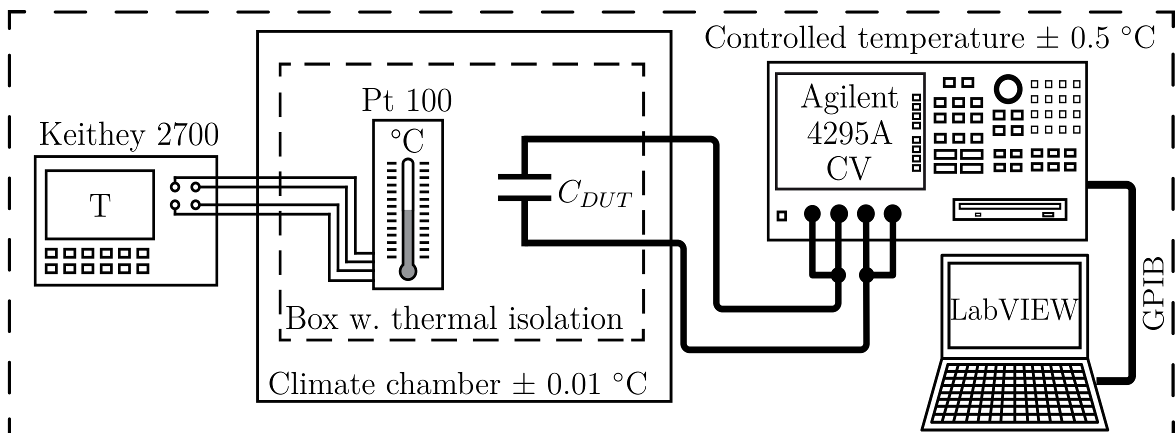


***Figure 5.15: Capacitor electrical measurement setup.*** *The setup deploys an Agilent 4294A Impedance Analyzer. The DUT is placed in a box with thermal isolation and the temperature is monitored through a Pt 100 thermometer. In the setup the bending apparatus can be additionally accommodated.*

fA range. During the work it was made clear that measuring such tiny changes requires the right choice of PCB material where the chip will be mounted on, low-noise cables, vibration-free setups and very clean surfaces. Utilizing the common glass reinforced epoxy laminate (FR4) PCBs will lead to increased leakage currents on the PCB, which will exceed the signal to be measured. In this work ceramic PCBs have been utilized and proved to be an essential choice. Moreover the material of the bending apparatus and its shielding can also influenced significantly the measurements of integrated capacitors, where an AC signal has been fed into the device. Metal bending apparati proved to exhibit a high capacitance between the apparatus and the conducting paths, even when the apparatus has been grounded. These parasitic influences on the measured capacitance have been minimized by employing poly-vinyl-chloride (PVC) bending apparati together with antistatic prevention measures. More information can be found in [HDW13].

## 5.4 Synopsis

In this chapter, the experimental methods used throughout this work have been presented. First the in-house manufactured bending apparatus to apply external uniaxial mechanical stress, based on cylindrical deformation, has been described. Next, the diverse electrical and optical measurement setups have been documented. The chapter closes with guidelines on measurement techniques and the proper choice of materials for accurate experimental results.

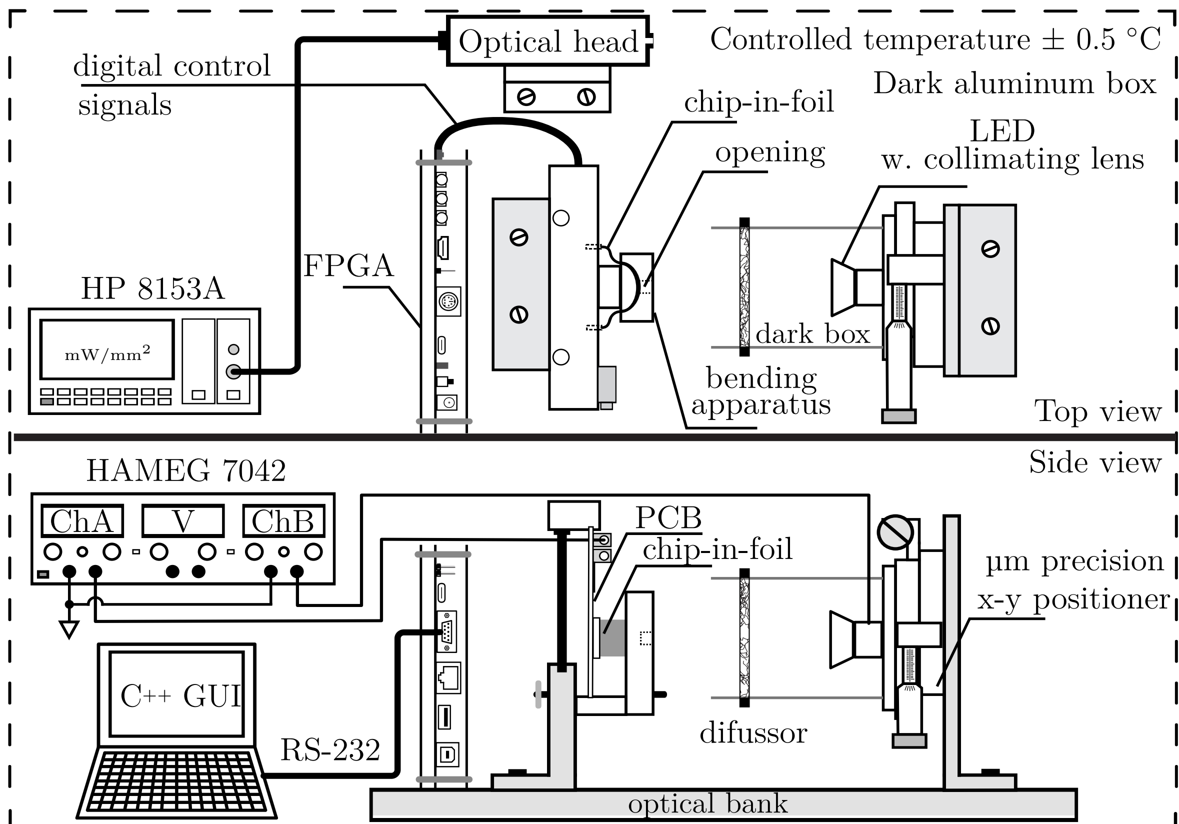


***Figure 5.16: Top and side view of the optical measurement setup for CMOS image test sensors.*** *The setup deploys a collimated light source followed by a diffusive lens. A PCB supplies all necessary reference voltages and currents to the stressed image sensor (chip-in-foil) and digitizes the chip output data. An FPGA controls the chip and collects the data feeding them to the computer. An optical power meter HP 8153A is used to measure the light beam intensity. The setup is placed in a black shielded box.*

# Chapter 6 - Experimental Results

In this chapter the experimental results obtained in this work will be in detail presented. In section 6.1 p-n junction based photodiodes will be electrically and optically characterized under mechanical stress utilizing the measurement setups presented in the previous chapter. Measurements of uniaxially strained MOS capacitors and MOS transistors follow in sections 6.2 and 6.3 respectively. Bendable image test sensors will be characterized and discussed in section 6.4, while a bendable bandgap reference under mechanical stress will be evaluated in 6.5. Based on the accomplished results, the design of a flexible CIS for bendable applications is presented in section 6.6. The proposed sensor is designed to exhibit a mechanical stress independent operation, which renders it the first CMOS image sensor ever published in literature with such feature. Section 6.7 summarizes and closes this chapter. The majority of the presented results are published by the author in [HMD+12], [Dog13], [DHM+13] and [DHG13].

## 6.1 Strained p-n Junction Based Photodiode

The characteristics of the integrated p-n junction based photodiodes have been investigated under mechanical stress. Electrical characteristics such as dark current as well as optical characteristics have been experimentally determined under strained conditions. Starting from the electrical characteristics, the strained-induced changes of the dark current have been measured for different diode orientations and geometries (recall figure 5.2). The dark current of a diode is proportional to its area as well as its perimeter as dictated by (3.2.2) and contains different components (diffusion current and the generation/drift current).

Each of the components exhibits a strong temperature dependence mainly owing to the existence of the intrinsic carrier concentration $n_i$ in equation (3.2.2). However, the diffusion current component shows a square-law dependence on $n_i$ ($I_{diff} \propto n_i^2 = f^2(T)$), while the generation/drift current component a linear dependence ($I_{drift} \propto n_i = f(T)$). Therefore, the temperature dependence of the dark current components $\partial \log I_{diff}/\partial T$, $\partial \log I_{ge}/\partial T$ can be expressed as follows:

$$\frac{\partial \log I_{diff}}{\partial T} \propto \frac{2}{f(T)} \frac{\partial f(T)}{\partial T} \tag{6.1.1}$$

$$\frac{\partial \log I_{ge}}{\partial T} \propto \frac{1}{f(T)} \frac{\partial f(T)}{\partial T} \tag{6.1.2}$$

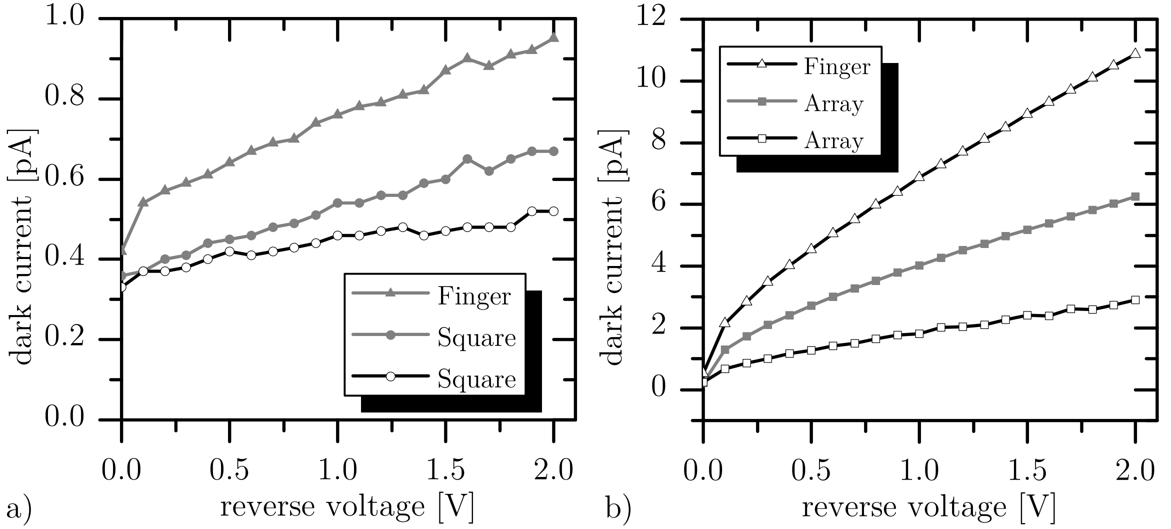


***Figure 6.1: Dark current dependence on diode geometry, type and and reverse voltage.*** *a) Measurement at room temperature. Black solid lines with open symbols denote n-well/p photodiodes, while gray solid lines with closed symbols n+/p photodiodes. Note how here the diffusion current dominates. b) Measurement at room temperature. Black solid lines with open symbols denote n-well/p photodiodes, while gray solid lines with closed symbols n+/p photodiodes. Note how here the generation/drift current component dominates (square root dependency on the reverse voltage).*

(6.1.3)

Through the above equations it is made clear that:

$$\frac{\partial \log I_{diff}}{\partial T} = 2 \cdot \frac{\partial \log I_{ge}}{\partial T} \tag{6.1.4}$$

Moreover, the applied reverse voltage will increase the generation/drift component according to square root of the reverse voltage. Thus, performing a dark current measurement under different temperatures, reverse voltages and for different diodes and plotting the results in a semi-logarithmic scale allows a further understanding of the dominant dark current component. In other words, a steeper slope in the temperature plot would suggest a more dominant diffusion component in the measured dark current, while a less steep slope a more dominant generation/drift current. Diffusion dark current dominated PDs will exhibit the double slope in the the temperature plot, when compare to generation/drift dark current dominated PDs, according to equation (6.1.4).

On the other hand, a reverse voltage dependence suggests also a larger generation/drift current. Figure 6.1a and 6.1b illustrate the dependence on the photodiode geometry (Square, Array, Finger: recall table 5.2), type (n+/p or n-well/p) and reverse voltage. In figure 6.2 temperature measurements for different diodes and reverse voltages have been performed.

The n-well/p and n+/p square-shaped photodiodes exhibit a small dependence on reverse voltage (Figure 6.1a)), which suggests that in this type of PDs the diffusion component of the dark current is very pronounced. A similar observation is valid for the n+/p finger-shaped photodiode, shown in the same figure. All other photodiodes, namely the n-well/p and n+/p array-shaped photodiodes and the n-well/p finger-shaped photodiode exhibit a large reverse voltage dependence and thus can be assumed that the generation/drift component of the dark current is here dominant.

This observation can be verified with temperature measurements under high and low reverse voltages. Figure 6.2 presents the temperature dependence of dark current of four photodiodes under high ($V_R = 2\ V$) and low ($V_R = 0.2\ V$) reverse voltage $V_R$. Under high reverse voltages all shown four PD types exhibit almost equal slopes, with the slope of the finger-shaped n+/p photodiode to be little higher in comparison to others. When each slope (of the figure 6.2a) is compared to the respective slope of the same photodiode under low reverse voltage (of the figure 6.2b), it is observed the following: The slopes of the PDs remain almost unchanged (increase at around 15 %), while the slope of the finger-shaped n+/p photodiode shows a higher change in comparison to others. The observed slope increase with decreasing reverse voltage is expected, since for lower reverse voltages the diffusion component of the dark current (with a larger dependence on temperature) becomes more pronounced since the drift component (with a lower dependence on temperature) is suppressed (low reverse voltage). These observations are a sign that in the finger-shaped n+/p photodiode the diffusion component of the dark current is more pronounced, which confirms the measurement in figure 6.1a.

Here, has to be underlined that the slope in the temperature plot between the finger-shaped n+/p photodiode and the other three measured PDs is not double (it is around 35 % higher than the other PD slopes - recall equation (6.1.4)), which leads to the conclusion that for this diode the diffusion and the generation/drift current are both similarly pronounced and none of the two components can be assumed to be negligible when compared to the other. In addition to the fact that all the rest

PD types demonstrate comparable temperature slopes leads to the conclusion that the n-well/p and n+/p array-shaped photodiodes and the n-well/p finger-shaped photodiode exhibit the same dominant dark current generation mechanism, similarly to the simulation results (recall figure 4.6). The dominant dark current mechanism is in this case the generation/recombination mechanism, since a) the dark current depends on the reverse voltage and b) the slope on the temperature plot is slightly dependent on the applied reverse voltage. This result verifies our assumption (recall discussion in section 3.2 p. 66), that the dominant dark current component for the photodiodes measured under mechanical stress in this work is the generation/drift dark current.

Here, it is worth to note that finger-shaped photodiodes exhibit typically high drift dark currents due to their long interface at the semiconductor surface. However, the designed array-shaped n+/p photodiode in this work shows a higher drift dark current component than its array-shaped n-well/p counterpart. An explanation for this outcome is, that the doping concentration of the n-type region of the PD affects the width of the depletion region, which becomes larger with increasing doping concentrations. Therefore, the observed drift dark current by the array-shaped n+/p photodiode is higher than its n-well/p counterpart. Moreover, the spacing between each PD of the finger- or array-shaped photodiode and the depth of the well (recall figure 5.2c) plays a critical role on the dark current components. The deeper the n-type well (such as in n-well/p PDs) the larger the vertical SCR and thus the diffusion dark current can be larger w.r.t. to a shallower n-type well. The spacing among the PDs of the finger- or the array-shaped PDs plays also an important role, since the horizontal SCRs (recall figure 2.8) of the neighboring PDs can touch or overlap, thus reducing the diffusion dark current component.

Having verified the assumption on the dominant dark current mechanism, the mechanical stress dependence on the dark current is presented. Here as underlined by the model presented in section 3.2, the expected changes in the region of ± 350 MPa are less than +10 % for compressive and no more than −2 % for tensile stresses. The strained-induced dark current changes are measured in diverse temperatures and uniaxial bending configurations. Figure 6.3a shows the dark current dependence of an array-shaped n-well/p photodiode on the applied reverse voltage $V_R$ and the applied [110] compressive mechanical stress at 55 °C. Figure 6.3b depicts its temperature and stress dependence for a constant $V_R = 2$ V. The results for tensile stresses are depicted in figure 6.4. Similarly, figures 6.5 and 6.6 illustrate the results of an array-shaped n+/p photodiode under stress. For both photodiode types an increase in the dark

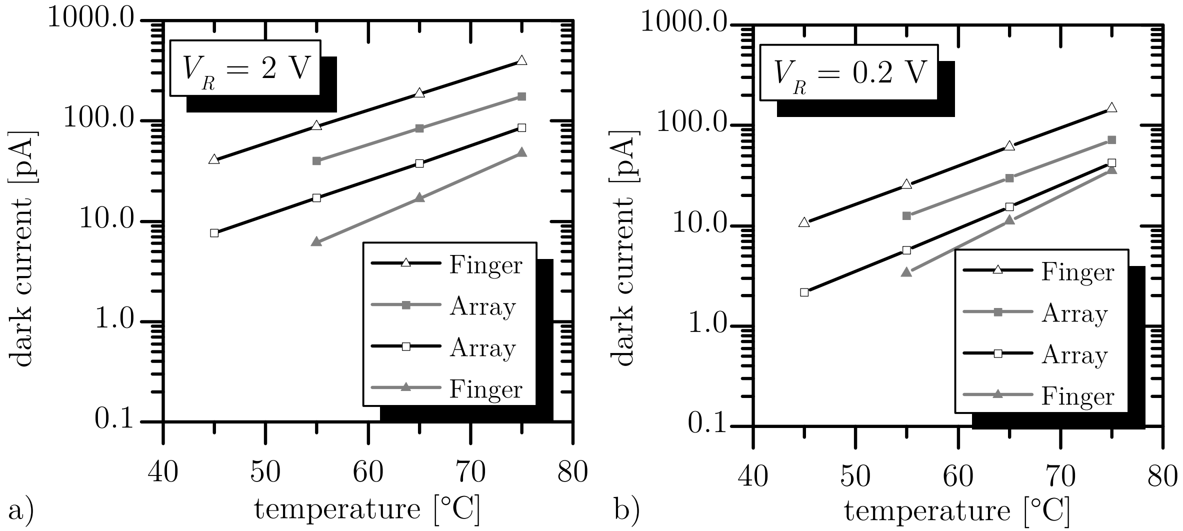


***Figure 6.2: Dark current dependence on temperature and reverse voltage $V_R$.*** *a) At a reverse voltage of 2 V. b) At a reverse voltage of 0.2 V. Black solid lines with open symbols denote n-well/p photodiodes, while gray solid lines with closed symbols n+/p photodiodes. Note that the slopes are almost equal among different photodiode types, except for the finger-shaped n+/p photodiode which is slightly steeper. Moreover, the the temperature dependence of a PD does not change significantly with increasing reverse voltage, which is a sign of a pronounced drift dark current component. For the finger-shaped n+/p photodiode the steeper slope is a clear sign of an increased diffusion dark current component.*

current under uniaxial [110] compressive stress is observed, while the dark current decreases under uniaxial [110] tensile stress as anticipated by the model.

Next, results of the strain-induced dark current changes will be presented under different temperatures. The investigated photodiodes have been measured in the setup of figure 5.14 under accurately controlled temperature (< ± 0.01 °C). The changes should demonstrate an exponential dependence on the applied uniaxial mechanical stress, according to the developed model of equations (3.2.10) and (3.2.9). Figures 6.7 and 6.8 illustrate such strain-induced dark current changes of different photodiode types and geometries. Figure 6.7 depicts the exponential dark current changes (increase) for an array-shaped and a finder-shaped n-well/p photodiode for different temperatures. As predicted by the model, the measured results follow an exponential character. It is also worth to note that the strain-induced changes are dependent on the temperature, namely strain-induced changes decline with increasing temperature. This result underlines the decrease of the piezojunction coefficient with increasing temperature as was elucidated for the piezoresistive coefficients of silicon in table 3.3 (negative TCP). The

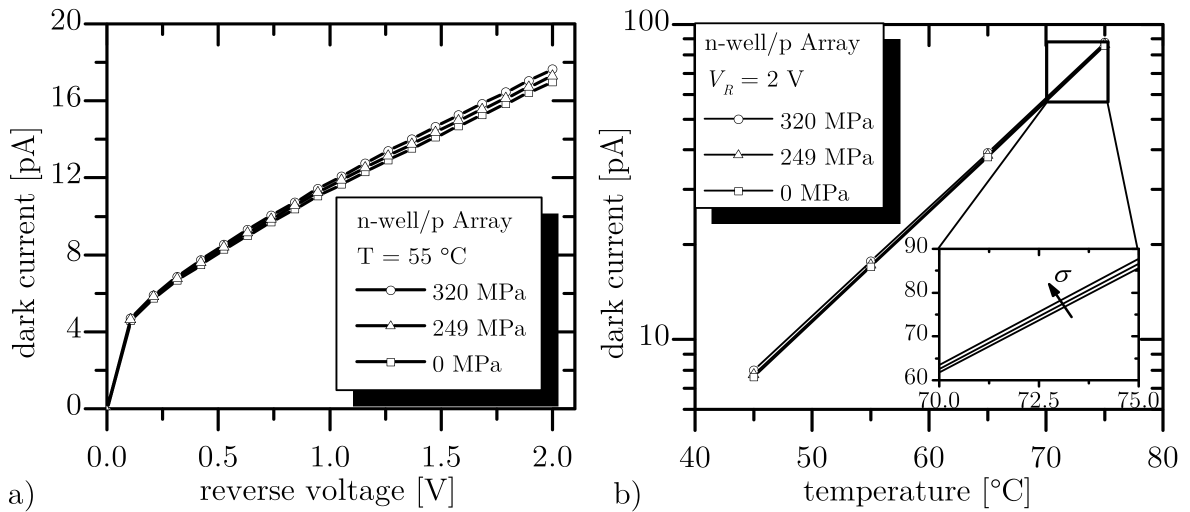


***Figure 6.3: Dark current characteristics of an array-shaped n-well/p photodiode under compressive mechanical stress.*** *a) At a temperature of* 55 °*C. b) At a reverse voltage* $V_R = 2$ *V. Note the dark current increase under compression.*

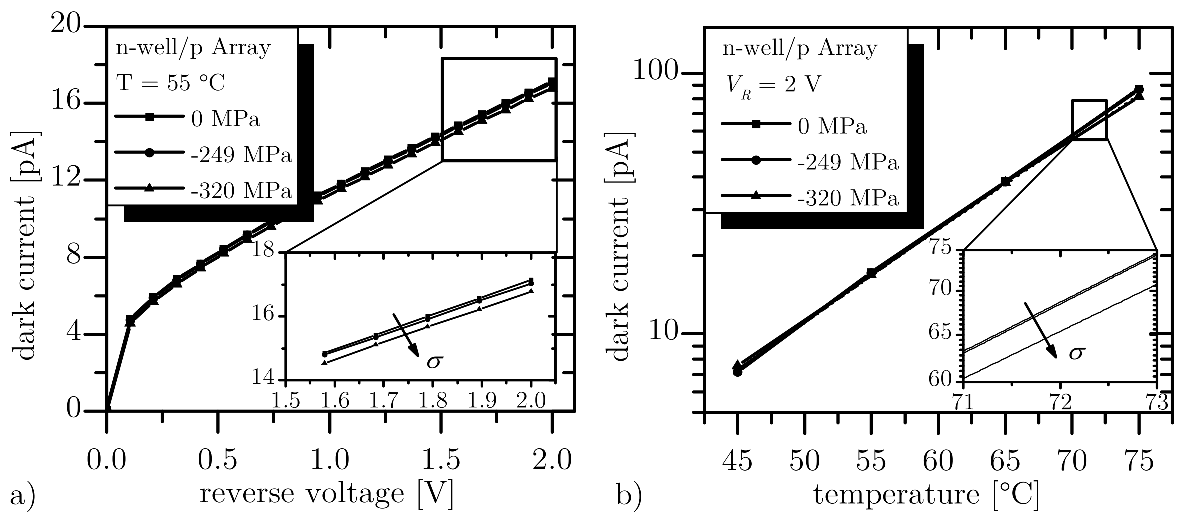


***Figure 6.4: Dark current characteristics of an array-shaped n-well/p photodiode under tensile mechanical stress.*** *a) At a temperature of* 55 °*C. b) At a reverse voltage* $V_R = 2$ *V. Note the decrease in dark current under tensile stress.*

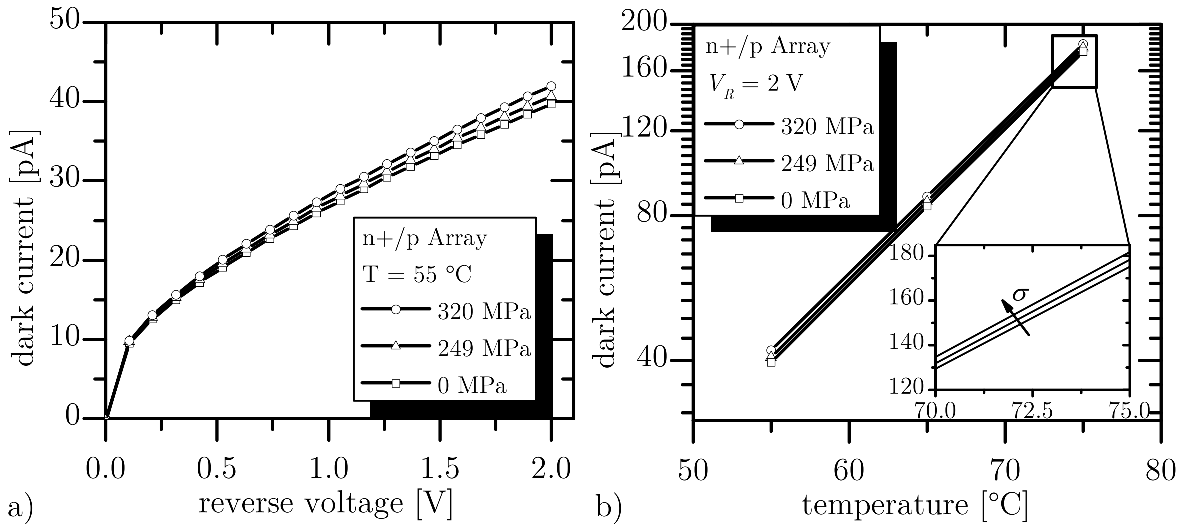


***Figure 6.5: Dark current characteristics of an array-shaped n+/p photodiode under compressive mechanical stress.*** *a) At a temperature of 55 °C. b) At a reverse voltage $V_R = 2$ V. Note the increase in dark current under compressive mechanical stress.*

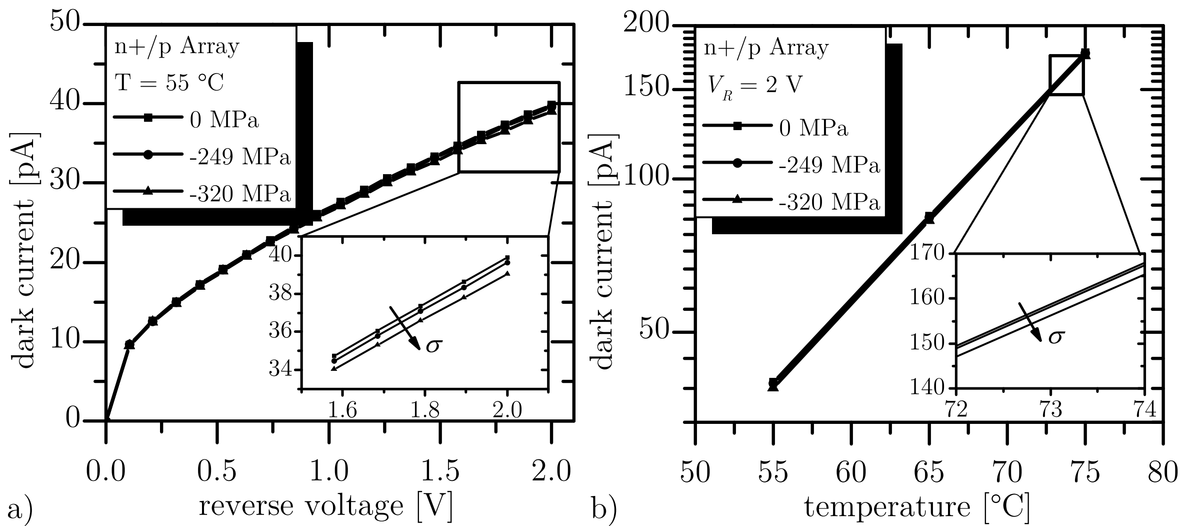


***Figure 6.6: Dark current characteristics of an array-shaped n+/p photodiode under tensile mechanical stress.*** *a) At a temperature of 55 °C. b) At a reverse voltage $V_R = 2$ V. Note the decrease in dark current under tensile mechanical stress.*

temperature coefficient of the dark current changes for each diode type is computed and is shown on the respective figure. A reduction of the TCP with increasing doping concentration is also observed in the case of finger-shaped PDs, where the TCP of n+/p PDs (featuring a higher doping concentration) is lower than the TCP of its n-well/p counterpart (featuring a lower doping concentration).

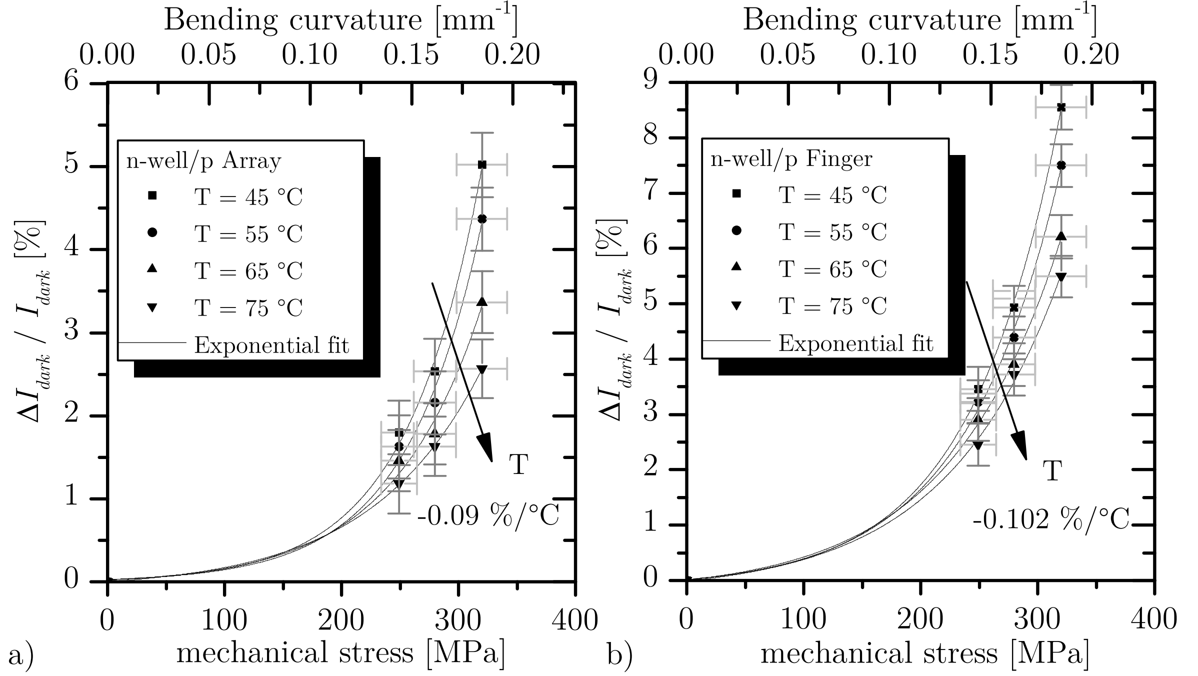


***Figure 6.7: Strain-induced dark current changes of n-well/p photodiodes under compressive mechanical stress at a reverse voltage of $V_R = 2$ V.*** *a) Array-shaped PD. b) Finger-shaped PD. Note the exponential increase of dark current with the applied compressive stress and the decrease of the dark current changes with increasing temperature. Solid lines represent the exponential fit of the measured data, while the gray bars denote measurement errors.*

In figures 6.7 and 6.8 the measured data have been fitted with an exponential function $A\,[exp(\pi_j \sigma) - 1]$. The values of the coefficient $A$ and the piezojunction coefficient $\pi_j$ have been calculated for every temperature and are depicted in figure 6.9. Here, the general tendency of a decreasing piezojunction coefficient $\pi_j$ with increasing temperature is observed (recall that the TCP of silicon is negative). Assuming a linear dependence of $\pi_j$ with increasing temperature the dark current characteristics at lower temperatures i.e., 25 °C or 35 °C can be extrapolated. At these temperatures the strain-induced changes are very difficult to be determined experimentally due to the very low magnitude of the signal to be measured (several decades of fA). Such cal-

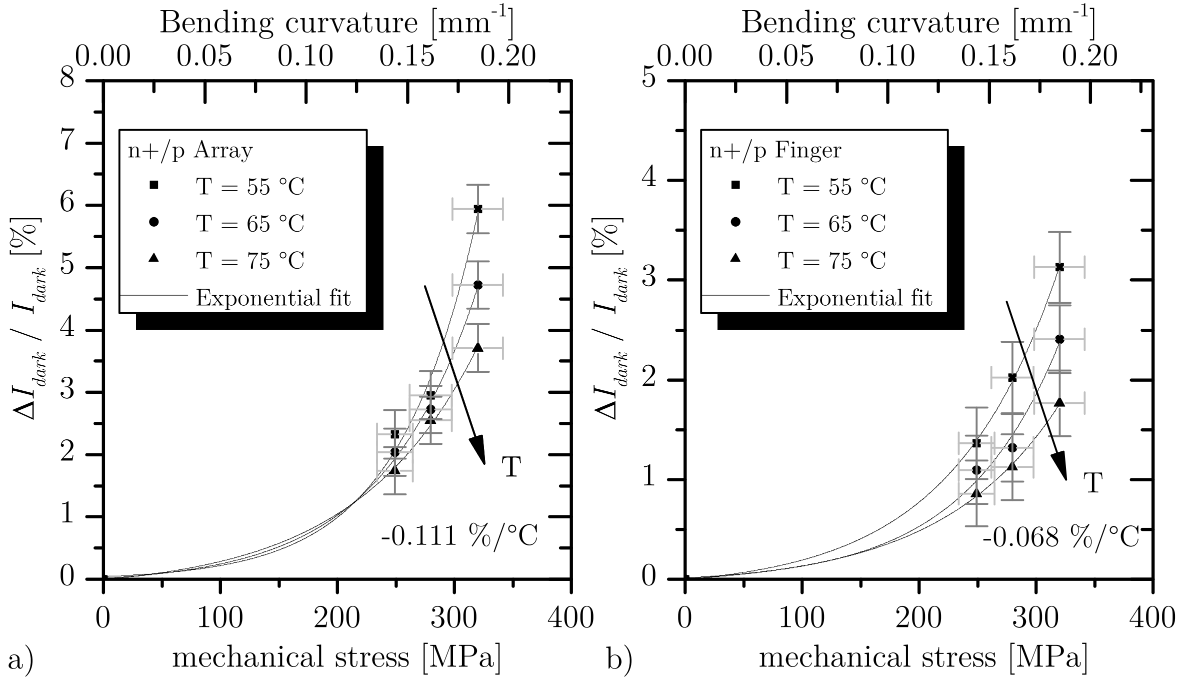


***Figure 6.8: Strain-induced dark current changes of an array-shaped n+/p photodiode under compressive mechanical stress at a reverse voltage of $V_R = 2$ V.*** *a) Array-shaped PD. b) Finger-shaped PD. Note the exponential increase of dark current with the applied compressive stress and the decrease of the dark current changes with increasing temperature. Solid lines represent the exponential fit of the measured data, while the gray bars denote measurement errors.*

culations have been performed and shown for the n-well/p type photodiodes in figure 6.10.

For uniaxial tensile stresses the dark current changes anticipated are significantly smaller than the presented ones for uniaxial compressive stresses and reproducible measurements are hard to be achieved. However, under constant temperature (±0.01 °C) and averaging performed on several measurements satisfactory results can be achieved. Figures 6.11 and 6.12 illustrate overall strain-induced dark current changes of different photodiode types and geometries. The measurement results verify the model outcome, which describes negative dark current changes under the application of uniaxial tensile stresses up to 350 MPa.

Next, results on the optical characteristics of p-n junction based photodiodes on flexible chips-in-foil under mechanical stress are presented. The optical sensitivity of silicon p-n junction based photodiodes under uniaxial mechanical stress has not been reported yet to the knowledge of the author. Recall the reasoning of section 3.2 p.

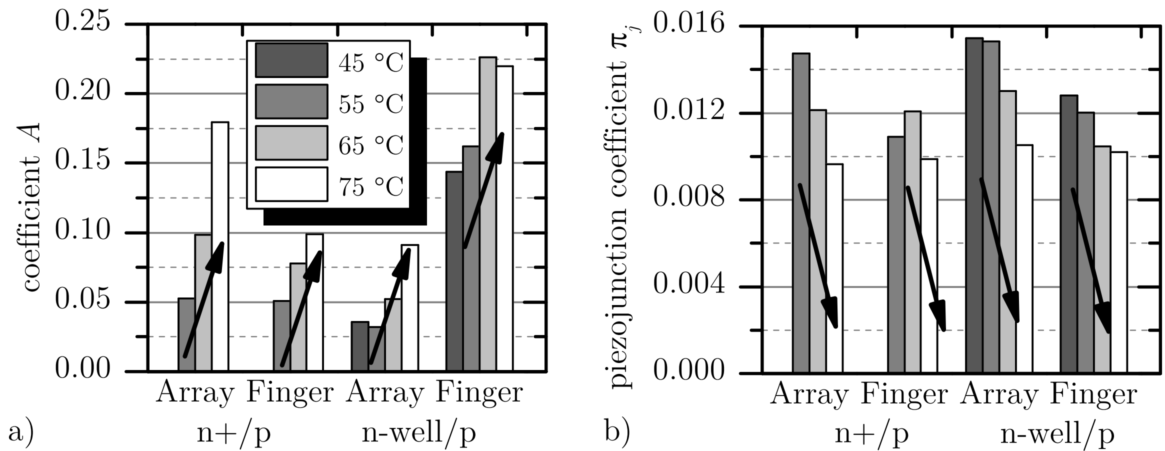


***Figure 6.9: Exponential fit parameters A and $\pi_j$ versus temperature.*** *Note the general tendency of a decreasing piezojunction coefficient $\pi_j$ with increasing temperature.*

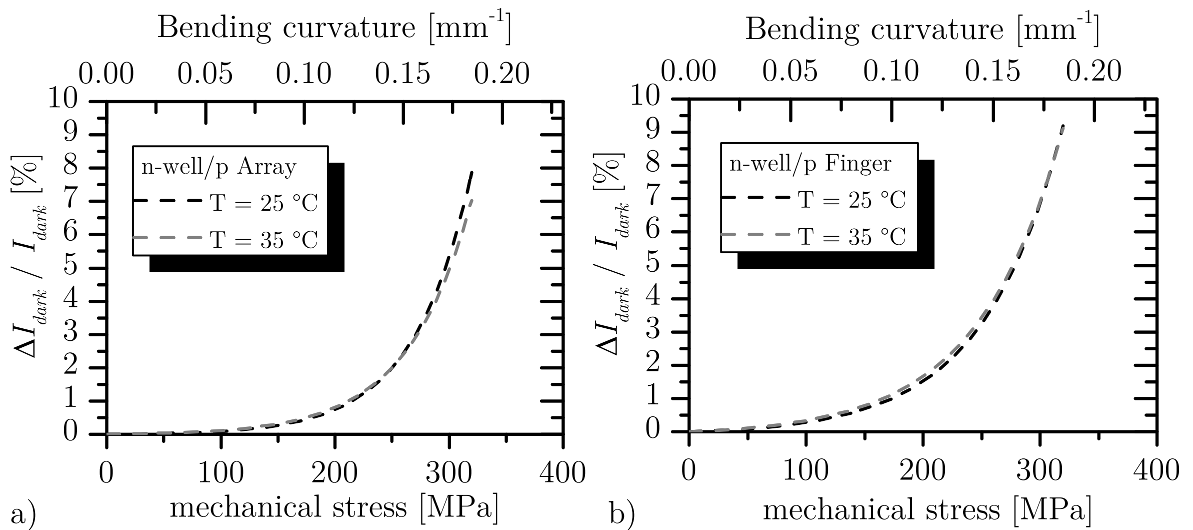


***Figure 6.10: Extrapolation of strain-induced dark current changes at 25° C and 35° C.*** *a) Array-shaped n-well/p photodiode. b) Finger-shaped n-well/p photodiode.*

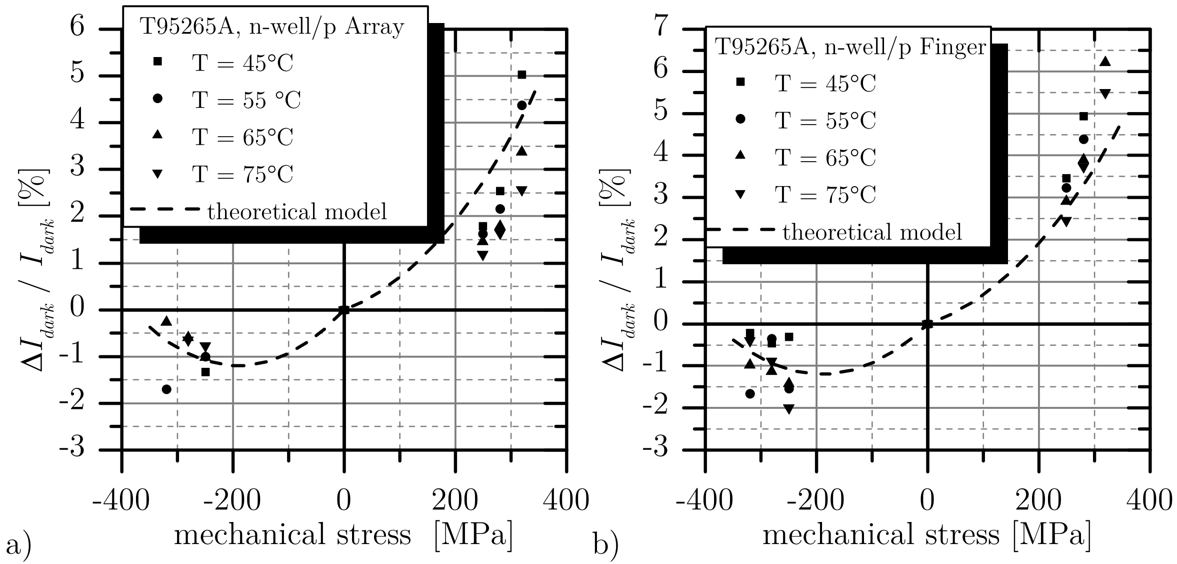


***Figure 6.11: Overall dark current strain-induced changes of n-well/p photodiodes.*** *a) Array-shaped PD. b) Finger-shaped PD. Note the exponential increase of dark current with the applied compressive stress and its decrease with tensile stresses. The dashed line represents the theoretical model.*

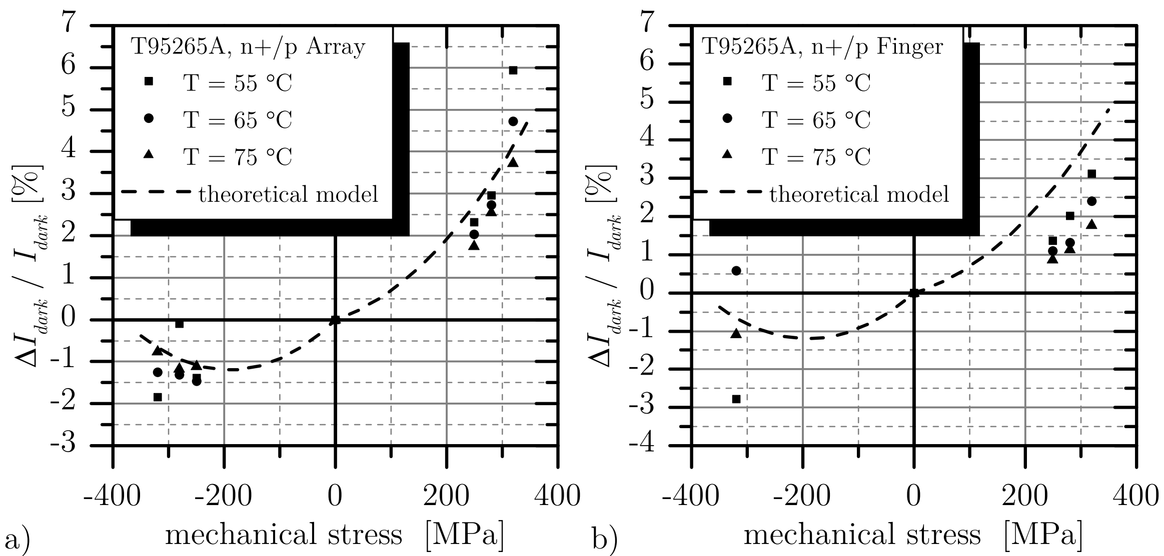


***Figure 6.12: Overall dark current strain-induced changes of n+/p photodiodes.*** *a) Array-shaped PD. b) Finger-shaped PD. Note the exponential increase of dark current with the applied compressive stress and its decrease with tensile stresses. The dashed line represents the theoretical model.*

70 on the anticipated stress independence of the optical sensitivity of a photodiode operated in the visible spectrum of light. Optical sensitivity measurements of uniaxially stressed photodiodes (recall figure 5.2) are performed in both tensile and compressive stress configurations utilizing the setup of figure 5.13. Figure 6.13 presents the results of n+/p photodiodes under strained and relaxed conditions. Similarly, figure 6.14 presents the results of n-well/p photodiodes under strained and strain-free (relaxed) conditions.

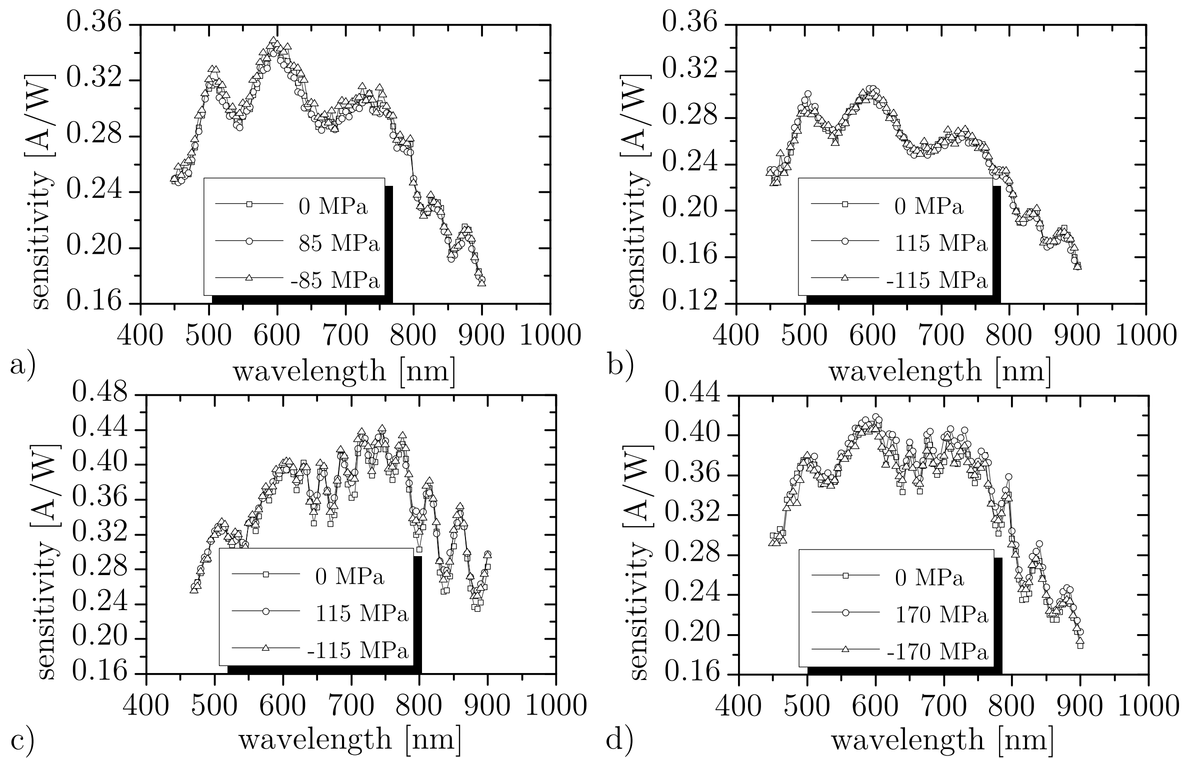


***Figure 6.13: Strain-induced changes on optical sensitivity of n+/p photodiodes under uniaxial* [110] *mechanical stress.*** *a) Finger-shaped photodiode with a* $0°$ *orientation. b) Finger-shaped photodiode with a* $90°$ *orientation. c) Square-shaped photodiode. d) Array-shaped photodiode.*

The figures presented above reveal that the optical characteristics of p-n junction based photodiodes under mechanical stress and visible illumination do no show significant changes. Moreover, no dependence of the orientation of the stripes of finger-shaped photodiodes on mechanical stress is observed. The small shift of the graphs (figure 6.14a-d) between the strain-free(relaxed) and the strained states lies into the reproducibility of the used measurement setup. This result is very important towards the goal for a stress independent image sensor.

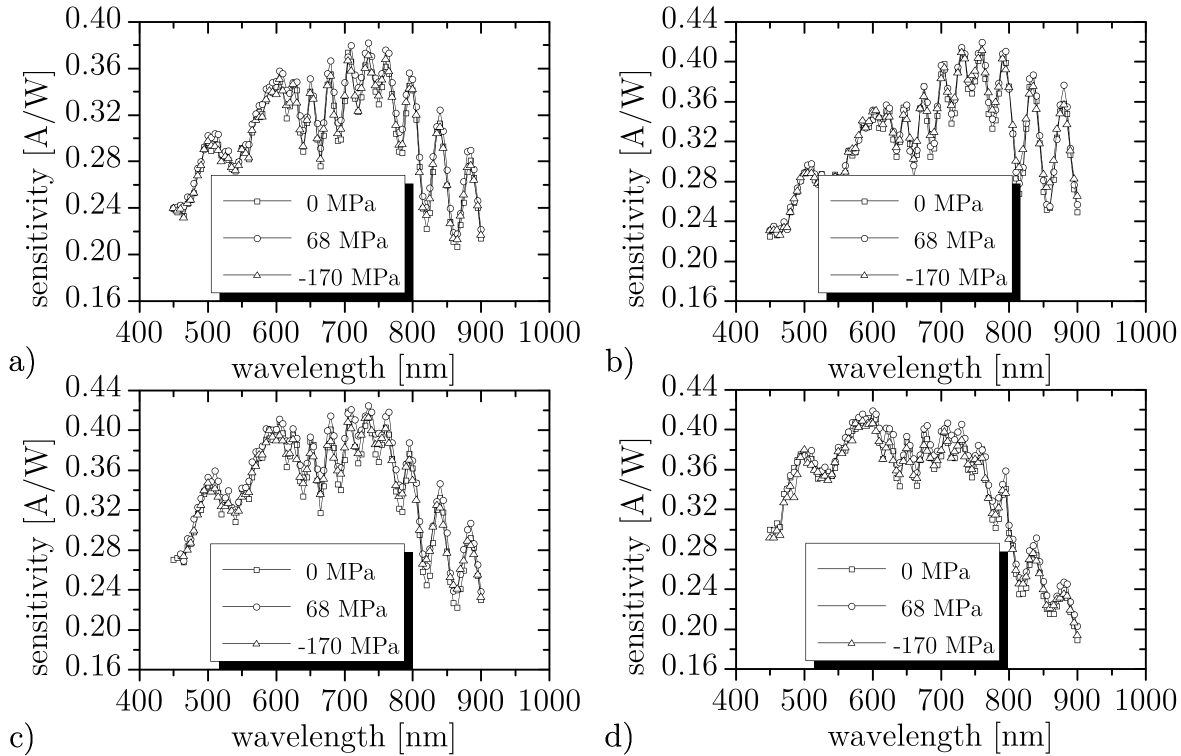


***Figure 6.14: Strain-induced changes on optical sensitivity of n-well/p photodiodes under uniaxial* [110] *mechanical stress.*** *a) Finger-shaped photodiode with a* 0° *orientation. b) Finger-shaped photodiode with a* 90° *orientation. c) Square-shaped photodiode. d) Array-shaped photodiode.*

However, figures 6.13d) and 6.14d) show an interesting effect arising when investigating the array-shaped photodiodes under mechanical stress. The interference pattern in the sensitivity data, which is observed in the middle range of the visible spectrum and arises due to the interface of the silicon substrate with the oxide layers on top, is reduced when mechanical stress on the photodiode is applied. However, the average sensitivity of the photodiode remains on the same levels. The same effect but to a smaller extent is also observed for the square-shaped photodiodes in 6.13c). The explanation of this finding lies behind the curved state of the photodiode in front of a collimated light source and the position of the photodiode with respect to the chip center. Under a bent state, the impinging collimated radiation hits every photodiode pixel of the $15 \times 15$ array with a different angle, thus affecting the creation of the minima and maxima of the “Fabry Perot” interferences. Moreover, the optical crosstalk between neighboring pixels, which would increase the interference, is lower for the array-shaped photodiodes in comparison with the square-shaped ones, due to the existence of metal

layers around each pixel. Due to the fact that all photodiode pixels of the array are connected in parallel, its optical response under mechanical stress appears to be more homogenized, since the maximum (minimum) of the interference pattern for a certain wavelength does not arise simultaneously at all photodiode pixels due to the different impinging angles of the collimated light. The guideline won from these investigations is that employing a stress independent flexible image sensor in a tensile configuration is preferred w.r.t. the strain-induced dark current change.

## 6.2 Strained Capacitor

The characteristics of the integrated MOS based capacitors offered in the CMOS process utilized in this work have been investigated under mechanical stress. Integrated PIP and MIM capacitors have not been included in the investigations, since as mentioned in section 3.3, their capacitance is dependent mainly on their oxide thickness and their geometric characteristics, which changes are assumed to be negligible under moderate stress levels applied in this work. The stress independence of the integrated MOS based capacitors, which are engineered to remain in accumulation for the allowed voltage ranges specified for the device ($\pm 3.3$ V), is presented in figure 6.15. The capacitance should be equal to the oxide capacitance, as shown in table 2.2, since the stress-dependent depletion capacitance is not rising. Therefore, the deployed capacitors are solely dependent on their geometry characteristics. Here, capacitors with four different geometries (recall section 5.1) have been experimentally characterized under diverse stress levels and the stain-induced changes of the capacitance are drawn. The observed strain-induced changes are less than 0.5 % and thus assumed negligible. The observed changes are mostly due to parasitic capacitances and have been caused by the use of the bending apparatus on the chip-in-foil. In order to achieve a stress independent response, the design guideline proposed here is to make use of circuit topologies referring to capacitor ratios and not absolute capacitor values. The capacitor ratio, i.e, $\Delta\frac{C_1/C_2}{C_1/C_2}$ will be less sensitive to mechanical stress w.r.t. the sensitivities of the capacitors $C_1$ and $C_2$, under the assumption that the strain-induced changes on both capacitors are similar.

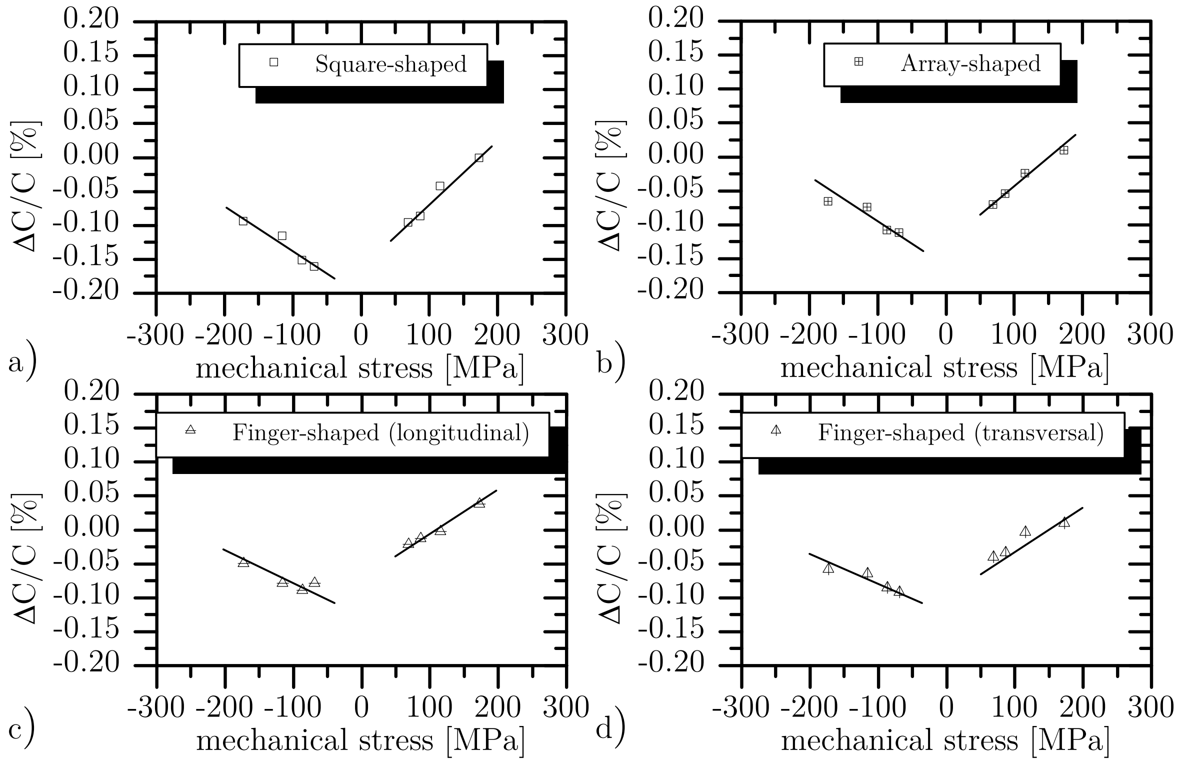


***Figure 6.15: Strain-induced changes on MOS based integrated capacitors under uniaxial* [110] *mechanical stress.*** *a) Square-shaped capacitor. b) Array-shaped capacitor. c) Finger-shaped capacitor with a* 0° *orientation (longitudinal). d) Finger-shaped capacitor with a* 90° *orientation (transversal).*

## 6.3 Strained MOS Transistor

The characteristics of the integrated MOSFET have also been investigated under mechanical stress. Electrical characteristics such as input and output characteristics as well as the subthreshold slope and the threshold voltage have been experimentally determined under strained conditions. The influence of the thinning and encapsulation techniques on the electrical behavior has been also studied. Transistor noise levels under strained conditions have been investigated and will be presented. The MOSFET piezoresistive coefficients under [110] uniaxial mechanical stress have been determined for the two mainly utilized channel orientations, 0° and 90° w.r.t. the direction of the applied stress. Furthermore, for minimization of the piezoresistance effect directly on the device level, circular gate transistors have been measured under mechanical stress and the results will be presented next.

Before presenting the piezoresistive characteristics of MOSFETs, the influence of

the thinning (DbyT) and encapsulation technique will be put forward. Figure 6.16 presents the input and output characteristics of a $W/L = 40/10$ nMOSFET and a $W/L = 40/10$ pMOSFET before and after the thinning and encapsulation procedures.

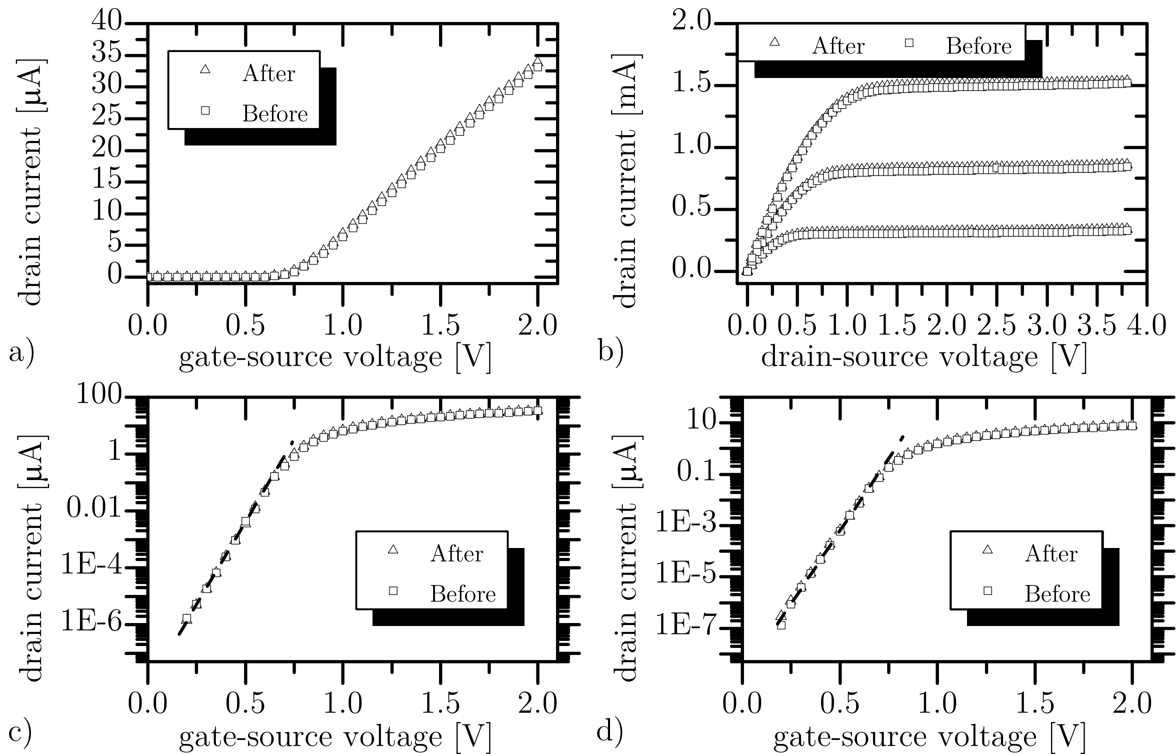


***Figure 6.16: Influence of microsystems technology on device characteristics.*** *In a) and b) nMOSFET input and output characteristics before and after performing the thinning and encapsulation techniques are presented. Note the negligible changes on the drain current and the threshold voltage. In c) and d) logarithmic input characteristics of a 40/10 nMOSFET and a 40/10 pMOSFET are presented. Note the constant subthreshold slope with a dashed line.*

Both input and output characteristics face negligible shifts. The maximum drain current change in the output characteristics for both n- and pMOSFET is $< 4$ %. The extracted threshold voltage as well subthreshold slope exhibit a $< 1$ % shift after thinning and encapsulation is performed. These changes are small and considered to be negligible, since the main reason of these shifts are the different measurement conditions, attributable to the encapsulation technique. The measurements of the rigid chips are performed on wafer level with the use of probes, where measurement needles are directly placed on the chip pads. However, in the case of the thinned chip-in-

foil the chip pads are contacted over conducting paths on the PI foil and the PI foil through a PCB connector and 1 m long cable to the measurement instrument. All these components exhibit a resistance in series with the device to be measured, which will influence the applied voltage on the actual device terminals.

Next, the piezoresistive behavior of the input and output characteristics will be presented. In figure 6.17 the input and output characteristics of MOSFETs under mechanical stress are depicted.

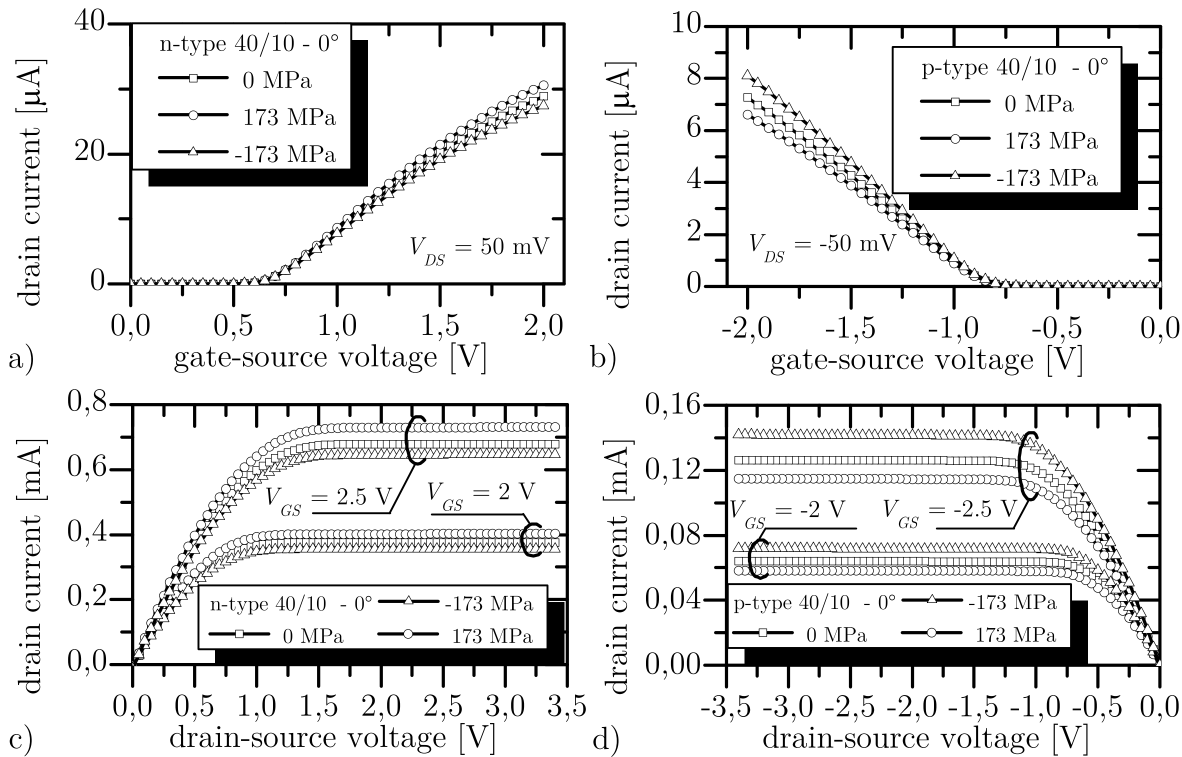


***Figure 6.17: Input and output characteristics of* [110] *uniaxially strained MOSFETs.*** *In a) and b) a 40/10 nMOSFET with a* 0° *channel orientation (longitudinal) is presented. In c) and d) characteristics of a 40/10 pMOSFET with a* 0° *orientation (longitudinal) are shown. Positive stresses denote tension, while negative ones compression.*

Both transistors channels are oriented in parallel with the applied stress direction (0° - longitudinal). The characteristics are shown for comparison purposes under strain-free (relaxed) and strained conditions. It is made clear, that the strain-induced drain current change depends on both the MOSFET type and the channel orientation. As will be shown later the strain-induced drain current changes depend slightly on the

operation point of the transistor and are significantly influenced from the parasitic drain-source resistance.

Before proceeding to the extraction of the piezoresistive coefficients of n- and p-type MOSFETs, data on the stress independence of the channel length modulation parameter $\lambda$ will be given. Here, a linear regression in the saturation regime of the output characteristics of [110] uniaxially strained MOSFETs has been performed. Thereby the early voltage $|V_A| = |1/\lambda|$ has been extracted and listed in table 6.1. For both n-type as well as p-type short channel transistors the strain-induced changes of the channel length modulation parameter $\lambda$ are less than |1 %| for [110] uniaxial mechanical stress and thus less significant than strain-induced mobility changes. Hence, $\lambda$ will be considered as a stress independent parameter within the applied mechanical stress range.

***Table 6.1: Strain-induced changes of the channel length modulation parameter of 10/0.4 strained MOSFETs.***

| MOSFET type | $\lvert\lambda\rvert$ [V$^{-1}$] @ 0 MPa | $\lvert\lambda\rvert$ [V$^{-1}$] @ 146 MPa | $\frac{\Delta\lambda}{\lambda}$ [%] |
|---|---|---|---|
| n-type longitudinal | 0.1149 | 0.1138 | -0.96 |
| n-type transversal | 0.1098 | 0.1093 | -0.46 |
| p-type longitudinal | 0.1062 | 0.1068 | 0.56 |
| p-type transversal | 0.1222 | 0.1223 | 0.10 |

With the help of equations (3.4.4) and (3.4.5) one can extract the longitudinal and transversal piezoresistance coefficients $\pi_L$ and $\pi_T$ by calculating the measured strain-induced changes $(I_{D,strained} - I_{D,relaxed})/I_{D,relaxed} = \Delta I_D/I_D$ and plotting them against the applied [110] uniaxial mechanical stress. This can be performed for different gate-source $V_{GS}$ and drain-source voltages $V_{DS}$, defining the point of operation. Figure 6.18 presents the strain-induced drain current changes of a 40/10 nMOSFET and a 40/10 pMOSFET with 0° and 90° channel orientations under compressive and tensile uniaxial [110] mechanical stress in the linear region of operation.

The piezoresistive coefficients are calculated from the slopes of the lines in the figures and are summarized in table 6.2, while compared with other values found in open literature.

***Table 6.2: Comparison of piezoresistive coefficients of n-type and p-type MOSFETs in literature.*** *The coefficients reported in* [GRG+03] *refer to bulk silicon chips.*

| Coefficient | this work | | Wacker et al. [WRSB08] | | Gallon et al. [GRG+03] | |
|---|---|---|---|---|---|---|
| $[(\mathrm{TPa})^{-1}]$ | nMOS | pMOS | nMOS | pMOS | nMOS | pMOS |
| $\pi_L$ | 375 | −649 | 478 | −637 | 485 | −600 |
| $\pi_T$ | 219 | 366 | 134 | 409 | 212 | 383 |

Furthermore, it was found that the threshold voltages for both NMOS and PMOS transistors do not show significant changes under stress within the applied mechanical stress range, therefore, threshold voltage is assumed to be a stress independent parameter. This result is in good agreement with results given [LTF04]. These small threshold variations found do not exceed the 0.3 % change for all bending configurations. Figure 6.19 shows the strain-induced threshold voltage shifts of a p-type 40/10 and an n-type 40/10 MOSFET.

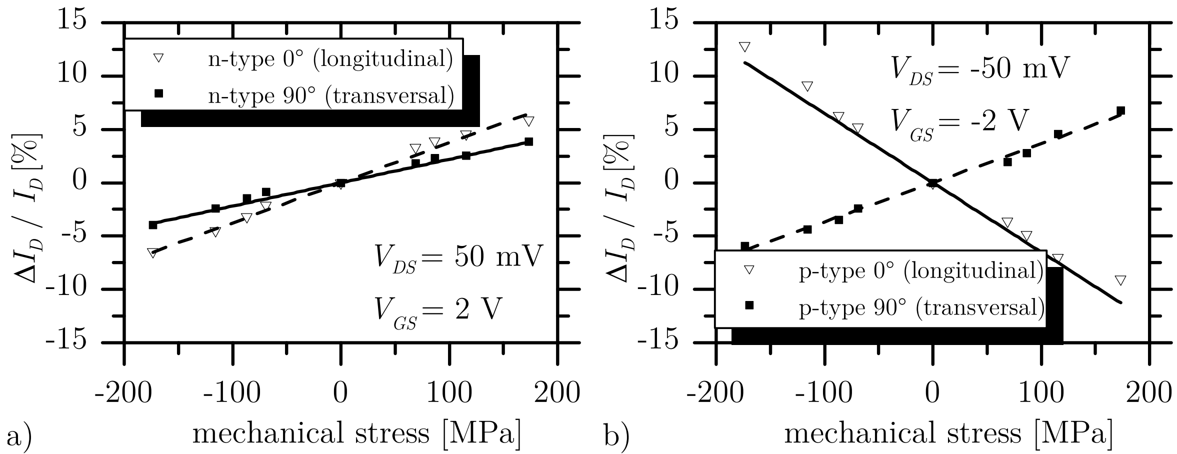


***Figure 6.18: Strain-induced drain current changes in the linear region of operation.*** *a) A 40/10 nMOSFET with 0° and 90° channel orientations. b) A 40/10 pMOSFET with 0° (longitudinal) and 90° (transversal) channel orientations.* $|V_{GS}| = 2$ *V and* $|V_{DS}| = 50$ *mV.*

The dependence of the piezoresistive coefficients on the operational point of the transistor is presented next. The change of the piezoresistive coefficients for both nMOSFETs and pMOSFETs is less sensitive on drain-source voltage $V_{DS}$ changes. The dependence on $V_{DS}$ is mainly observed in the linear region of operation. Furthermore, the dependence of the piezoresistive coefficients for both transistor types

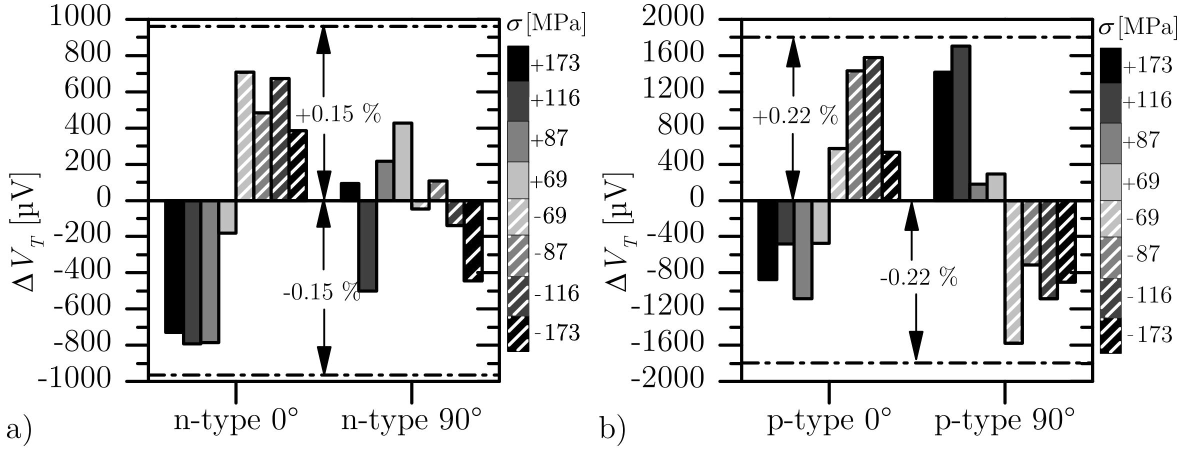


***Figure 6.19: Strain-induced threshold voltage changes of a 40/10 nMOSFET and a 40/10 pMOSFET.*** *a) With* 0° *channel orientation (longitudinal). b) With* 90° *channel orientation (transversal). Note how the changes do not exceed* 0.3 %.

on the gate-source voltage $V_{GS}$ is more significant. The reason of this behaviour has been experimentally observed in the literature before [Dor71] and has been attributed to the quantization of energy levels in silicon inversion layers [Dor71]. This quantization causes generally an occupation anisotropy of the valleys, which in turn affects the population of the conduction subbands as well as the intervalley scattering. Figures 6.20 and 6.21 illustrate the dependence of the longitudinal $\pi_L$ and transversal $\pi_T$ piezoresistive coefficients of pMOSFETs and nMOSFETs on the drain-source $V_{DS}$ and gate-source voltage $V_{GS}$. Additionally, the piezoresistive coefficients depend on the temperature. Figure 6.22 presents the temperature dependence of the longitudinal $\pi_L$ of a p-type 40/10 transistor. The absolute value of longitudinal coefficient is reduced by the increasing temperature, which agrees well with results in the open literature [CJS08].

Furthermore, the subthreshold slope under various bending configurations has been analyzed and depicted in figure 6.23. For long transistors no significant change is observed. This result can be also explained for long transistors as following. Recall that the subthreshold slope $S$ is given by (2.2.37). Assuming that geometrical changes of the gate oxide under the applied moderate stress levels can be neglected, the oxide capacitance $C_{OX}$ remains constant under the application of mechanical stress. The depletion

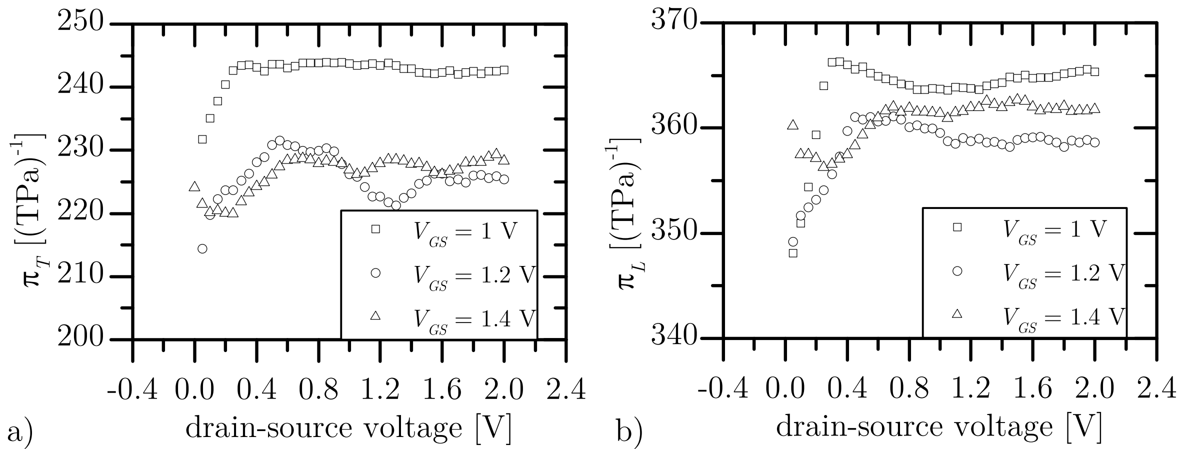


***Figure 6.20: Dependence of piezoresistive coefficients on the operational point ($V_{GS}$, $V_{DS}$) of a 40/10 nMOSFET.*** *a) Transversal $\pi_T$ coefficient. b) Longitudinal $\pi_L$ coefficient. Note how the coefficients exhibit a reduced sensitivity on the applied drain-source voltage $V_{DS}$.*

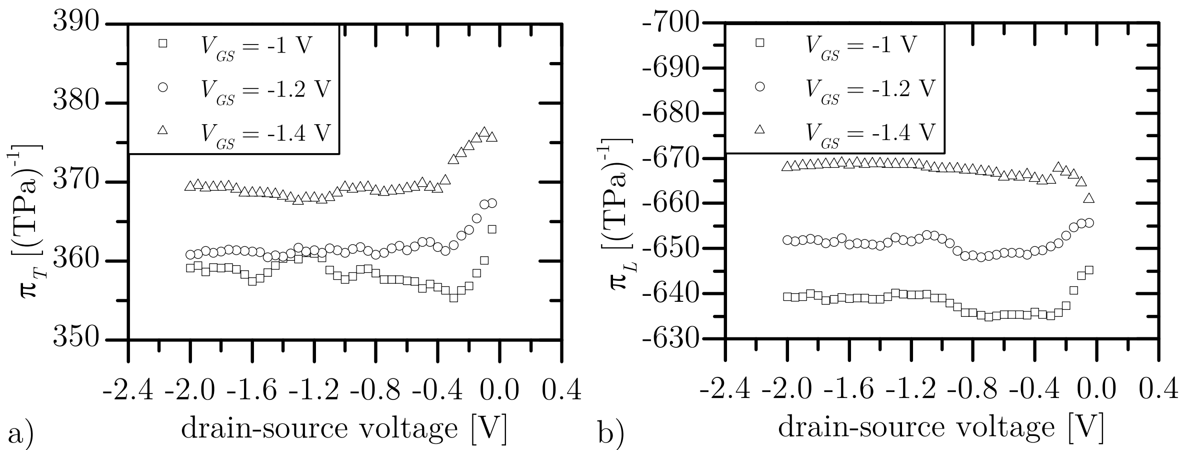


***Figure 6.21: Dependence of piezoresistive coefficients on the operational point ($V_{GS}$, $V_{DS}$) of a 40/10 pMOSFET.*** *a) Transversal $\pi_T$ coefficient. b) Longitudinal $\pi_L$ coefficient. Note how the coefficients exhibit a reduced sensitivity on the applied drain-source voltage $V_{DS}$.*

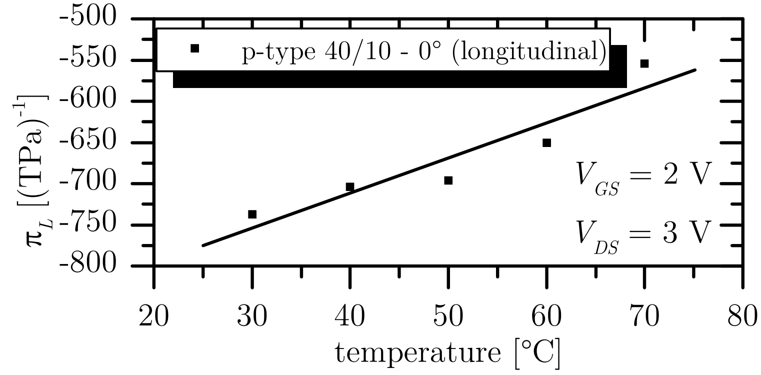


***Figure 6.22: Dependence of the longitudinal piezoresistive coefficient on temperature of a 40/10 pMOSFET.***

capacitance $C_D$ in weak inversion can be expressed for nMOSFETs as follows [SN10]:

$$C_D = \epsilon_s \left( \sqrt{\left(\frac{\epsilon_s}{C_{OX}}\right)^2 + \frac{2\epsilon_s V_{GS}}{qN_D}} - \frac{\epsilon_s}{C_{OX}} \right)^{-1} \tag{6.3.1}$$

where $\epsilon_s$ stands for the permittivity of silicon, $V_{GS}$ is the gate-source voltage, and $C_{OX}$ is the gate oxide capacitance. Using equation (6.3.1) can be clearly stated, that the depletion capacitance $C_D$ in weak inversion is also stress independent. Thus, and with the help of (2.2.37), the subthreshold slope for long transistors should also remain constant under the application of moderate stress levels. Similar results are valid for pMOSFETs and have been published in [HMD$^+$12] and [Lor12].

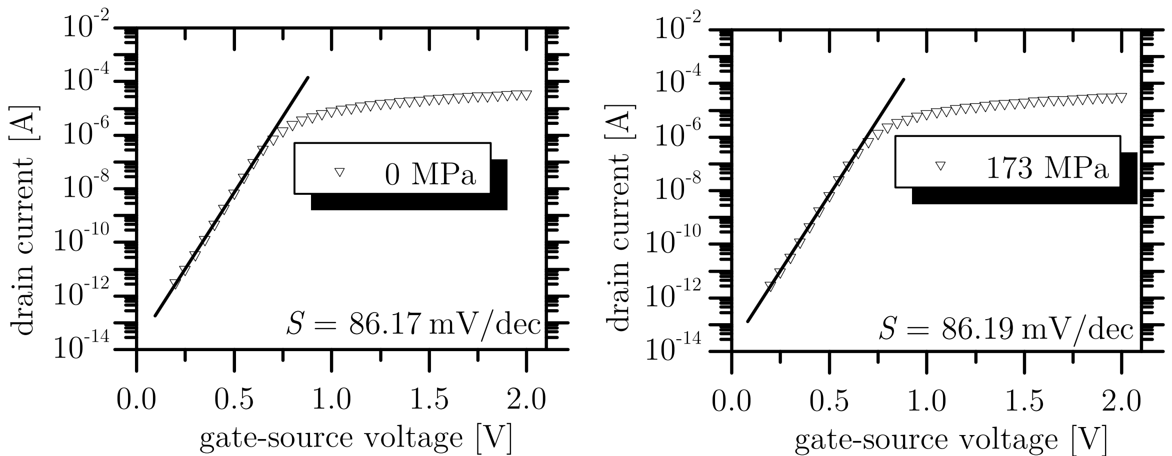


***Figure 6.23: Dependence of subthreshold swing of a 40/10 nMOSFET with a 0° channel orientation under uniaxial tensile* [110] *mechanical stress.***

The results until now have revealed that in spite of the strain-induced changes there are ways for minimizing the strain-induced influences in a circuit branch employing MOSFETs. For example, the use of longitudinal NMOS and transversal PMOS transistors in the same series circuit would be beneficial, since they exhibit almost similar piezoresistive characteristics (recall table 6.2). Thus, a common mode change would appear in both devices affecting the current through the circuit path, but keeping the voltage operational point on the devices constant. Moreover, the parallel connection of longitudinal and transversal p-type transistors would reduce the stress dependence of the entire parallel combination. This benefit arises from their positive and negative piezoresistive coefficients, respectively, as shown in table 6.2. In this direction, the idea of circular gate pMOSFETs has arisen, as presented in figure 5.4a. Instead of combining in parallel transversal and longitudinal pMOSFETs, the use of circular gate transistors must also exhibit a similar effect, since the drain current is forced to flow over all crystallographic directions on the (001) plane. The theoretical calculation of such a transistor structure is given in the Appendix and the result is that the piezoresistive coefficient of a round transistor should be:

$$\pi_{round} = \frac{\pi_{11}^{(v)} + \pi_{12}^{(v)}}{2} = \frac{\pi_L + \pi_T}{2} \approx 141 \ (\text{TPa})^{-1} \tag{6.3.2}$$

where $\pi_L$ and $\pi_T$ the longitudinal and transversal piezoresistance coefficients of linear gate pMOSFETs (table 6.2), respectively and $\pi_{11}^{(v)}$ and $\pi_{12}^{(v)}$ the piezoresistance coefficients of silicon in the main crystallographic coordinate system. This outcome makes clear that a round transistor should exhibit the same piezoresistive coefficient as the parallel combination of a longitudinal and transversal traditional transistors with linear gates. Two p-type transistors designed with round gates have been experimentally measured under tensile and compressive [110] mechanical stress and their drain-induced changes are depicted in figure 6.24. The obtained piezoresistive coefficients $\pi_{round}^{circle} = 76 \pm 52$ [(TPa)$^{-1}$] and $\pi_{round}^{donut} = 59 \pm 46$ [(TPa)$^{-1}$] are lower but very close though to the calculated piezoresistive coefficients taking into account also the measurement error. This is a very interesting result, since such transistors could be employed towards a stress independent circuit operation, such as the bandgap reference circuit of figure 5.4b, where the circuit uses only pMOSFETs, while the operational amplifier consists of a pMOSFET input differential pair and is biased using a p-type current source.

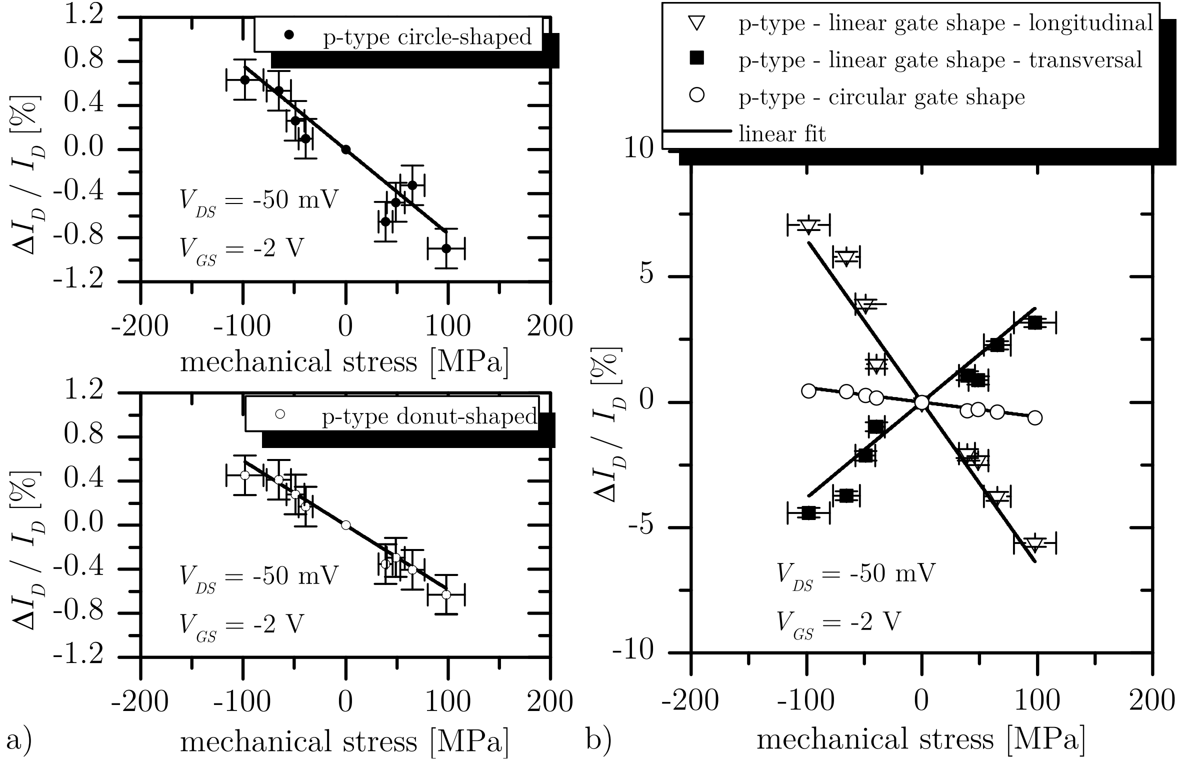


***Figure 6.24: Strain-induced drain current changes of round gate p-type transistors under uniaxial* [110] *mechanical stress.*** *a) Recall the two round gate transistors designed in this work (figure 5.4): the donut-shaped and the circle-shaped pMOSFET. b) Comparison of the traditional linear and the round gate format pMOSFETs regarding their piezoresistive behavior. All solid black lines are linear fit of the measured data.*

Another important aspect of the transistors employed in analog circuits is their 1/f noise characteristics. Since the drain-current changes under mechanical stress, the drain current noise power spectral density (PSD) $S_{ID}$ of MOSFETs has to follow these changes. Both n- as well p-type transistors have been measured under uniaxial mechanical stress in the setup of figure 5.12. The results on the 1/f noise of uniaxially strained nMOSFETs on ultra-thin chips are presented in figure 6.25. The 1/f noise changes of uniaxially strained pMOSFETs appear in figure 6.26. In the linear part of the measured noise PSD the exponent $\alpha$ and the noise magnitude at 1 Hz have been extracted and the frequency dependence of the drain current noise PSD changes has been calculated.

It can observed that in the case of nMOSFETs for higher frequencies there is a lower dependence of the noise PSD on the applied mechanical stress. Moreover, the 1/f noise

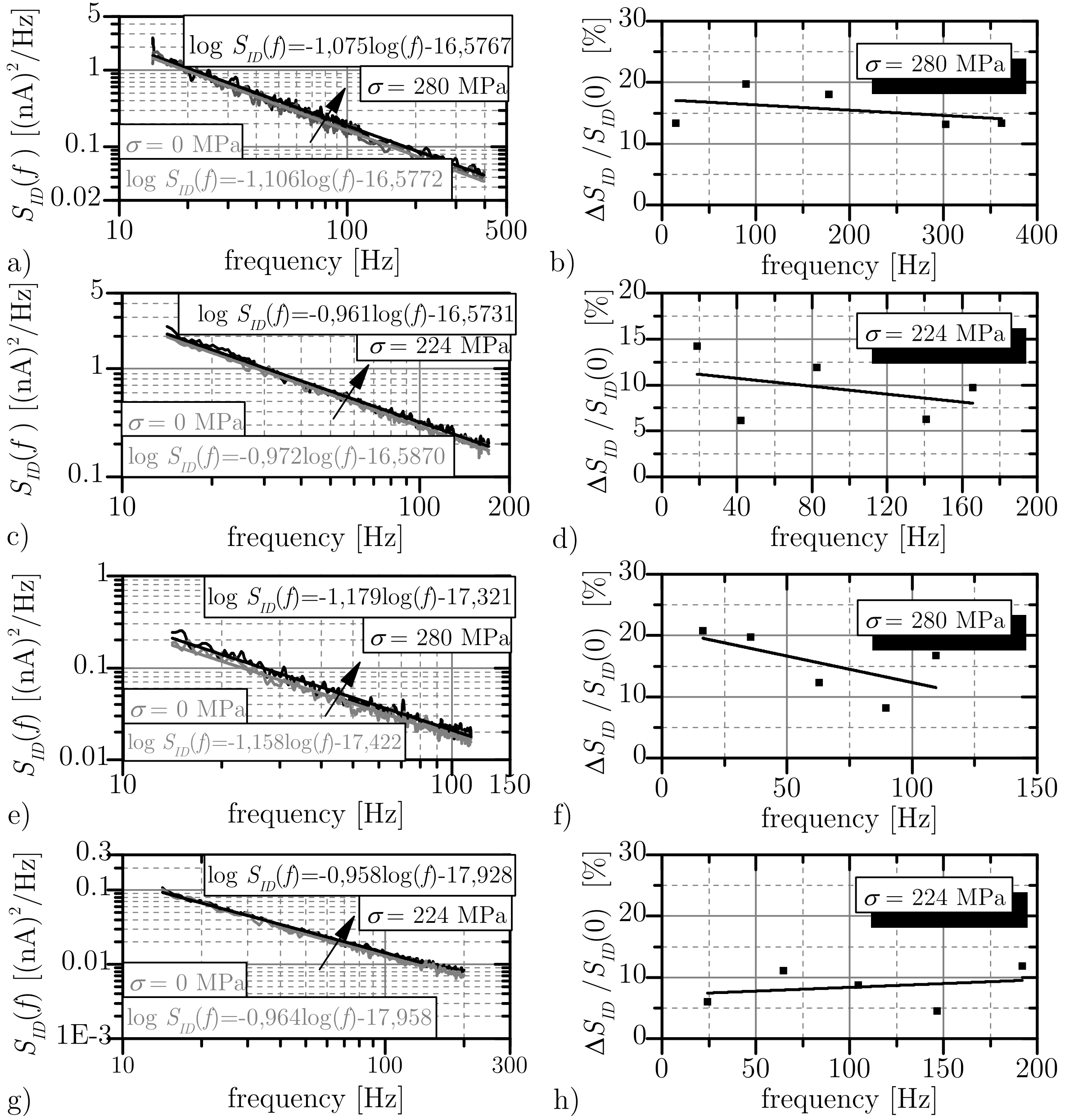


***Figure 6.25: Strain-induced changes on 1/f noise characteristics of n-type transistors under uniaxial* [110] *tensile mechanical stress.*** *a)-d) 1/f noise characteristics under relaxed and stressed conditions on the left and extracted drain current noise PSD relative changes versus frequency for an n-type 0° oriented 20/2 MOSFET. e)-g) Similar measurements for an n-type 90° oriented 40/10 MOSFET. Note the extraction of the noise magnitude $S_{ID}$ and exponent $\alpha$ from the logarithmic plots. Gray lines denote measured strain-free (relaxed) data, while black lines denote a strained condition. The lines on the plots are linear fits of the data.*

drain current PSD follows the strain-induced drain current changes, as presented in chapter 3. Namely, the noise PSD increases with tensile stress for nMOSFETs and decreases with compressive stress independent of the channel orientation. For p-type MOSFETs the noise PSD increases with compressive stress and decreases with tensile stress for a 0° channel orientation. For a 90° channel orientation of pMOSFETs the noise PSD increases with tensile stress and decreases with compressive stress. The results of the 1/f noise dependence follow the equation (3.4.11). The strain dependence of 1/f noise in MOSFETs is attributed to changes on both carrier trapping/detrapping and mobility fluctuations through strain-induced change in mobility, since the applied mechanical stress shifts the carrier subband levels in the inversion layer and changes the conductivity effective mass [LAT+09].

## 6.4 Bendable Image Test Sensors

Since the correlated double sampling readout circuit plays an important role in CMOS image sensors, it is necessary to verify the theoretical considerations of the compensating nature of the CDS circuit. For this reason the fabricated test image sensor which contains a CDS stage has been electrically and optically measured under different bending configurations. First, the stand-alone operation of the CDS amplifier itself has been investigated under stress (figure 3.10). It has been verified that the CDS amplifier under mechanical stress can be assumed as a stress independent circuit. Moreover, the chosen orientation of the transistors forming the amplifier itself (recall section 5.1) does not alter its stress independence. The results presented in figure 6.27 verify our design guideline, that negative feedback applied to the CDS circuit renders the circuit less sensitive to mechanical stress according to equation (3.6.3). This guideline applies not only to CDS circuits but to any switched-capacitor circuit employing negative feedback. It also applies to resistor feedback as long as it relies on resistor ratios. In case of capacitor-resistor feedback circuits, where both components may exhibit different stress sensitivities, this guideline would not render the circuit operation fully stress independent. The circuit designer has to wisely choose components with matched piezoresistive behavior (stress sensitivity), in order to achieve a low stress sensitivity of the entire circuit. The operation of the CDS circuit is as follows: At first the circuit is reset at $V_{bias,CDS} = 1.66$ V, while its input lies at $V_{in}^{\phi_1} = 0.66$ V. During the clock phase $\phi_2$ the input voltage lies at $V_{in}^{\phi_2} = 1.66$ V. According to equation (3.6.5)

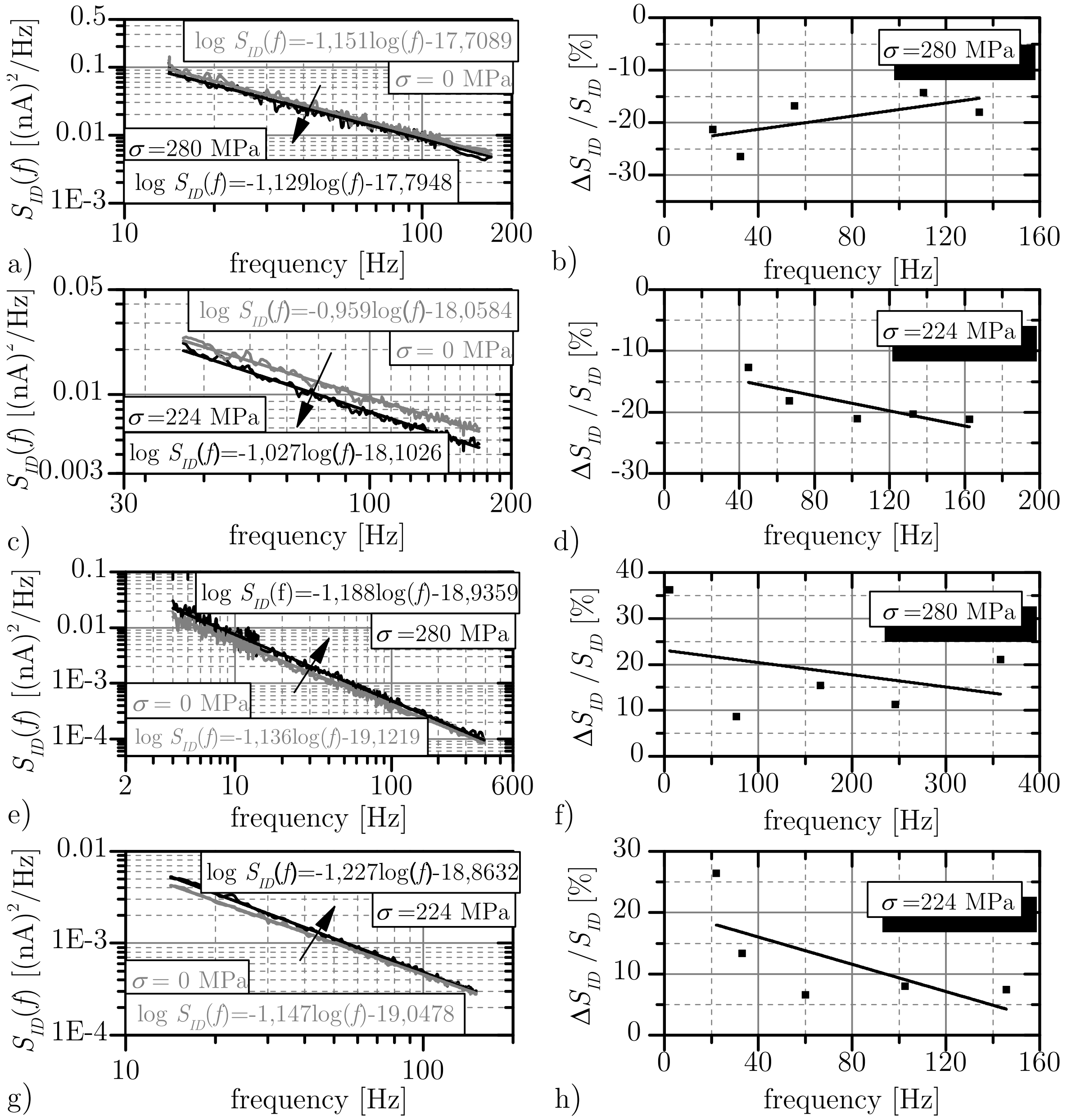


***Figure 6.26: Strain-induced changes on 1/f noise characteristics of p-type transistors under uniaxial* [110] *tensile mechanical stress.*** *a)-d) 1/f noise characteristics under relaxed and stressed conditions on the left and extracted drain current noise PSD relative changes versus frequency for a p-type 0° oriented 20/2 MOSFET. e)-g) Similar measurements for a p-type 90° oriented 40/10 MOSFET. Note the extraction of the noise magnitude $S_{ID}$ and exponent $\alpha$ from the logarithmic plots. Gray lines denote measured strain-free (relaxed) data, while black lines denote a strained condition. The lines on the plots are linear fits of the data.*

the CDS circuit output is proportional to the difference between the two applied input samples, which is added to the applied reference voltage $V_{ref} = 1.66$ V. Therefore the output yields around $V_{out} = V_{ref} + (V_{in}^{\phi_1} - V_{in}^{\phi_2}) = 660$ mV. Both under tension or compression, the output level of the circuit does not change significantly.

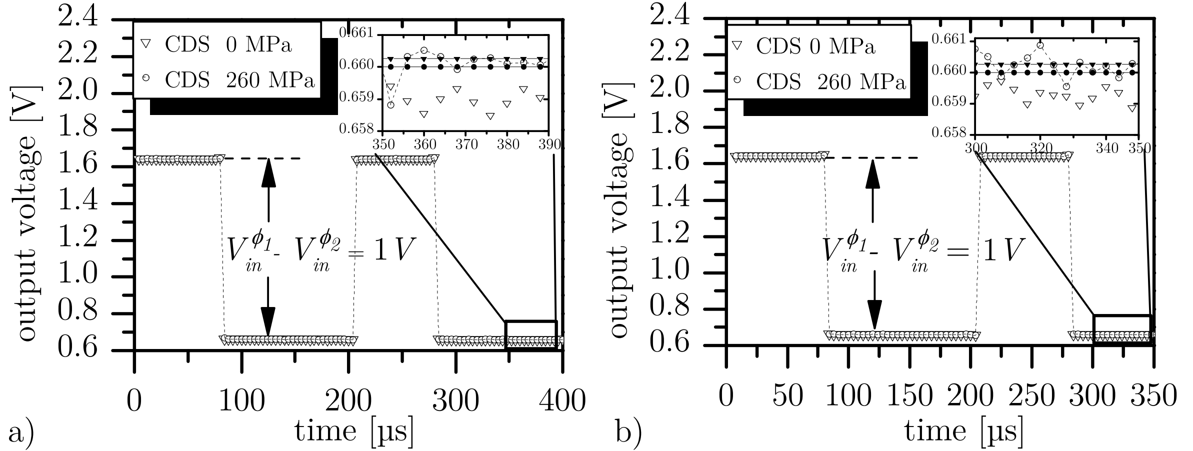


***Figure 6.27: Strain-induced changes on the CDS circuit output under 260 MPa uniaxial* [110] *mechanical stress.*** *a) CDS circuit employing internal nMOSFETs and pMOSFETs with the same layout orientation. b) CDS circuit employing internal nMOSFETs and pMOSFETs at a perpendicular layout orientation. Open symbols stand for experimental data, while closed symbols and solid lines for simulated data.*

Next, the output of a test image sensor incorporating the above presented CDS circuit will be investigated. For this purpose, the chip T95265B will be employed (figure 5.3), where the pixel circuits designed are read out using two independent column circuits. The one is utilizing the CDS concept and the other is based only on source followers (the in-pixel n-type SF and the column p-type SF - recall figure 5.3). That way the design guideline for the compensation of the strain-induced effects on the in-pixel source follower using the CDS circuit can be investigated. Under the same illumination and temperature conditions the pixel output with and without the use of the CDS circuit is monitored and compared utilizing the measurement setup of figure 5.16. Figure 6.28 shows these results, where can be concluded that the output signal with the use of the CDS circuit is less sensitive to the applied mechanical stress (a factor of 2-3). Note that the CDS circuit inverts the output signal when compared to the simple SF. This observation is valid for both tensile as well compressive stress, verifying our proposed design guideline i.e., the use of a CDS amplifier to readout the pixel allows a partial compensation of the strain-induced shifts on the in-pixel source

follower. The small changes observed under mechanical stress with the use of the CDS technique can be explained as follows. First, as we theoretically investigated the photodiode capacitance faces shifts around ±2 % under mechanical stress, which will arise at the output, as explained in section 3.6 and equation (4.3.1). Moreover, but less significant, inaccuracies of the measurement procedure, the illumination intensity and the ADC quantization add up to the final result.

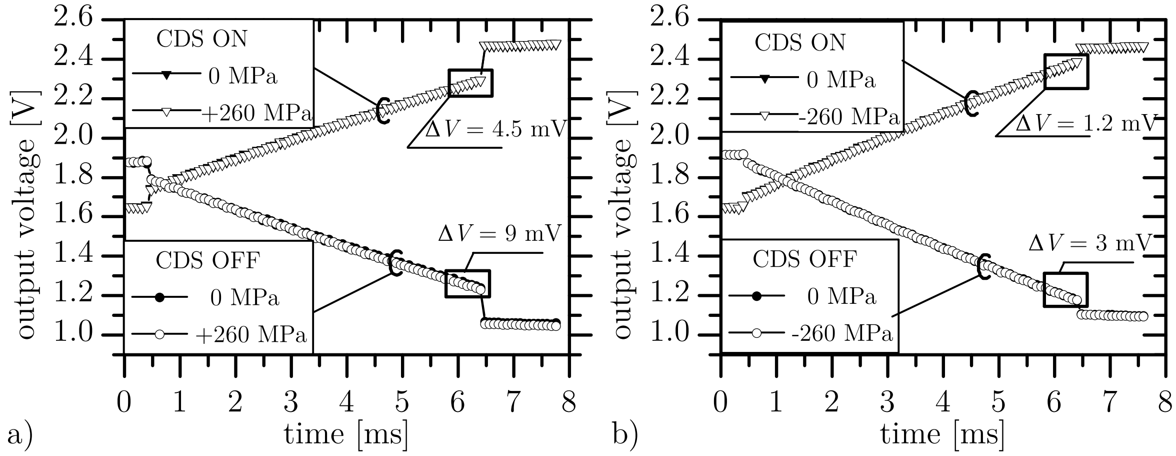


***Figure 6.28: Strain-induced changes of the pixel circuit response with and without employing the CDS concept output under ±260 MPa uniaxial* [110] *mechanical stress and illumination.*** *Closed and open symbols represent experimental data under strained and strain-free (relaxed) conditions, respectively.*

Utilizing the same chip (T95265B) another informative measurement can be performed, which will allow the verification of the dark current characteristics of photodiodes under mechanical stress, which where presented in section 6.1. Here, the pixel output utilizing the CDS concept under dark conditions can be investigated. From the slope $S$ of the pixel output over a long integration time $t_{int}$, the dark current generation rate can be extracted. Therefore, the dark current under strain-free (relaxed) and strained conditions can be compared. Here it has to be noted, that in the final measured result the strain-induced shift of the photodiode capacitance is superimposed on the strain-induced dark current changes:

$$S = \frac{\Delta V_{PD}}{t_{int}} = \frac{I_{dark}}{C_{PD} + C_s} \tag{6.4.1}$$

$$\Rightarrow \frac{1}{S}\frac{\partial S}{\partial \sigma} = \frac{1}{I_{dark}}\frac{\partial I_{dark}}{\partial \sigma} - \frac{1}{C_{PD} + C_s}\frac{\partial C_{PD}}{\partial \sigma} \tag{6.4.2}$$

Different pixel structures have been investigated under dark conditions and under diverse bending configurations. Figure 6.29 presents the experimental data of the strain-induced slope changes of a pixel response under dark conditions employing a n+/p photodiode (closed symbols). Here the increase of the slope $S$ is clear, indicating that the dark current under mechanical stress increases non-linearly. This result agrees well with the experimental results of the strain-induced changes of the dark current measured directly at pn-junction based photodiodes and presented in section 6.1 as well as with the exponential characteristic of the presented theoretical model (solid line in the figure). There is, however, a small mismatch between the theoretical and experimental data observed in the figure. This inaccuracy lies mainly in two reasons: a) the strain-induced shift of the photodiode capacitance, which is superimposed on the strain-induced dark current changes (equation (6.4.2)) and b) the measurement accuracy of the employed measurement techniques, since the measurement error is comparable with the very small changes to be measured ($1 - 3\%$). Indeed, let us assume the values for the strain-induced shifts of MOS and depletion-layer capacitance reported in [MK03] and [GPM02] respectively. Namely, a capacitance increase under moderate compressive stresses up to 2% is reported. Hence, using equation (6.4.2) the dark current change decoupled from the capacitance change can be corrected in order to represent strain-induced dark current changes. Therefore, employing this correction would shift the measurement data of figure 6.29 closer to the theoretically predicted characteristic (open symbols in the figure).

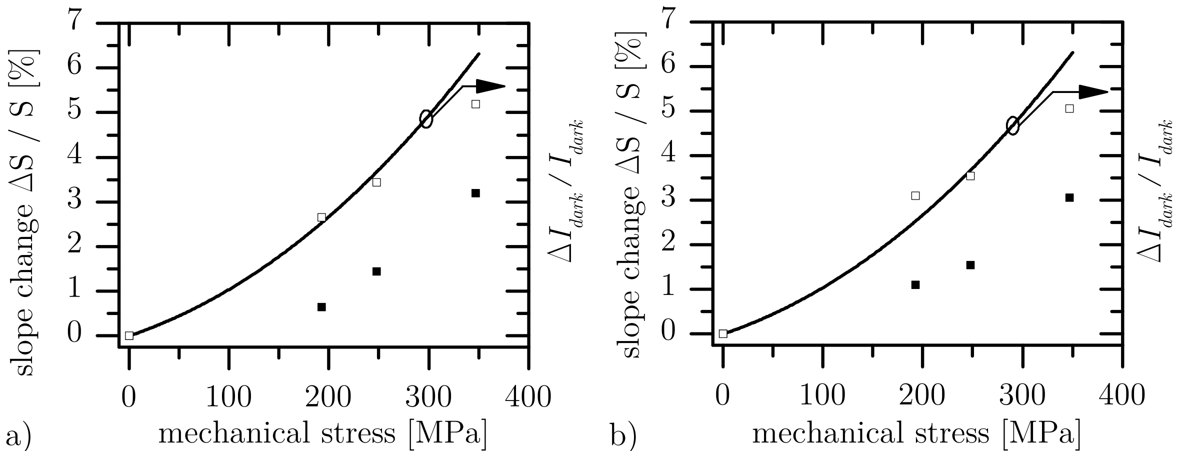


***Figure 6.29: Strain-induced changes of the pixel circuit response under dark conditions under uniaxial* [110] *mechanical stress.*** *Closed symbols represent measured data, while open symbols corrected data. The solid line represents the theoretical model of strain-induced dark current change.*

## 6.5 A Bendable Bandgap Voltage Reference

Having verified the compensation techniques for stress minimization in the readout electronics for image sensors, another vital circuit for any CMOS image sensor is a bandgap voltage reference. In section 4.5 the strain-induced changes of a widely used bandgap voltage reference topology have been already simulated. The changes have been explained and here experimental results verifying the simulations are put forward. The topology shown in figure 5.4 has been integrated on the T95265C chip and has been thinned down to 20 µm. The circuit has been tested in a similar setup as the one of figure 5.14 under varying temperature and mechanical stress. Figure 6.30 presents the experimental results of two different chips. Here, it has been verified that the mechanical stress actually amplifies the mismatch induced drain-current difference in the two main circuit branches. That way the application of mechanical stress does not shift the temperature characteristic in a predefined manner, but depends on the initial mismatch on the input transistor of the utilized operational amplifier. This is the reason why under the application of uniaxial compressive (or tensile) stress the shift of the characteristics is not toward the same direction when comparing two tested chips. Moreover, the magnitude of the changes is different in these two cases (11 mV vs. 17 mV). Recall the simulation results showing the same trends for the shift direction as well as for the shift magnitude and presented in figure 4.18.

## 6.6 A Flexible CIS for Bendable Applications

In the scope of this work a flexible image sensor chip has been designed featuring all techniques that have been proposed for a stress independent operation. The chip incorporates a 1200 × 200 active pixel matrix and is 2 cm long so that it can be wrapped around a cylinder rod and demonstrate its ability for panoramic imaging. Figure 6.31 shows a system overview of the fabricated sensor, while 6.32 shows the fabricated chip wire-bonded on a custom PCB. Digital circuits control the pixel matrix and can implement both a rolling shutter as well a global shutter readout technique. Moreover, the system can be configured so that either the entire or only a part of the pixel matrix can be read out. The pixel circuit design deployed here is based on a standard n+/p p-n junction based photodiode with a pMOSFET reset transistor and an nMOSFET based source follower, biased through a current mirror configuration. The

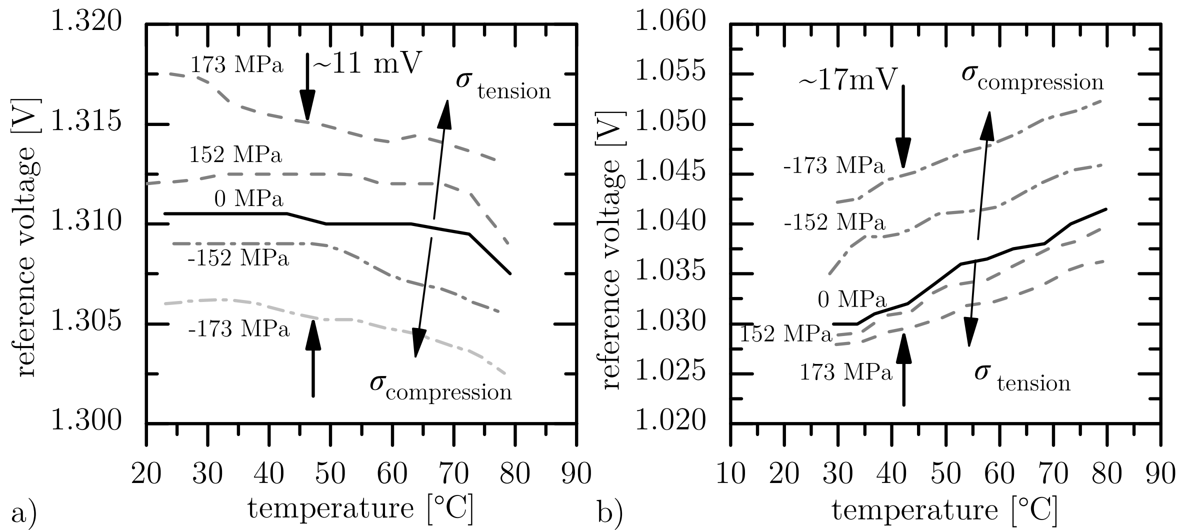


***Figure 6.30: Strain-induced changes of the bandgap voltage reference circuit under uniaxial* [110] *mechanical stress and varying temperature.*** *Solid black lines represent data under strain-free (relaxed) conditions. Dashed gray lines represent data under uniaxial tensile stress, while dash-dotted gray lines represent data under uniaxial compressive stress. Note the different trends of the shift of the characteristic among the two chips for the same mechanical stress direction.*

analog circuitry employed is based on the verified stress independent readout chain (recall 3.11). After the CDS stage, which is compensating the strain-induced shifts of the in-pixel SF, a S/H stage follows. The S/H stage is based on a negative capacitor feedback operational amplifier topology. Both CDS and S/H stages are based on ratios of capacitors, in order to minimize any stress-induced effects on the capacitance. The design splits the 1200 columns into 12 blocks of 100 columns each. Every block contains 10 multiplexers (first multiplexing stage) and 10 unity-gain buffers (precharge stage), based on a folded cascode topology. Through the first multiplexing stage each 100 columns are multiplexed to 10 outputs, each of one feeds the input of the block buffer. However, the inputs of each multiplexer are 10 interdigitated inputs, so that the first multiplexer is fed with column outputs (1,11,21...91), the second with column outputs (2,12,22...92) and the tenth with (10,20,...100). Through the employed interdigitation subsequent columns are redirected to different block buffers and thus the S/H stage of subsequent columns can precharge the line up to the buffer, before the value of this column is needed for the output (precharging stage). Each of the block buffer drives the long line up to the output multiplexing stage. Here a multiplexer connects one of the 120 block buffer outputs into the differential output amplifier, which drives the output pads. A more detailed description of the chip and the design, simulation and

timing results as well as layout considerations have been published in [Kle12].

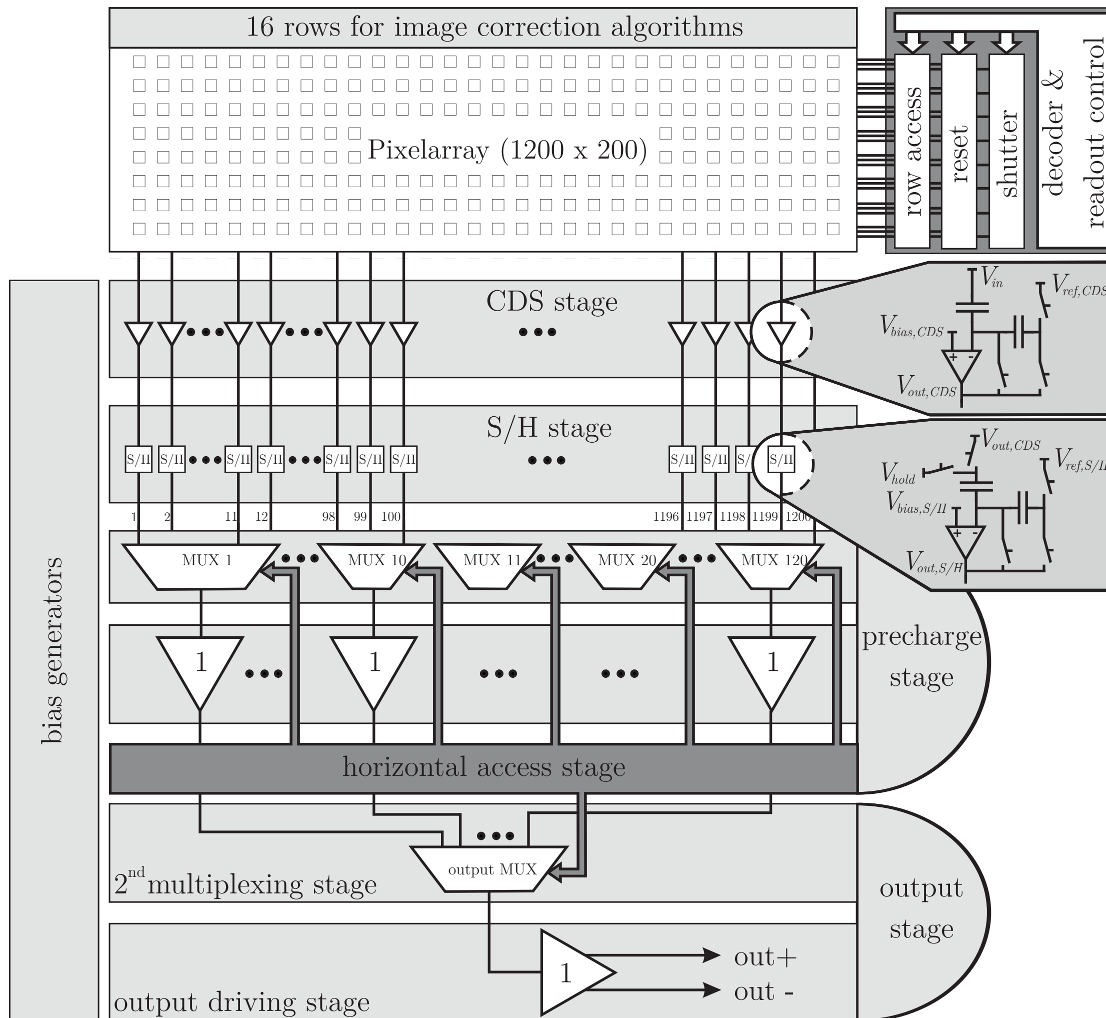


***Figure 6.31: System overview of the designed and fabricated CMOS image sensor.*** *Dark gray blocks are digital logic, while light gray represent analog circuitry.*

## 6.7 Synopsis

In this chapter the experimental results obtained in this work have been presented. Electrical characterization of p-n junction based photodiodes under mechanical stress showed that the dark current increases under tensile mechanical stress, while it decreases slightly under compressive mechanical stress. A temperature dependent piezo-junction coefficient has been extracted. The optical characteristics of the strained

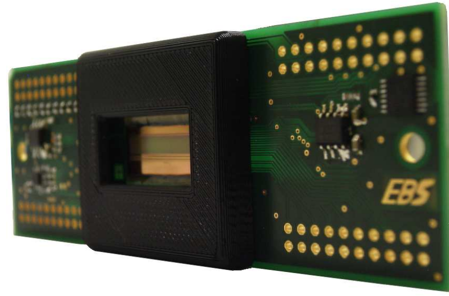


***Figure 6.32: Chip-on-board: The 750 $\mu$m thick, solid version of the fabricated image sensor wire-bonded on a PCB board for test purposes.*** *The black cover is a 3D-printed part providing protection to the bare chip and bonding wires.*

photodiodes in the visible spectrum are not influenced by mechanical stress. Similarly, uniaxially strained MOS capacitors show only slight, in fact negligible changes, under the application of uniaxial [110] mechanical stress. However, MOS transistors shift their DC characteristics significantly. Strain-induced drain current changes have been measured and the piezoresistive coefficients of the MOS transistors of the process used have been extracted. Their temperature dependence as well as their dependence from the chosen operational point has been demonstrated. Integrated circuits employing techniques toward a stress independent operation have been designed and measured and the proposed design techniques have been verified. A flexible bandgap voltage reference has been also designed and measured and its operation under mechanical stress has been verified in comparison with the simulation results. Based on the accomplished results, the design of the first monolithic CIS for bendable applications has been presented.

# Chapter 7 - Discussion

In the last chapter a discussion on the results obtained in this work and on potential applications of the fabricated flexible image sensor will be put forward. In section 7.1 design and layout guidelines will be presented, assisting the analog IC designer to design integrated circuits operating mechanical stress independently. Section 7.2 presents potential applications of the flexible image sensor concept. Further investigations based on the outcome of this work are proposed in section 7.3 targeting a transition from research into a potential product development.

## 7.1 Guidelines for a Stress Independent Circuit Operation

In this section design and layout guidelines for a stress independent circuit operation will be presented. The analog designer of flexible integrated circuits should first gain insight of the piezoresistive behavior of the devices utilized in the design. Characterizing the process under mechanical stress and extracting all piezocoefficients of integrated resistors, capacitors, MOSFETs and bipolar transistors would lead to accurate minimization techniques of the circuit stress dependence. Next, circuit- or system level stress dependence minimization or compensation techniques are listed.

1. Dynamic offset cancellation techniques (such as autozeroing or correlated double sampling) should be employed for stress independence. The input referred offset of an amplifier is a stress dependent quantity and its dynamic cancellation proves to be essential for minimization of the stress dependence. Recall the correlated double sampling amplifier presented in this work in sections 3.6 and 6.4.

2. Moreover, in image sensors the use of the CDS technique suppresses the shift of the in-pixel SF output, which is caused due to the piezoresistive behavior by the employed MOS transistors.

3. Circuits based on amplifiers employing negative feedback, such as switched-capacitor circuit techniques exhibit a significantly reduced stress dependence. The open loop gain of an amplifier is a stress dependent quantity. Thus incorporating the amplifier in a feedback loop the closed loop characteristics exhibit a reduced sensitivity on strain-induced changes.

4. Device characteristics typically shift under the application of mechanical stress. Therefore, utilizing circuit topologies based on absolute values of device characteristics is not recommended. Referring to ratios of device parameters is a way to minimize the stress dependence arising from strain-induced shifts of device characteristics.

5. Sample and hold circuits with a minimized stress dependence should not be implemented (as typically done) utilizing a SF amplifier, a capacitor and a transmission gate. For a stress independent operation, operational amplifier based S/H circuit topologies should be used. Moreover, topologies employing ratios of sampling and holding capacitors (recall section 3.6) are beneficial.

6. For a reduced sensitivity on bandgap voltage reference sources, the use of bipolar transistors exhibiting the smallest strain-induced changes is recommended. Moreover, in classical topologies such as the one presented in this work, the employed amplifier needs to be designed accurately targeting a reduced input offset. To reduce the amplifier stress dependence, circular gate pMOSFETs or a parallel connection of longitudinal and transversal pMOSFETs are recommended for use (input stage as well as biasing) due to their significantly reduced stress sensitivity when compared to traditional linear gate transistors.

7. The designer can use toward his/her benefit the fact that stress sensitivity of many devices changes sign for different layout orientations. This is the case for example with resistors and pMOSFETs. Here, combining resistors in series with different signs of stress sensitivity can minimize (or even cancel) the stress dependence of the overall series combination. Similarly, combining pMOSFETs with different orientations in parallel can lead to an increased stress independence of the parallel combination. Circular gate transistors with their decreased stress sensitivity are actually inherently utilizing the latter observation.

8. For circuit branches consisted of MOS transistors the designer can choose the proper transistor orientations, which will lead to either a common mode operational point shift under mechanical stress or to a differential change. As an example, a circuit branch with one pMOSFET and one nMOSFET in series could be designed in two ways: a) Either the voltage at the drains of the transistors remains stress independent utilizing transistor orientations exhibiting common mode changes under mechanical stress or b) the current flowing through the

branch is designed to remain stress independent utilizing transistor orientations exhibiting differential changes under mechanical stress.

9. Designers of image sensor pixels utilizing standard p-n junction based photodiodes should take into consideration the strain-induced shift of the p-n junction capacitance $C_{PD}$. In topologies where an in-pixel storage capacitor $C_s$ is utilized, the stress dependence of the pixel output can be minimized by employing a storage capacitor fabricated as an MOS-based or PIP capacitor, which both are stress independent (recall section 3.3). This observation is based on equation (3.6.6) where $C_s$ and $C_{PD}$ are added. In topologies employing pinned photodiodes (PPDs), where the charge-to-voltage conversion is being done at the floating diffusion node, this technique will not help. If, however, the goal is a stress independent operation a second matched floating diffusion could be integrated, in order to track its stress dependence.

10. Employing a stress independent flexible image sensor in a compressive configuration is preferred w.r.t. the strain-induced dark current shift. As shown in this work, under moderate compressive uniaxial mechanical stresses the dark current of p-n junction based photodiodes is decreasing and the PD capacitance shift is also lower.

## 7.2 Potential Applications

In this section potential applications of the developed flexible image sensor are briefly presented. Curved image sensors open up new vistas not only for research but also for novel consumer and medical applications.

Flexible image sensors could be for instance exploited in medical endoscopy or catheterization instruments. A flexible monolithic CIS similar to the one developed in this work, could be wrapped around the body of a conventional endoscope or a capsule endoscope. That way it could provide important panoramic information of hidden cavities that a conventional endoscope with a single forward looking image sensor on its tip would miss. Due to the close proximity of the endoscope to the vascular walls, the esophagus or the gastro-intestinal tract no imaging optics would be required. Figure 7.1 demonstrates the concept of the flexible CIS mounted around a conventional endoscope body or a capsule endoscope. A similar setup has been presented

in [MHvdHD13], where several rigid dummy chips (with a thickness of 300 µm and thus not bendable) have been mounted around the body of a 2 mm diameter catheter. However, replacing all the rigid dummy chips by one monolithic flexible sensor is advantageous in terms of cost, hardware control units and data acquisition units required to readout the sensors. Moreover, a lower power consumption can be achieved and the interconnection density can be significantly reduced.

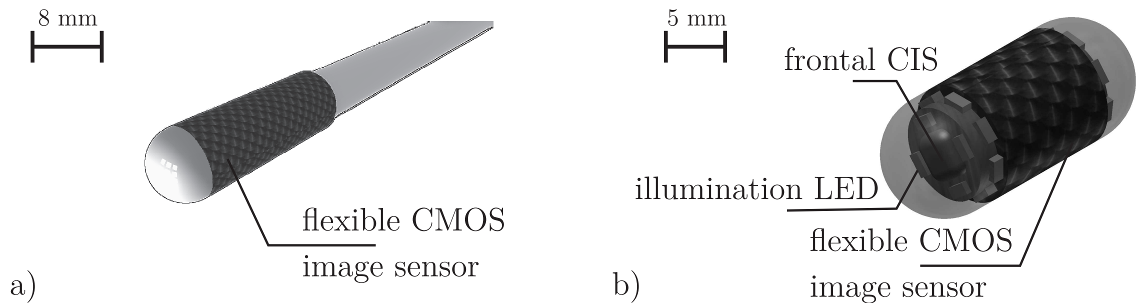


***Figure 7.1: Application concept of the flexible CIS in biomedical engineering.*** *a) Wrapped around a 9mm-diameter conventional endoscope. b) Wrapped within a 10mm capsule endoscope.*

Furthermore, in medical or biological research exciting application fields arise utilizing flexible CISs, such as panoramic biofluorescence imaging. Detection of fluorescence is a widely used measurement in biology and is typically performed by employing an imaging system deploying flat rigid CCD sensors. In this technique, a biological sample is tagged with fluorescent indicators, which after external optical excitation emit at a certain light wavelength. The emitted wavelengths are forwarded through an optical system (optical microscope or optical lenses) to the CCD sensor, where the imaging takes place. In the past years, genetically encoded fluorescent $Ca^{2+}$ indicators (GECIs) have been developed and targeted to cells or immobilized subjects in order to monitor their brain activity. This is performed by monitoring changes in the intracellular calcium concentration, which represents a valuable indicator for neural activity [THM+09] [FS03] [VKV+11]. After optically evoking the described calcium sensitive fluorescent indicators their emission characteristics shift with changes in the calcium concentration. The shifts on the emitted wavelengths are being again monitored by an optical system employing CCD sensors. For the proposed fluorescent applications the flexible image sensor can be used in two ways: a) Directly on or in the living organism for *in vivo* studies. b) Forming a panoramic imaging system of fluorescent emission. In the former concept, a flexible CIS could be conformed directly on tissues or organs of

living organisms. For instance, a flexible image sensor can be mounted directly on a mouse brain or wrapped around a fly brain and in combination with fluorescence techniques monitor its brain activity. Both application concepts are depicted in figure 7.2. Rigid CMOS image sensors performing such applications have been recently reported in literature [OHP+13]. Flexible image sensors mounted directly on or wrapped around the subject can assist toward continuous optical monitoring in fully conscious, mobile subjects. Moreover, mounting the image sensor under the subjects tissue is advantageous, since absorption and scatter of the emitted light by the subject tissue is avoided [RDAY07]. The latter concept describes an optical imaging system similar to the ones used for *in vivo* biofluorescence imaging, which are based on bulky CCD sensors with optics in a small chamber, where the subject under investigation is placed. Such system could be based on flexible CISs attached on all sidewalls within the chamber and thus record a panoramic fluorescent activity.

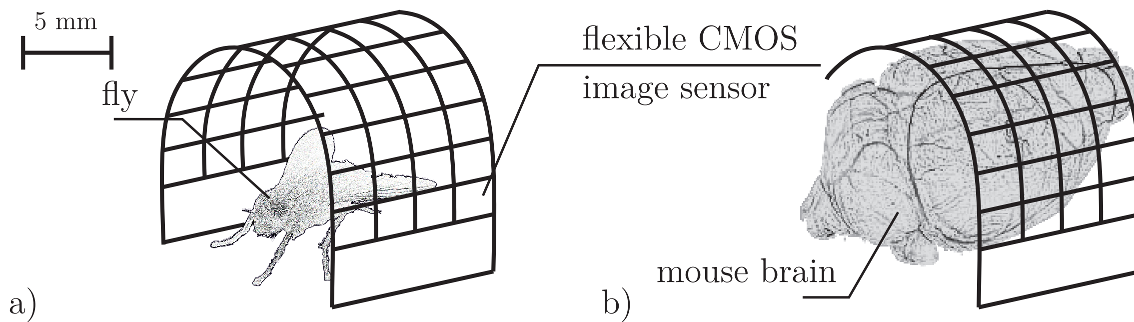


***Figure 7.2: Application concept of the flexible CIS in medical or biological research.*** *a) Wrapped around a fly brain and in combination with fluorescence techniques monitor its brain activity. b) Similarly wrapped around a mouse brain.*

In research studies of compound eyes and insect locomotion, flexible CISs bring several advantages. Together with an additional structure on top of the sensor to provide optical paths over each pixel, a compound eye structure can be emulated and studied. A similar idea based, however, on rigid silicon chips placed on a flexible foil has been presented in [FPCV+13] and the benefits of such an electronic eye are made clear. Apart from studies on insect vision, robotic vision can be enhanced by integrating such a flexible image sensor incorporating a compound eye optical structure atop. Such electronic eyes might not provide a classical image, as a typical user is used to shoot with a camera. Instead they provide a way to gain important data for motion and proximity estimation, which can be utilized for robot path tracking and navigation. Algorithms based on optical flow are reported to be the way insects navigate themselves,

detect obstacles and control their flight characteristics [BKW+11]. Such algorithms can be easily performed directly on-chip. Figure 7.3 illustrates the proposed application concept.

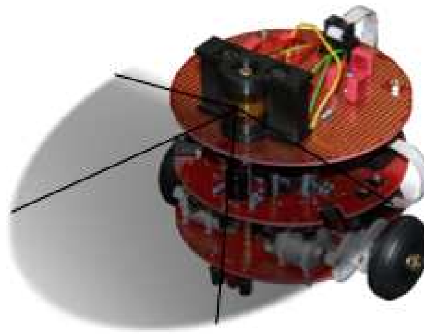

***Figure 7.3: Application concept of the flexible CIS in robotic or insect vision research.*** *A robot with a flexible panoramic image sensor mounted on top. Algorithms based on optical flow and running in the robot controller can provide useful information for motion and proximity estimation.*

Another potential consumer application of curved CISs is optical wireless communication (OWC). Figure 7.4a shows the classical approach of indoor OWC, while figure 7.4b utilizes panoramic optical communications sub-hubs for the local network between the nodes. The classical approach is based on mechanical transceivers with bulky optics, which first search the hub to setup a line-of-sight (LOS) before optically communicating. The proposed approach with the flexible CIS could be advantageous since the mechanical parts can be significantly reduced or even fully eliminated. By introducing a two dimensional detector the receiver efficiency can be enhanced [Oht08], [OFZ+05] and functionalities such as tracking of a mobile transmitting node can be demonstrated.

## 7.3 Synopsis and Further Work

In the last section of this work a brief summary of the achieved results will be listed and future work proposals will be discussed. The presented investigations led to the following knowledge:

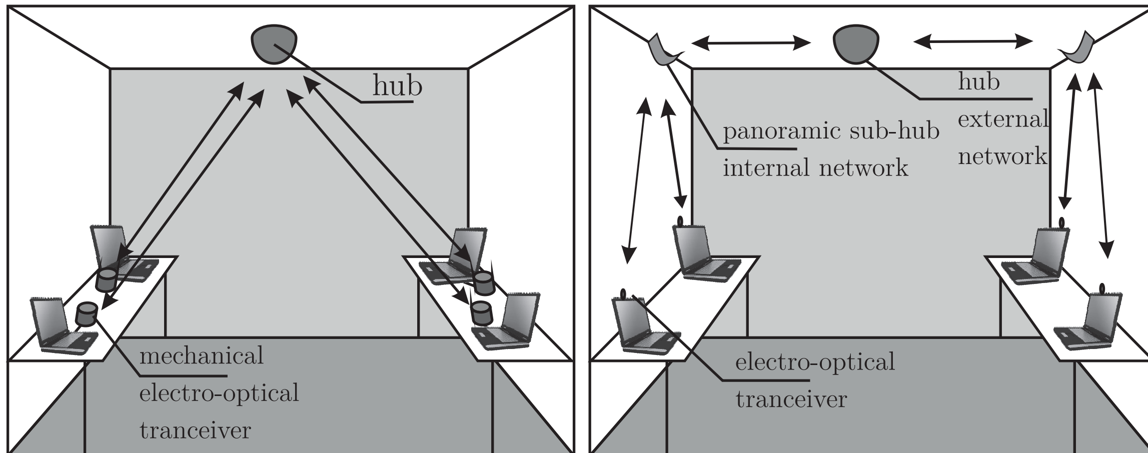


***Figure 7.4: Application concept of the flexible CIS in optical wireless communications.*** *a) Conventional indoor OWC. Adapted from [Oht08]. b) A communication sub-hub with a flexible image sensor mounted at the top, provides a panoramic coverage and internal node communication, while the main hub is used for external communication. The bulky mechanical tranceivers are not needed.*

1. Strain-induced dark current changes in p-n juctions and p-n junction based photodiodes show an exponential dependence on the applied uniaxial mechanical stress. The observed changes under compressive stress configurations are negative, while those observed under tensile stress are positive and of greater magnitude.

2. A model describing the strain-induced dark current changes has been presented and experimentally verified.

3. Optical measurements of p-n junction based photodiodes under mechanical stress have revealed that the optical sensitivity under visible illumination and moderate stress levels is a stress independent quantity.

4. Strain-induced drain current changes of circular gate MOS transistors show a decreased sensitivity to mechanical stress, when compared to the conventional linear gate format transistors. MOS transistors of the employed CMOS process have been characterized under uniaxial mechanical stress.

5. A novel simulation technique for devices under mechanical stress has been introduced, that can be used in standard circuit simulators and allows the simulation of complex analog and digital circuits.

6. A stress independent CMOS image sensor readout circuit chain has been proposed, simulated and experimentally verified.

7. A stress independent CMOS image sensor for flexible applications has been proposed, designed and fabricated.

8. Several guidelines presented in this chapter have been proposed for a stress independent CMOS circuit operation. Optimization and compensation techniques of strain-induced effects in CMOS analog circuits have been proposed and experimentally verified.

The results obtained in this work can be used for future research work on flexible electronics and curved image sensors. The presented application concepts constitute the future work that can be performed based on the obtained results and the fabricated flexible CIS. In particular using the designed flexible sensor a silicone structure can be integrated on top, imitating insect eyes ommatidia. That way investigations on insect and robotic vision and optical wireless communications can be performed. Another investigation domain of future work is strained micro-electro-mechanical systems (MEMS), which utilize the strain-induced effects on device characteristics to perform certain complex operations. As an example of a possible approach let us assume the silicon cantilever in figure 7.5. By applying a DC and AC voltage component on the electrode $V_1 = V_{DC,1} + u_{ac,1}(\sin(\omega_1 t))$, electrostatic forces are exerted on the beam and it can be brought to an oscillating state. In order to achieve a linear response (due to the square law governing the electrostatic force actuation), a differential electrostatic actuator can be used. That way the mechanical stress in the close proximity of the cantilever fixed end shows a sinusoidal characteristic. The MOS transistor integrated in the silicon beam will shift its IV-characteristics (drain current), as experimentally shown in this work, in a sinusoidal manner as well (by changing the channel's mobility). Applying at the transistor gate terminal an input voltage of $V_2 = V_{DC,2} + u_{ac,2}(\sin(\omega_2 t))$ the drain current will be a product of the two applied signals $V_1$ and $V_2$, thus forming a modulator. Assuming a transistor operation in the linear region, a frequency mixer (for modulation-demodulation applications) can be implemented by just a single MEMS structure. Another application that can be investigated with this structure is analog multiplication.

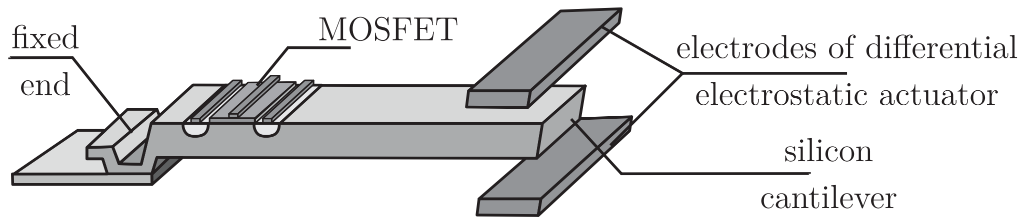


***Figure 7.5: Future work proposal on MEMS.*** *A silicon cantilever oscillates by applying a differential voltage based on $V_1$ at the electrodes. On the gate of the MOSFET the signal $V_2$ is applied. By observing the drain current of the MOS transistor frequency mixing or analog multiplication can be performed.*

# Appendix

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In this appendix definitions about the Voigt notation used for the stress-strain calculation and the stress tensor describing the applied uniaxial [110] mechanical stress throughout this work will be presented in section A.1. Section A.2 will introduce an example on calculating the piezoresistive coefficients of MOS transistors under uniaxial [110] mechanical stress, similarly to the performed experiments. Section A.3 will introduce an example on calculating the piezoresistive coefficients when uniaxial [110] mechanical stress is applied on round gate transistors, similarly to the ones investigated in this work.

## A.1 Stress, Strain and Piezoresistivity Relations in Strained Silicon

The Voigt notation is a way to reduce the order of a symmetric tensor. Let $\bar{\bar{A}}$ be a second order symmetric tensor:

$$\bar{\bar{A}} = \begin{Vmatrix} a_{xx} & a_{xy} & a_{xz} \\ a_{yx} & a_{yy} & a_{yz} \\ a_{zx} & a_{zy} & a_{zz} \end{Vmatrix} = \begin{Vmatrix} a_{xx} & a_{xy} & a_{xz} \\ a_{xy} & a_{yy} & a_{yz} \\ a_{xz} & a_{yz} & a_{zz} \end{Vmatrix} \tag{A.1.1}$$

The Voigt notation is defined as follows, where the superscript $(v)$ denotes that the quantity is given in Voigt notation:

$$\bar{\bar{A}} \rightarrow A^{(v)} = \begin{pmatrix} a_{xx} \\ a_{yy} \\ a_{zz} \\ a_{yz} \\ a_{xz} \\ a_{xy} \end{pmatrix} = \begin{pmatrix} a_1^{(v)} \\ a_2^{(v)} \\ a_3^{(v)} \\ a_4^{(v)} \\ a_5^{(v)} \\ a_6^{(v)} \end{pmatrix} \tag{A.1.2}$$

Equation (A.1.2) makes clear the benefits from such notation, since higher order symmetric tensors can be reduced in lower order tensors. Here a $3 \times 3$ tensor with 9 elements has been reduced to a $1 \times 6$ vector with 6 elements. Similarly, for example, a fourth order symmetric tensor with 81 components (as will come across later in this section) can be reduced using the Voigt notation in a $6 \times 6$ matrix with 36 elements.

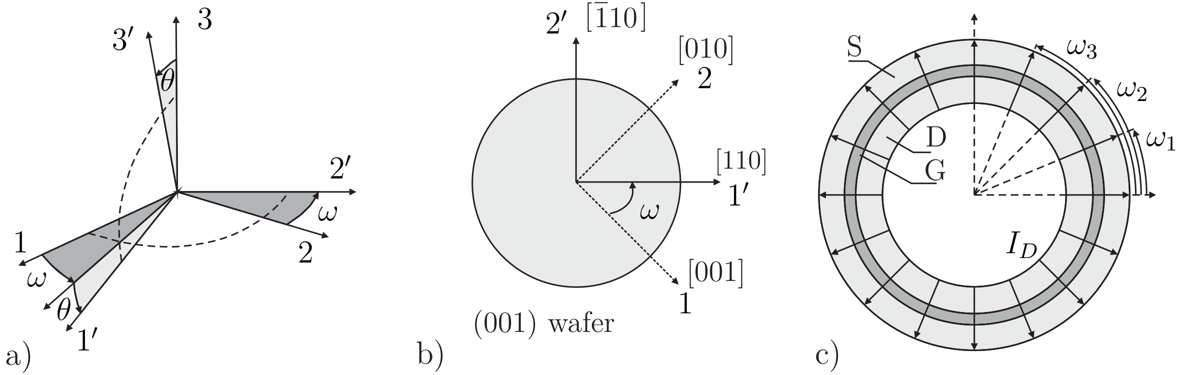


***Figure A.1: Coordinate transformation and round transistors.*** *a) The transformation from coordinate system* 123 *to* $1'2'3'$. *b) Crystallographic directions on a (100) silicon wafer. c) Round transistor decomposed in N elementary transistors in parallel.*

Before elaborating on piezoresistive theory a brief introduction on coordinate transformations will be presented. For a general rotation of a coordinate system 123 to the coordinate system $1'2'3'$ (shown in figure A.1a) the directions cosines $l_i, m_i, n_i$ (with $i \in 1, 2, 3$) are needed to form the rotation matrix. For a rotation $\omega$ only around the

$z$-axis the rotation matrix is given by:

$$\begin{pmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{pmatrix} = \begin{pmatrix} cos\,(\omega) & -sin\,(\omega) & 0 \\ -sin\,(\omega) & cos\,(\omega) & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{A.1.3}$$

If a coordinate transformation is performed, all quantities defined in the initial coordinate system 123 need to be transformed in the new coordinate system $1'2'3'$. Therefore, for transforming second order tensors the transformation matrix $R^{(v)}$ in Voigt notation is defined as follows:

$$R^{(v)} = \begin{pmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & (l_1n_3+l_3n_1) & (m_1n_3+m_3n_1) & (l_1m_3+l_3m_1) \\ l_2l_3 & m_2m_3 & n_2n_3 & (l_2n_3+l_3n_3) & (l_1n_3+m_3n_2) & (l_2m_3+l_3m_2) \\ l_1l_2 & m_1m_2 & n_1n_2 & (l_1n_2+l_2n_1) & (m_1n_2+m_2n_1) & (l_1m_2+l_2m_1) \end{pmatrix} \tag{A.1.4}$$

Recalling the Hooke's Law presented in subsection 2.1.3, can be written for the mechanical stress tensor $\bar{\bar{T}}$, the strain tensor $\bar{\bar{\varepsilon}}$, the elastic compliance tensor $\bar{\bar{C}}$, the elastic stiffness tensor $\bar{\bar{S}}$, the piezoresistivity tensor $\bar{\bar{\Pi}}$ and the tensor $\bar{\bar{P}}$ describing of the changes in resistivity $\rho$ the following:

$$\bar{\bar{T}} = \bar{\bar{C}} \otimes \bar{\bar{\varepsilon}} \tag{A.1.5}$$

$$\bar{\bar{\varepsilon}} = \bar{\bar{S}} \otimes \bar{\bar{T}} \tag{A.1.6}$$

$$\bar{\bar{P}} = \bar{\bar{\Pi}} \otimes \bar{\bar{T}} \tag{A.1.7}$$

where the $\otimes$ denotes a tensor product.

For silicon due to the symmetry of the crystal, the Voigt notation presented above can be utilized, so that the mechanical stress tensor $\bar{\bar{T}}$, the strain tensor $\bar{\bar{\varepsilon}}$, the elastic compliance tensor $\bar{\bar{C}}$, the elastic stiffness tensor $\bar{\bar{S}}$ and the piezoresistivity tensor $\bar{\bar{\Pi}}$ can

be reduced in the following matrices $T^{(v)}$, $\varepsilon^{(v)}$, $C^{(v)}$, $S^{(v)}$ and $\Pi^{(v)}$, respectively:

$$\bar{\bar{\varepsilon}} \rightarrow \varepsilon^{(v)} = \begin{pmatrix} \varepsilon_1^{(v)} \\ \varepsilon_2^{(v)} \\ \varepsilon_3^{(v)} \\ \varepsilon_4^{(v)} \\ \varepsilon_5^{(v)} \\ \varepsilon_6^{(v)} \end{pmatrix} = \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{pmatrix} \tag{A.1.8}$$

$$\bar{\bar{T}} \rightarrow T^{(v)} = \begin{pmatrix} \sigma_1^{(v)} \\ \sigma_2^{(v)} \\ \sigma_3^{(v)} \\ \sigma_4^{(v)} \\ \sigma_5^{(v)} \\ \sigma_6^{(v)} \end{pmatrix} = \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{pmatrix} \tag{A.1.9}$$

$$\bar{\bar{C}} \rightarrow C^{(v)} = \begin{pmatrix} c_{11}^{(v)} & c_{12}^{(v)} & c_{12}^{(v)} & 0 & 0 & 0 \\ c_{12}^{(v)} & c_{11}^{(v)} & c_{12}^{(v)} & 0 & 0 & 0 \\ c_{12}^{(v)} & c_{12}^{(v)} & c_{11}^{(v)} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44}^{(v)} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44}^{(v)} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44}^{(v)} \end{pmatrix} \tag{A.1.10}$$

$$\bar{\bar{S}} \rightarrow S^{(v)} = \begin{pmatrix} s_{11}^{(v)} & s_{12}^{(v)} & s_{12}^{(v)} & 0 & 0 & 0 \\ s_{12}^{(v)} & s_{11}^{(v)} & s_{12}^{(v)} & 0 & 0 & 0 \\ s_{12}^{(v)} & s_{12}^{(v)} & s_{11}^{(v)} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44}^{(v)} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44}^{(v)} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{44}^{(v)} \end{pmatrix} \tag{A.1.11}$$

$$\bar{\bar{\Pi}} \rightarrow \Pi^{(v)} = \begin{pmatrix} \pi_{11}^{(v)} & \pi_{12}^{(v)} & \pi_{13}^{(v)} & 0 & 0 & 0 \\ \pi_{12}^{(v)} & \pi_{11}^{(v)} & \pi_{13}^{(v)} & 0 & 0 & 0 \\ \pi_{13}^{(v)} & \pi_{13}^{(v)} & \pi_{33}^{(v)} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44}^{(v)} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44}^{(v)} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{66}^{(v)} \end{pmatrix} \tag{A.1.12}$$

where $c_{11}^{(v)}$, $c_{12}^{(v)}$, $c_{44}^{(v)}$ the elastic stiffness coefficients of silicon in room temperature and $s_{11}^{(v)}$, $s_{12}^{(v)}$, $s_{44}^{(v)}$ the elastic compliance coefficients of silicon in room temperature, both listed in table A.1. $\pi_{11}^{(v)}$, $\pi_{12}^{(v)}$, $\pi_{44}^{(v)}$ are the piezoresistive coefficients of silicon in the coordinate system of the main crystallographic directions in room temperature and are listed in table A.2.

***Table A.1: Elastic compliance* s *and stiffness* c *coefficients of silicon.*** [YC10]

| $c$ [GN/m$^2$] | | | $s$ $\left[(\mathrm{TN/m^2})^{-1}\right]$ | | |
|---|---|---|---|---|---|
| $c_{11}^{(v)}$ | $c_{12}^{(v)}$ | $c_{44}^{(v)}$ | $s_{11}^{(v)}$ | $s_{12}^{(v)}$ | $s_{44}^{(v)}$ |
| 165.7 | 63.9 | 79.6 | 7.68 | -2.14 | 12.56 |

***Table A.2: Piezoresistive coefficients of silicon in the main crystallographic direction.*** *All values are given in* $[(TPa)^{-1}]$ [Smi54].

| | $\pi_{11}^{(v)}$ | $\pi_{12}^{(v)}$ | $\pi_{44}^{(v)}$ |
|---|---|---|---|
| n-type silicon | $-1022$ | 537 | $-136$ |
| p-type silicon | 66 | $-11$ | 1381 |

Utilizing the definition of the quantities in Voigt notation can be written for the stress-strain relations:

$$T^{(v)} = C^{(v)} \cdot \varepsilon^{(v)} \quad \text{(A.1.13)}$$

$$\varepsilon^{(v)} = S^{(v)} \cdot T^{(v)} \quad \text{(A.1.14)}$$

$$P^{(v)} = \Pi^{(v)} \cdot T^{(v)} \quad \text{(A.1.15)}$$

where the tensor product calculations have been reduced to simple matrix multiplication calculations.

If the mechanical stress tensor $T'^{(v)}$ or the tensor $P'^{(v)}$ describing the resistivity changes $\Delta\rho/\rho$ have to be transformed in a new coordinate system $1'2'3'$, it can be written for the primed quantities in the new coordinate system:

$$T'^{(v)} = R^{(v)} T^{(v)} \quad \text{(A.1.16)}$$

$$\Pi'^{(v)} = R^{(v)} \Pi^{(v)} \left(R^{(v)}\right)^{-1} \quad \text{(A.1.17)}$$

## A.2 Transistors under [110] Uniaxial Mechanical Stress on (100) Silicon

The application of a uniaxial [110] mechanical stress $\sigma$ causes strains along the main axes of the used coordinate system. Following the calculations presented in [STN10] can be shown for $\bar{\bar{\varepsilon}}_{[110]}$:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{s_{11}^{(v)} + s_{12}^{(v)}}{2}\sigma,\ \varepsilon_{xy} = \frac{s_{44}^{(v)}}{2}\sigma,\ \varepsilon_{zz} = s_{12}^{(v)}\sigma \tag{A.2.1}$$

$$\bar{\bar{\varepsilon}}_{[110]} = \begin{Vmatrix} \varepsilon_{xx} & \varepsilon_{xy}/2 & 0 \\ \varepsilon_{xy}/2 & \varepsilon_{xx} & 0 \\ 0 & 0 & \varepsilon_{zz} \end{Vmatrix} \tag{A.2.2}$$

Utilizing equations (A.1.4), (A.1.12) and (A.1.17) can be written for the transformed piezoresistivity matrix in the new coordinate system (recall figure A.1b):

$$\Pi_{[110]}^{\prime(v)} = \begin{pmatrix} \pi_{11}^{\prime(v)} & \pi_{12}^{\prime(v)} & \pi_{13}^{\prime(v)} & 0 & 0 & 0 \\ \pi_{12}^{\prime(v)} & \pi_{11}^{\prime(v)} & \pi_{13}^{\prime(v)} & 0 & 0 & 0 \\ \pi_{13}^{\prime(v)} & \pi_{13}^{\prime(v)} & \pi_{33}^{\prime(v)} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44}^{\prime(v)} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44}^{\prime(v)} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{66}^{\prime(v)} \end{pmatrix} \tag{A.2.3}$$

The mechanical stress tensor $T_{[110]}^{\prime(v)}$ in Voigt notation for the applied uniaxial [110] mechanical stress $\sigma$ in the coordinate system $1'2'3'$ of figure A.1b is given by:

$$T_{[110]}^{\prime(v)} = \begin{pmatrix} \sigma \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{A.2.4}$$

Using equation (A.1.15) can be written for the resistivity changes $\Delta\rho/\rho$ and the corresponding tensor $P'^{(v)}_{[110]}$ in the coordinate system $1'2'3'$:

$$P'^{(v)}_{[110]} = \Pi'^{(v)}_{[110]} T'^{(v)}_{[110]} = \begin{pmatrix} \pi'^{(v)}_{11} \\ \pi'^{(v)}_{12} \\ \pi'^{(v)}_{13} \\ 0 \\ 0 \\ 0 \end{pmatrix} \sigma = \begin{pmatrix} \frac{1}{2}\left(\pi^{(v)}_{11} + \pi^{(v)}_{12} + \pi^{(v)}_{44}\right) \\ \frac{1}{2}\left(\pi^{(v)}_{11} + \pi^{(v)}_{12} - \pi^{(v)}_{44}\right) \\ \pi^{(v)}_{12} \\ 0 \\ 0 \\ 0 \end{pmatrix} \sigma = \begin{pmatrix} \pi_L \\ \pi_T \\ \pi^{(v)}_{12} \\ 0 \\ 0 \\ 0 \end{pmatrix} \sigma \quad \text{(A.2.5)}$$

## A.3 Round Transistors under [110] Uniaxial Mechanical Stress on (100) Silicon

Goal of this section is the theoretical calculation of the strain-induced resistivity change or the strain-induced drain-source current change of a round transistor similar to the one shown in figure A.1c. In order to compute the resistivity in such structure, the transistor will be decomposed in N elementary parallel transistors. The drain-source current of each transistor flows in a different angle $\omega_i$ w.r.t. the [110] direction. The angle $\omega_i$ runs over the entire structure and thus: $0 < \omega_i < 2\pi$. The goal is to compute the resistivity change matrix $P''^{(v)}_{\omega}$ for each elementary transistor. For this reason, we need to perform for each transistor a transformation to a new coordinate system $1''2''3''$, which $1''$-axis will be along the drain-source current direction. This transformation is a rotation of the coordinate system $1'2'3'$ by an angle $\omega$ around the 3-axis. Therefore, using equations (A.1.16) and (A.1.17) can be written for the resistivity change matrix $P''^{(v)}_{\omega}$ in the $1''2''3''$ coordinate system:

$$T''^{(v)}_{\omega} = R^{(v)}_{\omega} T'^{(v)}_{[110]} \quad \text{(A.3.1)}$$

$$\Pi''^{(v)}_{\omega} = R^{(v)}_{\omega} \Pi'^{(v)}_{[110]} \left(R^{(v)}_{\omega}\right)^{-1} \quad \text{(A.3.2)}$$

$$P''^{(v)}_{\omega} = \Pi''^{(v)}_{\omega} T''^{(v)}_{\omega} \quad \text{(A.3.3)}$$

Writing equation (A.3.3) for every elementary transistor and setting $\omega = \omega_i$ with

$\{i \in \mathbb{N} \,|1 < i < N\}$ can be written:

$$P''^{(v)}_{\omega_i} = \Pi''^{(v)}_{\omega_i} T''^{(v)}_{\omega_i} = \begin{pmatrix} \Delta\rho/\rho|''^{(v)}_{\omega_{i,1}} \\ \Delta\rho/\rho|''^{(v)}_{\omega_{i,2}} \\ \Delta\rho/\rho|''^{(v)}_{\omega_{i,3}} \\ \Delta\rho/\rho|''^{(v)}_{\omega_{i,4}} \\ \Delta\rho/\rho|''^{(v)}_{\omega_{i,5}} \\ \Delta\rho/\rho|''^{(v)}_{\omega_{i,6}} \end{pmatrix} \tag{A.3.4}$$

The first element of each computed vector $P''^{(v)}_{\omega_i}$ corresponds to the strain-induced resistivity change along the 1-axis of the transformed coordinate system, along which the drain-source current of the $i$-th elementary transistor flows. Summing up all the elements $\Delta\rho/\rho|''^{(v)}_{\omega_{i,1}}$ $\forall\, i$ and averaging over the number of elementary transistors N, the resistivity change $\left.\frac{\Delta\rho}{\rho}\right|_{\omega_{round}}$ of the round transistor can be obtained:

$$\left.\frac{\Delta\rho}{\rho}\right|_{\omega_{round}} = \frac{1}{N}\sum_{i}^{N} \Delta\rho/\rho|''^{(v)}_{\omega_{i,1}} = \left.\frac{\Delta I_D}{I_D}\right|_{\omega_{round}} \tag{A.3.5}$$

Dividing by the applied uniaxial [110] mechanical stress $\sigma$ the piezoresistive coefficient $\pi_{round}$ can be computed as follows:

$$\pi_{round} = \frac{\left.\frac{\Delta\rho}{\rho}\right|_{\omega_{round}}}{\sigma} = \frac{\pi^{(v)}_{11} + \pi^{(v)}_{12}}{2} \tag{A.3.6}$$

where $\pi^{(v)}_{11}$ and $\pi^{(v)}_{12}$ the piezoresistance coefficients of silicon in the main crystallographic coordinate system.

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