The Influence of Semiconductor Layer Morphology on the Performance of Indium Oxide TFTs

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To my family, for always being near, despite the distance

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Abstract

Scientific literature on solution processable metal oxide TFTs rarely discusses the influence of the semiconductor film morphology on the characteristics of the TFTs. It is sometimes mentioned as a result of the variation of one parameter or another, but never discussed as the independent variable in a given experiment. This is probably due to the multitude and complexity of factors that influence the morphology of an active layer and consequently the performance of the devices.

This work focuses on the deeper understanding of the factors that connect the semiconductor film morphology to the functionality of the fabricated indium oxide TFTs. On the one hand two different precursor systems which yield the same surface properties of the TFT's active layer are compared; on the other hand lies the comparison of two layers resulting from the same precursor material but with different semiconductor morphology.

The semiconductor formulations were prepared by screening several indium sources most often met in literature and additionally a precursor system provided by Evonik Industries AG. The initial tests favored indium nitrate hydrate and the indium precursor from Evonik for further investigations. Next the performance of the semiconductors was adjusted by varying the solvent of the formulations.

While the indium nitrate hydrate based TFTs showed excellent performance in bottom gate - bottom contact configuration, fabricated in air and at a processing temperature of 350°C, (μ_0 = 9.78 cm²/Vs, S = 0.46 V/dec), the precursor supplied by Evonik Industries AG, under the same processing conditions reached the following figures of merit: μ_0 = 15.12 cm²/Vs, S = 0.72 V/dec. In both cases the semiconductor films were uniform and smooth, with a root mean square surface roughness of about 0.5 nm.

A strong dependence of other performance indicators on the morphology of the semiconductor film was observed. For example the sheet resistance of the best performing rough samples was two times larger than that of the smooth active layers, but in most cases smaller than 1 MΩ. The contact resistance of the bottom contacts TFTs with ITO/Au source and drain electrodes was very small for all systems, comparable to reported literature values for sputtered a-IGZO with metal top contacts.

The TFTs fabricated with the semiconductor precursor from Evonik Industries AG showed outstanding stability, compared to other precursors, in either positive or negative bias temperature stress conditions when the films were smooth, and proved less stable when the active layers were rough.

Lastly, Arrhenius plots of ln(μ_0) against 1/T showed little energetic difference among the compared materials, probably caused by contamination with rests from solvents and side groups, as well as ease of ionized oxygen vacancy formation at the exposed surface of the semiconductor facilitated by surface defects.

Kurzfassung

In der wissenschaftlichen Literatur über lösungsprozessierbare, metalloxidische Dünnschichttransistoren (TFT) wird selten der Einfluss der Morphologie der Halbleiterschicht auf die Eigenschaften des TFTs diskutiert. Die Schichtmorphologie wird manchmal als Ergebnis der Variation des einen oder anderen Parameters erwähnt, aber nie als eine unabhängige Variable. Ein möglicher Grund ist die Vielfalt und die Komplexität der Faktoren, die die Schichtmorphologie sowie die Performance eines TFTs beeinflussen.

Ziel dieser Arbeit war ein tieferes Verständnis über den Zusammenhang zwischen Schichtmorphologie und Funktionalität eines Indiumoxid-basierten TFTs. Dafür wurden Proben, die aus verschiedenen indiumhaltigen Prekursoren hergestellt wurden und eine vergleichbare Schichtmorphologie hatten, verglichen. Außerdem wurden Proben aus demselben Prekursor aber mit verschiedenen Schichtrauigkeiten untersucht.

Als Basis für die verwendeten Halbleiterformulierungen dienten in der Literatur oft zitierte Indiumquellen, sowie ein Prekursorsystem von der Evonik Industries AG. Die ersten Versuche mit Indium-nitrat Hydrat und dem Evonik Prekursor zeigten die besten Ergebnisse. Deshalb wurden die auf diesen Materialien basierenden Lösungen optimiert indem das Lösemittel der Formulierungen variiert wurde.

Die Transistoren wurden in der „bottom gate – bottom contact“ Konfiguration an Luft bei einer Temperatur von 350°C hergestellt. Die auf Indium-nitrat Hydrat basierten TFTs zeigten eine Mobilität von μ_0 = 9,78 cm²/Vs und eine Steigung der Transferkennlinie unterhalb der Einsatzspannung von S = 0,46 V/dec. Die auf dem Evonik Prekursor basierenden TFTs hatten eine höhere Mobilität von μ_0 = 15,12 cm²/Vs, jedoch eine größere Steigung S = 0,72 V/dec. Die Schichtrauigkeit beider Proben war 0,5 nm.

Außerdem wurde eine starke Abhängigkeit anderer Parameter von der Morphologie der Halbleiterschicht beobachtet. Zum Beispiel war der Schichtwiderstand der Transistoren mit einer rauen Halbleiterschicht doppelt so hoch wie der Schichtwiderstand der Proben mit einer glatten Halbleiteroberfläche, in allen Fällen aber unter 1 MΩ. Der Kontaktwiderstand aller Proben mit ITO/Au Kontakten in der „bottom contact“ Konfiguration war klein und vergleichbar mit Literaturwerten.

Negative und positive Gatespannungsstressmessungen bei erhöhter Temperatur ergaben folgende Ergebnisse: Glatte Schichten zeigen eine geringere Verschiebung der Einsatzspannung als Proben mit rauer Oberfläche. Bei gleicher Morphologie erweisen sich Schichten die aus dem Evonik Prekursor hergestellt wurden als stabiler.

Die Arrhenius Plots von $\ln(\mu_0)$ gegen $1/T$ zeigten einen kleinen Unterschied zwischen den mit verschiedenen Indium Prekursoren hergestellten TFTs. Der Unterschied ist vermutlich auf Kohlenstoffkontaminationen aus den Lösemitteln und nicht vollständig umgesetztes Material zurückzuführen. Ein weiterer Grund könnte die Ausbildung von Sauerstofffehlstellen an der Halbleiteroberfläche sein.

1 Introduction

The combination of two completely unrelated discoveries in the 1960's [1]: the liquid crystals discovered by Friedrich Richard Reinitzer in 1888 [2] and the thin-film transistor invented by Bardeen and Brattain in late 1947 (although the ideas leading to the invention of the TFT were much older) [1] has enabled a new class of display technology which replaced the traditional *cathode ray tubes* (CRTs) in most applications in less than 40 years from its invention [3]. This was the *liquid crystal display* (LCD), which started receiving an enormous amount of attention after the paper of Lechner *et al.* published in 1971, in which they explained various possibilities to overcome the cross talk problem inherent to early LCDs [4].

Over the years the existing technologies have improved continuously and new ones have been introduced to complement the older ones or replace their shortcomings [1], [5]. Thus in addition to LCDs, the area of *flat panel displays* (FPDs) has branched into *plasma displays* (PDs), *light emitting diode* (LED) displays, *organic light emitting diode* (OLED) displays and *field emission displays* (FEDs) [5]. All these technologies have their unique advantages and areas of application.

For example the active matrix OLED displays are rapidly attracting interest because of several advantages they have over conventional LCDs, such as a wider and more saturated color gamut, lower power consumption, a wider viewing angle, higher contrast and fast response times [6]. These properties make OLED technology also attractive for the area of flexible displays which avoid the rigidity and brittleness of glass substrates and offer a larger freedom of design [7].

Such FPDs are driven by TFT back planes [5] which to date are based on traditional amorphous or (low temperature) polycrystalline silicon technology [7], [8], [9]. Amorphous silicon (a-Si) which is used as active material in the TFTs driving active matrix LCDs achieves charge carrier mobility values less than 1 cm^2/Vs [8], [10], and suffers from severe instability

against electrical and optical stressing [11]. The polycrystalline silicon can achieve mobility values well above 50 cm^2/Vs [8], does not suffer from the electrical instability of a-Si [10], but requires higher manufacturing temperatures, is more expensive than a-Si to produce, its grain boundaries present charge trapping and scattering centers and due to its random crystal orientation has a poor areal uniformity which makes it inapplicable to large area devices [7]- [11].

In 2004, Nomura *et al.* published a paper in which they presented a new class of semiconducting material, a transparent and amorphous metal oxide (indium-gallium-zinc-oxide – a-IGZO) with a charge carrier mobility above 8 cm^2/Vs, when sputtered even at room temperature [12]. This performance was already well above the estimated necessary mobility of 3 cm^2/Vs for driving an ultrahigh definition AMOLED TV at 120 Hz frame rate [13]. In the years to follow a great deal of research was performed on this class of materials, and various other combinations of suitable cations (see Table 2 and Table 3 in Chapter 3.1).

The origin of the high performance of the metal oxides was postulated back in 1996 [14] as being a result of the high overlap between the empty metal cation orbitals which formed an extended conduction band even in a disordered, amorphous state. That is why several material systems composed of cations from the specified region of the periodic table were found to achieve a satisfying performance (Table 2), although the main focus of sputtered materials remained the a-IGZO system. The characteristic high mobility of this material class, its transparency and large area uniformity due to the amorphous state made it appear very attractive for device applications and soon most of the research focused on its electrical and optical stability [15], [16].

While sputtered amorphous metal oxide semiconductors show an incredible potential at this time, the application of vacuum processes to large substrates is costly [17]. That is why many scientific groups have diverted their efforts to the development of solution processable metal oxides which would offer numerous advantages compared to vacuum techniques: low cost production, high throughput, simplicity of equipment [18], [19]. At the moment most solution processable metal oxides require high annealing temperatures to convert the precursor materials into the metal oxide films and much research is aimed at lowering this temperature in order to make the processes compatible with plastic substrates

for flexible electronics [20], [21]. Electric stability is also an important issue often addressed in scientific literature [22].

What makes the development of a solution processable metal oxide formulation so interesting and at the same time challenging is the enormous variety of precursor materials and solvents with compatibility issues, different solubility, reactivity and optical properties. The performance of the TFTs fabricated with metal oxide formulation no longer depends only on the chemical composition of the material, but also on the density of the film, its contamination with solvent and anion residues, on the volatility of these residues which will eventually determine the temperature which needs to be supplied to the semiconductor film to bring it to the required quality. The quality of the active layer is crucial for an adequate performance of a TFT fabricated via a solution process, and is also influenced by the film morphology, which was the subject of research in the present thesis.

Due to the myriad of options for multi-cation systems possible for the reasons stated above, a detailed investigation of a single-cation system was deemed more feasible. Zinc oxide is a very popular metal oxide widely discussed in literature; gallium oxide alone is normally an insulator and is used in small amounts to control the charge concentration in mixed oxides [17], therefore the research in this work has been concentrated on indium oxide as a model system, which also appears often in literature, but usually as a comparison system. The research that followed was grouped in this thesis as follows:

Chapter 2 covers the basics of charge transport, TFT architecture and operation. It deals with the derivation of the gradual channel approximation method used to characterize the charge transport in TFTs and introduces several models for the extraction of the figures of merit. Among them is the gate-voltage-dependent mobility model which was applied to extract the charge carrier mobility, threshold voltage and disorder (gate voltage dependence) parameter. Methods to calculate the subthreshold slope and areal density of states used in this work are also introduced.

Chapter 3 summarizes the current trends in metal oxide semiconductors research and illustrates the main points of interest.

Chapter 4 elaborates on the methods applied to fabricate and characterize the investigated thin-film transistors.

The bulk of the results are presented in Chapter 5. The chapter is divided in three parts. In the first part the reader will find a detailed account of the selection process of the material systems. The second half will describe in detail the properties of the TFTs fabricated with indium nitrate hydrate in methoxyisopropanol formulations and the influence of the morphology of the deposited semiconductor film on device performance. Finally, the last third of the chapter will compare the performance described before with that of TFTs fabricated with solutions of an indium oxoalkoxide provided by Evonik Industries AG.

Chapter 6 will discuss the implications of the observed behavior of the figures of merit with respect to the material system and the dependent on it film morphology.

Chapter 7 will be a summary of the presented work with mentions of potential research to further understand the investigated materials.

2

Theoretical background

2.1. TFT architecture and operation

2.1.1. Principles of TFT operation

The characteristic building block of a *Thin Film Transistor* (TFT) is a *Metal-Insulator-Semiconductor* (MIS) structure. The voltage applied at the metal side is used to control the charge concentration at the semiconductor-insulator interface [23]. In the case of an n-type semiconductor, if a small negative voltage is applied at the metal side, the bands of the semiconductor bend upwards, causing the negative charge to move away from the semiconductor-insulator interface, depleting the interface (Figure 1.a). Therefore this regime is called *depletion*.

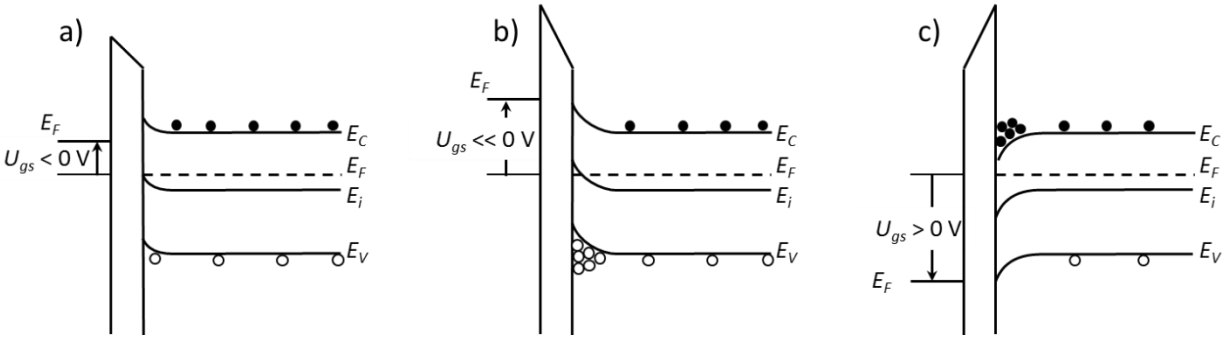

Figure 1. Band diagrams of a MIS-structure in a) depletion, b) inversion and c) accumulation modes. Adapted from [23].

If the voltage at the metal side is lowered further, it will lead eventually to the situation when the intrinsic energy level of the semiconductor will cross the Fermi energy and will lead to an accumulation of holes at the interface. This situation is called *inversion* (Figure 1.b). And lastly, if the voltage on the metal side is made positive, the bands of the semiconductor will bend downwards, accumulating negative charge at the interface and opening a conductive channel. This regime is called *accumulation* (Figure 1.c). The

accumulated negative charge at the interface can be used to conduct a current between metallic electrodes placed on the side of the semiconductor.

The electrodes that are taking advantage of the charge accumulated at the semiconductor-insulator interface are called *source* and *drain electrodes*. The source is normally grounded and serves as a reference potential. The current through the TFT is modulated via the potential applied at the drain electrode. For an n-type conductive channel, applying a positive potential at the drain electrode, will cause the electrons to move from the source electrode (hence the name) to the drain electrode. The current will flow in the opposite direction, respectively, and will be called drain current. The metal electrode of the MIS structure is called *gate electrode*.

When the voltage applied at the gate electrode reaches the value at which the accumulated charge at the semiconductor-insulator interface forms the conductive channel, the TFT is turned on. By applying a small drain-source potential one conducts a drain current which, in an ideal TFT, depends linearly on the drain-source potential and this operation mode is known as the *linear regime*. In the case of a TFT operating in inversion mode, the drain electrode is positively biased and it forms a depletion region around itself (Figure 2.a). As the drain voltage increases, so does the depletion region. This depletion region squeezes the conductive channel to the point when the conductive channel is completely pinched off at the drain electrode. This happens when the drain voltage equals the gate voltage above the turn on voltage of the TFT (Figure 2.b). As the drain voltage is further increased, the depletion region around the drain electrode keeps increasing and starts pushing the pinch-off point towards the source electrode, causing a shortening of the effective channel (Figure 2.c). The increasing resistance of the channel caused by this phenomenon, counteracted by the physical shortening of the channel, causes the drain current to lose its dependence on the drain voltage and its value is controlled only by the amount of charge induced in the channel, e.g. by the applied gate voltage. This regime of operation is called the *saturation regime* [23].

From a phenomenological point of view, accumulation mode operation is equivalent to inversion mode, in the sense that a negatively charged conductive channel forms at the semiconductor-insulator interface. Close to the drain contact the amount of accumulated charge depends on the applied voltage. As the voltage increases, the amount of

accumulated charge decreases. When the potential applied to the drain contact is large enough so that no more charge can be accumulated in its vicinity and the conductive channel becomes pinched off. This value of the drain-source voltage corresponds to the onset of the saturation regime.

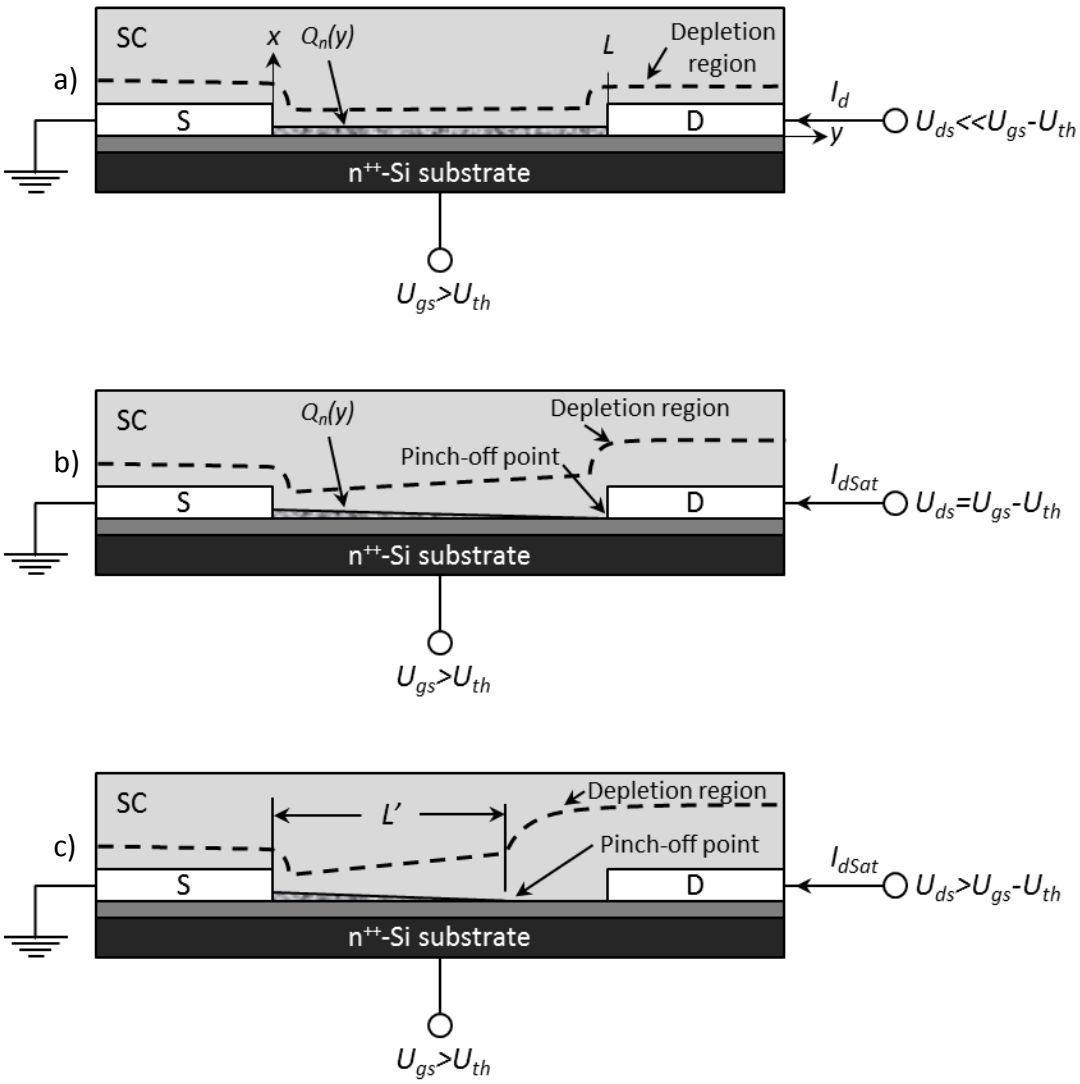

Figure 2. Illustration of the transition of the operating mode of a TFT from the linear into the saturation regime. Adapted from [23].

2.1.2. TFT operation modes

Depending on the charge carrier concentration in the semiconductor material, a TFT might operate in either enhancement mode or in depletion mode [23]. In enhancement mode the concentration of charge carriers in the conductive channel is low, the TFT is normally off at zero gate bias, and one needs to apply a higher positive gate voltage in order to turn the TFT on. The TFT is said to operate in depletion mode if the concentration of charge carriers in the channel is so high, that the TFT is on when no gate bias is applied. In

this case one needs to apply a negative gate voltage in order to switch the TFT off. Figure 3 summarizes the two TFT operation modes.

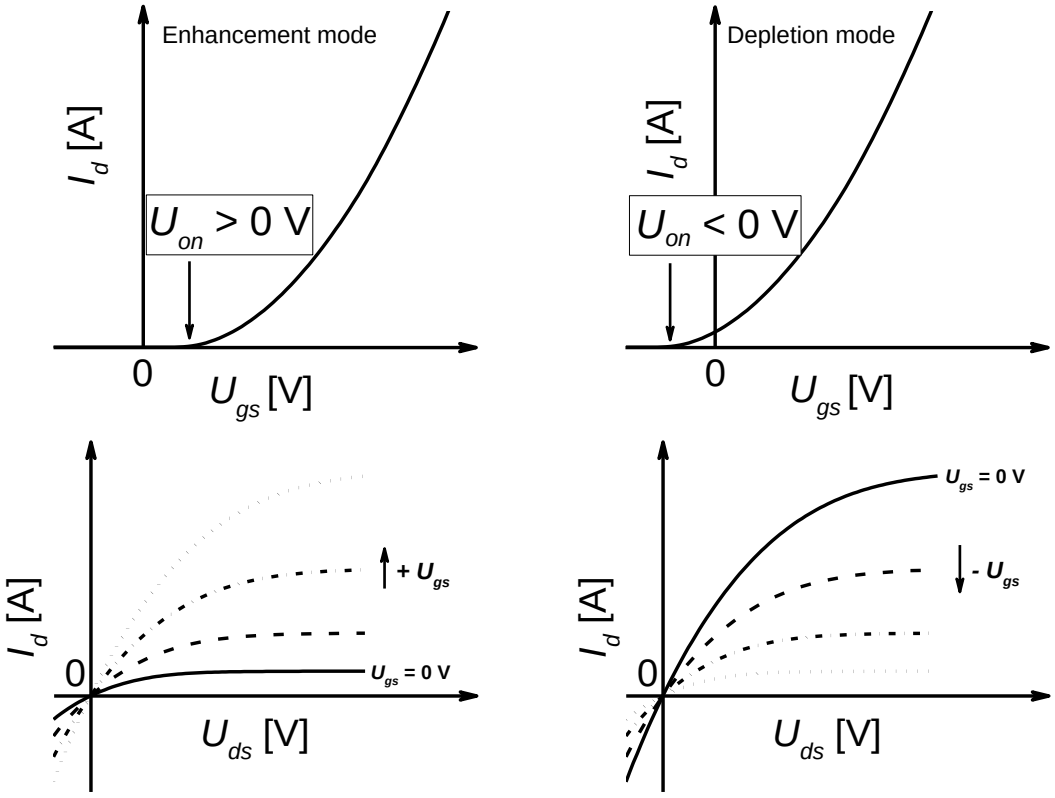

Figure 3. TFT operation modes: Enhancement mode on the left (positive onset, positive gate bias needs to be applied to turn the device on); Depletion mode on the right (negative onset, negative gate bias needs to be applied to turn the device off). Reproduced from [23]**.**

2.1.3. TFT architecture

The architecture of the TFTs can be classified into 4 main categories, depending on the position of the individual layers with respect to the carrier substrate [8], [24]. These are bottom gate – bottom contact, bottom gate – top contact, top gate – bottom contact and top gate – top contact (Figure 4). Depending on the position of the gate and source drain contacts with respect to the semiconductor film, the TFTs can be either coplanar, if the gate and source/drain electrodes are on the same side of the semiconductor, or staggered, if the source/drain contacts and the gate are on opposite sides of the semiconductor layer.

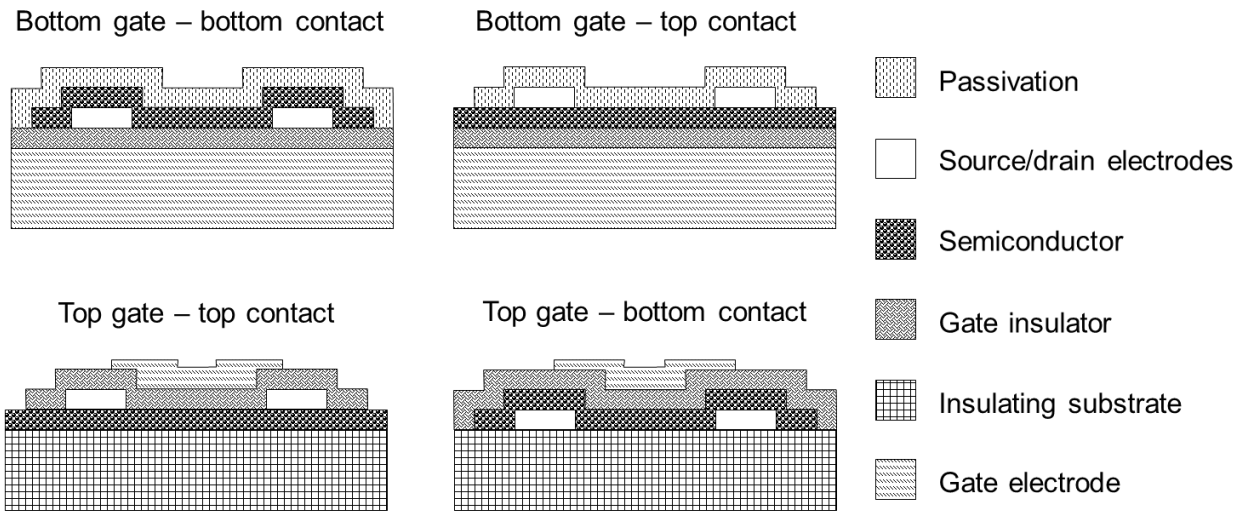

Figure 4. TFT architecture classified according to the position of the source/drain and gate electrodes relative to the substrate of the TFT.

Each of these configurations has its advantages and disadvantages. The bottom gate configuration is generally easier to construct. The semiconductor layer however remains open to the ambient atmosphere and is susceptible to the negative influence of atmospheric factors. That is why this configuration usually needs an additional passivation layer to protect the active channel. In the coplanar bottom gate configuration there's always the risk of increased contact resistance due to a less than optimal quality of the semiconductor-electrode interface, and the parasitic capacitances between the gate and source/drain electrodes, which slow down the TFT, are large in the case of a non-structured gate. The staggered bottom gate configuration has the advantage of an improved quality of the interface between the contacts and the semiconductor, e.g. improved charge injection. Depending on the patterning method used for the source/drain electrodes, the semiconductor might be sensitive to the chemicals used in the process. Often an additional etch-stopper layer is required to protect the active channel [8].

The top gate configurations have the advantage that the gate insulator layer has to be deposited on top of the semiconductor and acts as a passivizing layer. In the staggered configuration it will also protect the channel from harmful chemicals used in subsequent processing, but the risk of poor semiconductor-electrodes interface quality remains.

Lastly, in the top gate – top contact configuration an etch-stopper layer might be needed to protect the semiconductor, depending on the electrodes' deposition technique, but other than that, it combines the positive aspects of all the other configurations: the improved source/drain electrodes to semiconductor interface of a top contact architecture, the

passivation function of the gate insulator and the decreased parasitic capacitance due to gate structuring from a top gate configuration.

2.2. Device parameter extraction

2.2.1. Derivation of a comprehensive conduction model

Understanding the transport phenomena occurring in a semiconductor involves developing a suitable model which describes accurately enough the behavior of the device under investigation. The model that is most widely accepted and used in the scientific community nowadays is the *Gradual Channel Approximation Model* [23], [25], also known as the *Standard Model*. This model looks at the current transport in two dimensions, considering that there is no transport happening parallel to the fingers of the transistor. If the direction parallel to the semiconductor-insulator interface is *y* and the direction perpendicular to it is *x*, then if a potential U_{gs} is applied to the gate electrode of the TFT (Figure 2), the induced negative charge at the semiconductor-insulator interface (Q_n) will form a conductive channel. It is further assumed that the conductive channel is confined at the interface and its spread in the *x*-direction is negligible. The distribution of the electrons in the channel will then be a function of the *U(y)* potential along the *y*-axis, in addition to U_{gs} [26]:

$$Q_n(y) = -C_i\left(U_{gs} - U_{th} - U(y)\right) \tag{1}$$

where C_i is the capacitance per unit area of the gate insulator. In equation (1) appears another potential, U_{th}, which is the value of the gate voltage at which the TFT turns on and is called the *Threshold Voltage*. Its meaning will be discussed in detail later.

The current at any point along the *y*-axis is then given by:

$$I_d(y) = W\left|Q_n(y)\right|v(y) \tag{2}$$

Equation (2) takes into account the contribution of the entire length of the TFT's electrodes (*W*) and introduces the drift velocity of the charge carriers, *v(y).* Assuming a constant mobility of the electrons, one can express *v(y)* in terms of the mobility (μ_n) and the electric field (*E(y)*) along the channel:

$$v(y) = -E(y)\mu_n \tag{3}$$

Replacing *v(y)* from (3) in (2) and integrating (2) from source to drain, e.g. from 0 to *L* (*L* being the TFT's channel length), results in the expression of the drain current along the channel [27]:

$$I_d = \frac{W}{L}\mu_n \int_0^L |Q_n(y)|E(y)dy \tag{4}$$

Since the electric field equals the first derivative of the potential along the channel, equation (4) becomes:

$$I_d = \frac{W}{L}\mu_n \int_0^{U_{ds}} |Q_n(U)|dU \tag{5}$$

With the expression of the induced charge ($Q_n(y)$) from equation (1), solving the integral from (5) results in the following expression for the drain-source current:

$$I_d = \frac{W}{L}C_i\mu_n\left[(U_{gs} - U_{th}) - \frac{U_{ds}}{2}\right]U_{ds} \tag{6}$$

where I_d is the drain-source current, W and L are the TFT's channel width and length respectively, C_i is the gate insulator's capacitance per unit area, U_{gs}, U_{th} and U_{ds} are the gate-source, threshold and drain-source voltages respectively.

As long as the U_{gs}-U_{th} term is much larger than U_{ds}, the TFT is known to operate in the linear regime, e.g. the dependence of the current is linear in the TFT's on-state and can be expressed via:

$$I_d = \frac{W}{L}C_i\mu_n(U_{gs} - U_{th})U_{ds} \tag{7}$$

As U_{ds} increases to the point where U_{gs}-U_{th}= U_{ds}, the channel becomes "pinched-off". The TFT enters the saturation regime of operation in which the current flowing between drain and source is independent of the applied drain-source potential and does not increase anymore if U_{ds} is increased further. In this regime the operation of the TFT is described by the following equation:

$$I_d = \frac{W}{2L}C_i\mu_n(U_{gs} - U_{th})^2 \tag{8}$$

In the derivation of the expression for the standard model, the following assumptions were made [23]:

- The gate capacitor is ideal, free of interface traps and mobile ions
- The diffusion of charge in the channel is small compared to the charge drift, and therefore is ignored
- The doping inside the cannel is uniform
- The leakage current is negligible
- The mobility of the charge carriers is constant
- The electric field over the gate insulator is much larger than the electric field between the source and drain electrodes.

Some of these assumptions may not be applicable to each type of TFTs, therefore in some cases different corrections to the parameters in equation (6) are necessary to account for observed effects. These often involve corrections to the channel length and width to account for short channel effects and parasitic resistances, to the charge carrier mobility which is often dependent on the geometry of the TFT and operating conditions.

2.2.2. Charge carrier mobility

The most often used method to extract the charge carrier mobility out of the measured data is based on the standard model due to historical reasons [23], [25]. Anyone working with a new semiconductor material and wanting to compare the performance of the said material with that of the Silicon TFTs may want to use this well established method to extract the charge carrier mobility. By applying a small and constant U_{ds} for the linear regime one measures the drain-source current as a function of the applied gate bias U_{gs}. Plotting this dependence and taking the first derivative of the resulting curve, e.g. dI_d/dU_{gs}, should give access to the slope of *I-V* curve out of which one calculates the mobility at maximum transconductance via [28]:

$$\mu_n = \frac{dI_d}{dU_{gs}} \left(\frac{W}{L} C_i U_{ds} \right)^{-1} \tag{9}$$

In the saturation regime one should apply a U_{ds} larger than the maximum U_{gs} of the measurement range to ensure that the TFT operates in saturation. Since the current depends quadratically on the applied gate bias, one needs to plot the square root of the measured current against the gate bias and take the first derivative of the resulting curve. The square of the slope of that curve calculated in this way allows extracting the charge carrier mobility via the following equation:

$$\mu_n = \left(\frac{d\sqrt{I_d}}{dU_{gs}} \right)^2 \left(\frac{W}{2L} C_i \right)^{-1} \tag{10}$$

Figure 5 shows an example of a transfer curve measured in linear regime with U_{ds} = 2 V, together with the calculated charge carrier mobility according to equation (9), which reaches a maximum value of 22.55 cm²/Vs at the maximum applied gate voltage.

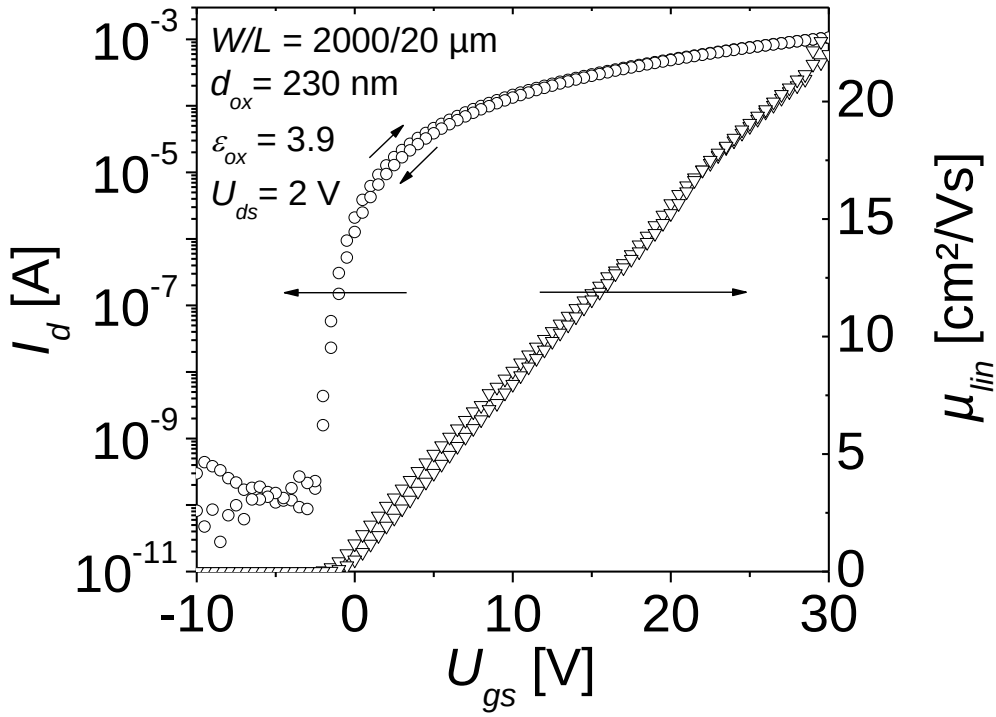

Figure 5. Transfer curve measured in the linear regime and calculated charge carrier mobility using the standard model.

What one can immediately discern in Figure 5 is that for this particular TFT the assumption that the mobility is constant does not hold. This is generally true for disordered, non-crystalline systems. In such systems the transport of carriers can be influenced by the film morphology, which will introduce potential wells in the form of defects [29] or energetic barriers, in the form of grain boundaries [30]. An *I-V* measurement alone does not provide enough information to distinguish between the two. However, according to Street *et al*. a so called Levinson plot, in which one plots the $\ln(I_d/U_{gs})$ against the inverse of the gate bias ($1/U_{gs}$), can provide the necessary evidence of a barrier dominated transport if the resulting plot is linear. A positive onset (for a p-type semiconductor, and respectively a negative onset for an n-type semiconductor) is another hint towards a grainy morphology [30], in which the grain boundaries are thought of as energetic barriers.

If a system disorder is dominated by traps, the conduction through this material may be described by the so called Poole-Frenkel model [23], [31], [32]. This model states that the conduction is dependent on the magnitude of the longitudinal electric field E_L, created by the potential drop between the source and drain electrodes. In this case the charge carrier mobility is described by the following equation:

$$\mu_n = \mu_0 \exp\left[\frac{-q\left(\phi_B - \sqrt{qE_L/\pi\varepsilon}\right)}{k_B T}\right] \tag{11}$$

where q is the elementary charge (1.602×10^{-19} C), ϕ_B is the trap depth, ε is the permittivity of the semiconductor, T is the absolute temperature and k_B is the Boltzmann constant (1.38×10^{-23} J/K). This type of conduction manifests itself in strong nonlinearity of the current in the linear region of the output curves, an effect also known as the current crowding [33], which gives the output curve a characteristic s-shape.

At low longitudinal fields, this model allows to determine the depth of the traps by studying the behavior of the charge carrier mobility with temperature. In this case equation (11) becomes:

$$\mu_n = \mu_0 \alpha \exp\left[-\frac{\Delta E_a}{k_B T}\right] \tag{12}$$

with ΔE_a being the activation energy of the trapped charges, and α the ratio between the free and trapped charges [31]. By plotting the $\ln(\mu_n)$ against the inverse absolute temperature (Arrhenius plot) one can extract the activation energy from the slope of the linear region of the graph.

Since the ratio of the free to trapped charges depends on the perpendicular electric field, e.g. on the applied gate bias, one could expect that the mobility will exhibit a gate voltage dependence as well. This dependence was described by Vissenberg and Matters [34], for organic semiconductors, assuming an exponential distribution of band-tail states, in the following way:

$$\mu_n = \mu_0(T) U_{gs}^{2\left(\frac{T_0}{T}-1\right)} \tag{13}$$

where T_0 is a parameter that describes the distribution of the tail states.

A generalization of this model applied by many authors [25], [31], [32], [33], [35], [36], [37] to different systems states that:

$$\mu_n = \mu_0(T)(U_{gs} - U_{th})^{\gamma} \tag{14}$$

In this equation the parameter γ is known as *the disorder parameter* and describes the energetic disorder within the system. Stallinga *et al.* described this parameter as an indicator of the amount of free charge relative to the trapped charge within the active layer of the TFT [31]. In this form however, the model makes it rather difficult to compare different devices, since γ depends strongly on the semiconductor material, semiconductor-insulator interface, as well as on the fabrication conditions [33]. This means that the extracted charge carrier mobility will have units of $V^{-\gamma}$, which will differ from device to device. In order to circumvent this problem, one can add to equation (14) an additional parameter U_{aa}, as did for example Necliudov and co-workers [38], in order to remove the *"units"* issue.

$$\mu_n = \mu_0(T)\left(\frac{U_{gs} - U_{th}}{U_{aa}}\right)^{\gamma} \tag{15}$$

This gives the extracted mobility values the same units, but because U_{aa} is used as a fit parameter, the mobility values become arbitrary, meaning that the comparison of different devices is again not possible. Some authors set U_{aa} to 1 V, but this results in erroneously small mobility values. Fung *et al.* describe U_{aa} as a material dependent critical voltage [33]. What U_{aa} actually does, is it describes the measurement range, e.g. the gate-source voltage "distance" from the threshold voltage at which the average mobility value will reach the gate voltage independent prefactor μ_0. Replacing μ_n in equation (7) with the expression in (15), and taking the derivative of the current with respect to U_{gs}, the expression of the transconductance becomes:

$$\frac{dI_d}{dU_{gs}} = \frac{W}{L} C_i U_{ds} \mu_0(T)(\gamma+1)\left(\frac{U_{gs} - U_{th}}{U_{aa}}\right)^{\gamma} \tag{16}$$

Equation (16) shows that the mobility calculated with the standard model will be (γ+1) times larger than the U_{gs} dependent mobility. In order to be able to compare the mobility values extracted with this model with the values resulting from the standard model, one should set the value of U_{aa} equal to $(\gamma+1)^{1/\gamma}$ times ($U_{gs\text{-}max}$-U_{th}), which means that for γ values close to 1, this scaling factor is conveniently equal to 2.

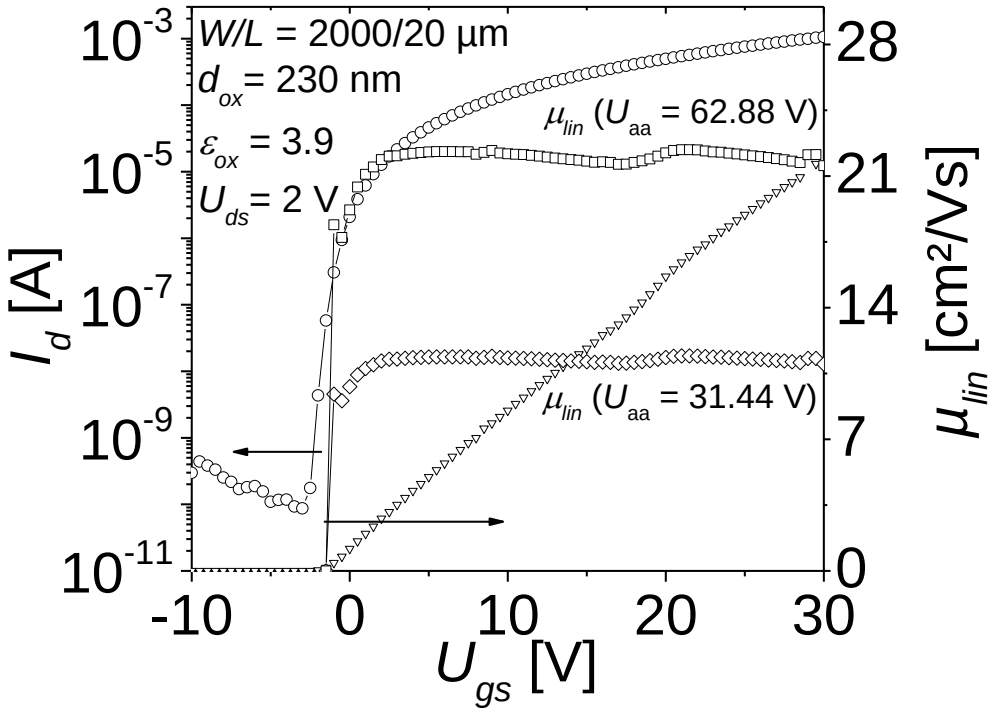

Figure 6. Measured *I-V* curve, calculated mobility with the standard model and with the gate-voltage-dependent mobility model for 2 values of the U_{aa} parameter.

Figure 6 illustrates the comparison of the 2 models based on the data from Figure 5. The *I-V* curve is plotted using circles and the triangles represent the mobility values calculated with the standard model in linear regime (U_{ds} = 2 V). The mobility values extracted using the gate-voltage-dependent mobility model were calculated using the following values for the U_{th}, γ and U_{aa}: U_{th} = -1.44 V, γ = 0.97 and U_{aa} = 31.44 V (diamonds) and U_{aa} = 62.88 V (squares) and were 11.15 cm²/Vs and 21.11 cm²/Vs respectively.

In addition to providing comparable mobility values, the gate-voltage-dependent mobility model results in a much better fit of the transfer curve than the standard model in the linear regime, evident from Figure 7, in which both models are compared. It also allows the systematic extraction of another important parameter in the characterization of TFTs, namely the threshold voltage. One could argue that since both the γ parameter and the U_{th} are fit parameters in the gate-voltage-dependent mobility model, the values of the threshold voltage are strongly influenced by the magnitude of γ, which makes them unrealistic.

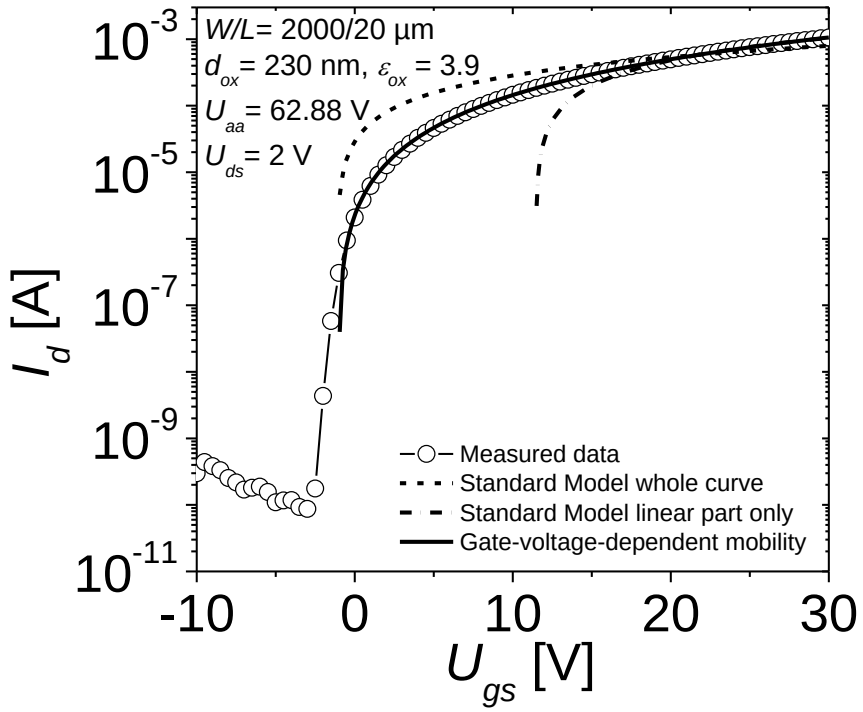

Figure 7. *I-V* curve fitted with the standard model (whole curve and linear part only) and with the gate-voltage-dependent mobility model.

The following section will focus on the comparison of various U_{th} extraction methods accepted by the scientific community with the gate-voltage-dependent mobility model and will discuss the viability of the presented method to extract the threshold voltage.

2.2.3. Threshold voltage

The motivation to look deeper into the topic of threshold voltage extraction methods stems from the comparison of the gate-voltage-dependent mobility model result with the value obtained by using one of the most widely applied methods to obtain U_{th}, namely extrapolating the *I-V* curve in the linear regime to the point where $y = 0$ and reading out the value of U_{th} [37], [39], [40]. A linear and log-plot of the same *I-V* data set are presented in Figure 8 for comparison. The log plot was fitted with the gate-voltage-dependent mobility model, resulting in a U_{th} = -1.44 V, while the linear plot was subjected to the extrapolation method mentioned above, resulting in a U_{th} = 12.45 V. A large discrepancy in the obtained U_{th} values immediately poses the question: which method was erroneously applied?

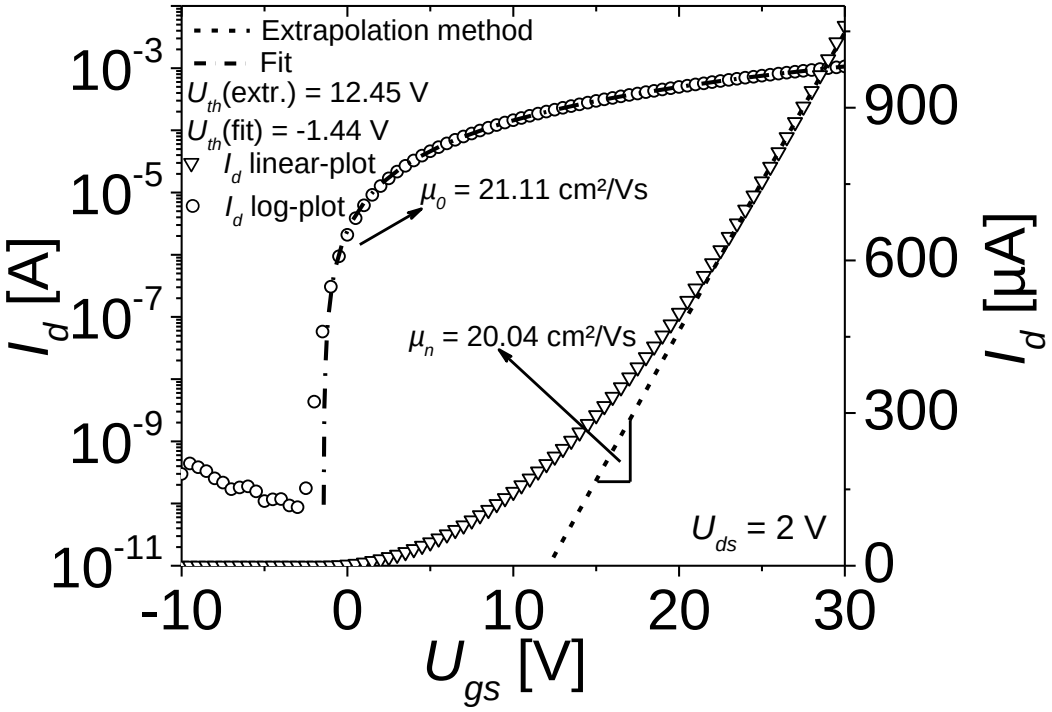

Figure 8. Linear and log plot of measured *I-V* data. Extracted threshold voltage via fitting and by extrapolating the *I-V* curve in the linear region.

In order to decide which method returns more realistic values, the same data set was analyzed using other models to extract the threshold voltage presented in literature [37], [39]. In the following these models will be presented in the increasing order of their complexity.

The extrapolation of the transconductance (g_m) in the linear region is used not so often but is as easy to implement as the current extrapolation method which was mentioned above [39], [41]. It is based on the assumptions that when the TFT is in weak inversion, the transconductance depends exponentially on gate bias. In the transition region between weak and strong inversion the dependence is linear. In the strong inversion region g_m is either constant or decreases with U_{gs}, depending on the magnitude of the parasitic resistances and mobility degradation. Therefore, by extrapolating the g_m vs U_{gs} plot in the linear region to zero results in the value of the threshold voltage. With this method, the extracted U_{th} value was -1.34 V (Figure 9). This method is also valid in the case of a TFT operating in accumulation because the processes occurring while the transistor is being switched on are similar for devices operating in either accumulation or inversion.

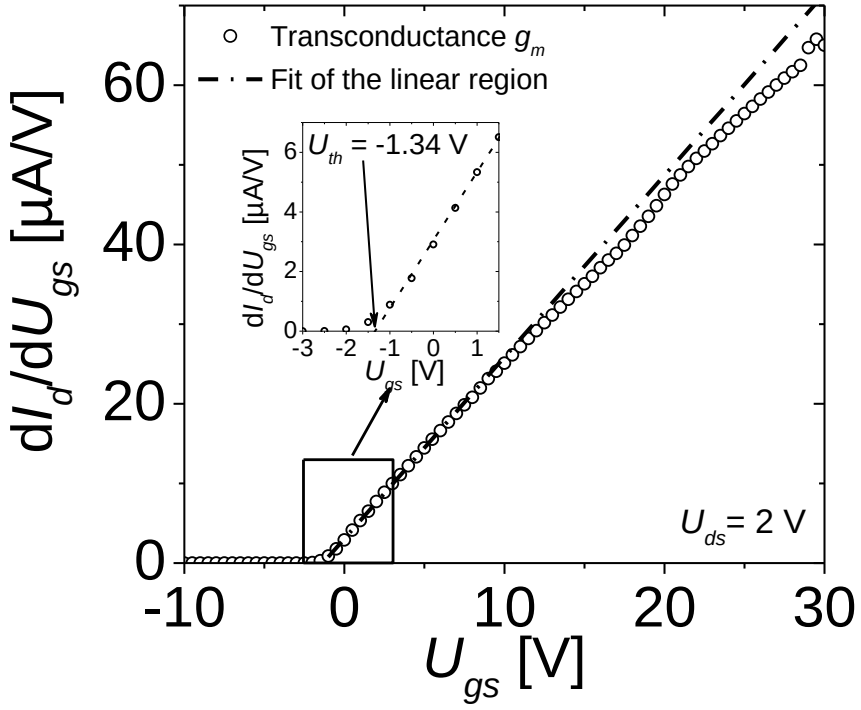

Figure 9. Extraction of the threshold voltage by extrapolating to zero the g_m vs U_{gs} plot in the linear region.

The methods presented in Figure 10 are both based on taking the second derivative of current-related quantities with respect to the gate bias. The method presented in Figure 10 (a) is based on finding the point of maximum slope on the g_m-U_{gs} curve [42]. The U_{gs} at which the first derivative of the curve presented in Figure 9 reaches its maximum is the U_{th} of the tested device. The idea behind this method is the consideration of an ideal device, who's current is zero for $U_{gs} < U_{th}$ and increases linearly for $U_{gs} > U_{th}$. This means that the first derivative of such a curve would be a step function and the second derivative would tend to infinity at U_{th}. Since the tested device is not ideal and its *I-V* curve is already dominated by nonlinearity, the second derivative of this curve displays a maximum at $U_{gs} = U_{th}$.

The method presented in Figure 10 (b) was proposed in 1995 by Aoyama [43] and is based on taking the second derivative of the natural logarithm of the drain-source current with respect to the gate bias. The resulting curve should present a minimum at the point where $U_{gs} = U_{th}$, e.g. where the drift and diffusion currents are equal to each other. According to the author, this method is applicable to a MOSFET in either linear or saturation regime, which makes it more practical than the extrapolation of the current in the linear region method. In addition, the former overcomes the issue of the nonlinearity of the drain-

source current in the linear region which normally makes the application of the latter difficult.

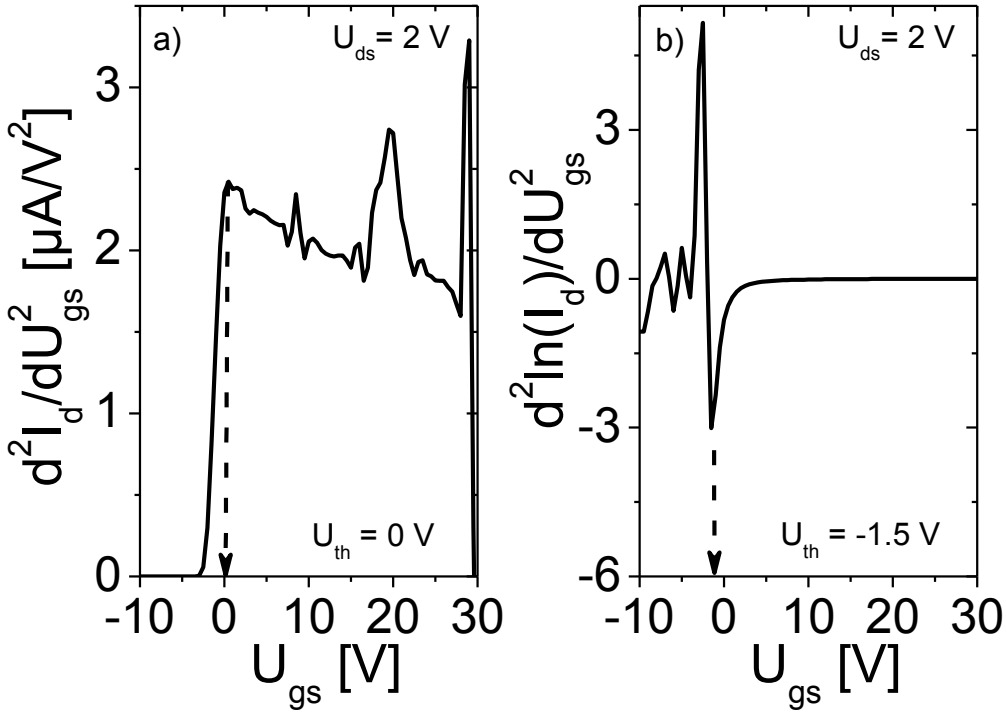

Figure 10. Second derivative of I_d taken with respect to U_{gs} (a) and second derivative of the natural logarithm of I_d with respect to U_{gs} (b).

The application of these methods yields the following values for U_{th}: 0 V for the second derivative of I_d and -1.5 V for the second derivative of ln(I_d). The main disadvantage of these 2 methods is the strong dependence on measurement conditions, i.e. measurement speed and step. The accuracy of the result is a direct result of the step magnitude, in this case the error being as large as 0.5 V. Reducing the step introduces measurement noise, which is being strongly amplified by differentiating twice (the derivative function being a high-pass filter [39]).

In their paper form 1997 [44], Ortiz-Conde *et al.* introduce an Integral Method to determine the threshold voltage by circumventing the parasitic source and drain series resistances of a MOSFET. They define a function D_{MOS}, based on theoretical considerations described earlier [45], [46], in the following way:

$$D_{MOS} = \int_0^{I_{max}} UdI - \int_0^{U_{max}} IdU \qquad (17)$$

where I_{max} and U_{max} are the device's maximum current and voltage. By applying a change of variables: $U_{gs} \rightarrow U_{gb}$, defined as $U_{gb}=U_{max}-U_{gs}$, and introducing a new variable, the total resistance of the device defined as $R_m=U_{ds}/I_d$, they transform equation (17) into the following:

$$\begin{aligned} D_{MOS}\left(R_m U_{gb}, U_{gb}\right) &= \int_0^{\left(R_m U_{gb}\right)} U_{gb}\, d\left(R_m U_{gb}\right) - \int_0^{U_{gb}} \left(R_m U_{gb}\right) dU_{gb} \\ &= R_m U_{gb}^2 - 2\int_0^{U_{gb}} \left(R_m U_{gb}\right) dU_{gb} \end{aligned} \tag{18}$$

The authors apply the standard model in order to define the current-voltage relationship:

$$I_d \cong f\left(U_{gs} - U_{th}\right) U_{ds} \tag{19}$$

with f containing information about the channel geometry (W/L), gate capacitance per unit area (C_i) and effective mobility (μ_{eff}). In their further derivation they apply the mobility degradation model, where the effective mobility is gate voltage dependent and expressed in terms of the constant bulk mobility μ_0 and the mobility degradation factor θ.

$$\mu_{eff} = \frac{\mu_0}{1+\theta\left(U_{gs} - U_{th}\right)} \tag{20}$$

Keeping this in mind the current expression becomes:

$$I_d = \frac{K\left(U_{gs} - U_{th}\right)}{1+\theta\left(U_{gs} - U_{th}\right)} U_{ds} \tag{21}$$

where the constant K contains only information about the channel width and length (W/L), gate capacitance per unit area (C_i) and the constant bulk mobility μ_0.

Combining equations (18) and (21) one obtains the fitting model to be applied to the measured data:

$$D_{MOS}\left(U_{gb}, R_m U_{gb}\right) = \frac{2U_{gb}}{K} + \frac{U_{gb}^2}{K\left(U_{\max} - U_{th} - U_{gb}\right)} + \frac{2\left(U_{\max} - U_{th}\right)}{K} \ln\left[1 - \frac{U_{gb}}{\left(U_{\max} - U_{th}\right)}\right] \tag{22}$$

Fitting this equation to the calculated curve using the measured I-V data one can extract the threshold voltage U_{th} and the K parameter, out of which one could calculate the bulk charge carrier mobility μ_0. Applying this method to the data set investigated in this analysis,

the following parameters were extracted (Figure 11): U_{th} = 3.29 V and K = 9.22×10^{-6} A/V^2. With W = 2000 µm, L = 20 µm and C_i = 1.5×10^{-8} F/cm², the bulk mobility is μ_0 = 6.15 cm²/Vs. This value is surprisingly small compared to the values extracted so far using other models.

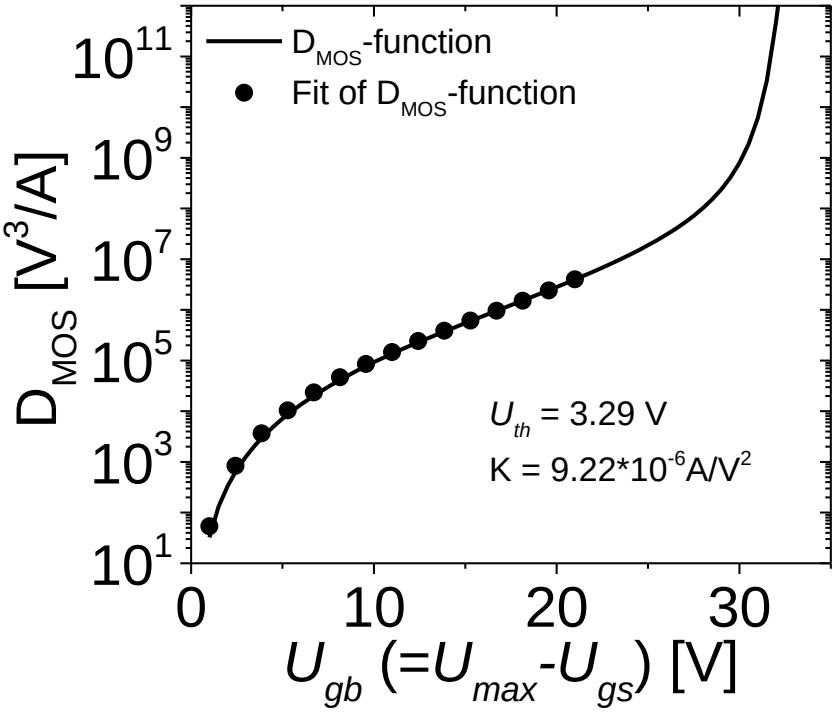

Figure 11. Application of the Integral Method to the calculated curve out of the measured *I-V* data to extract the threshold voltage.

It is worth mentioning, however, that the substitutions made in equations (20) and (21) are unnecessary, since inserting equation (19) (with f replaced by K) in equation (18), then solving the integral results in exactly the same expression as (22). This means that the K parameter contains the gate-voltage-dependent mobility which will affect the integration of (18). This makes the application of this method questionable.

A more appropriate way to avoid the gate voltage dependence of the K parameter is to use a method mentioned in [39], applied to non-crystalline MOSFETs whose current-voltage characteristics are nonlinear in the strong inversion region and are therefore modeled by the following equation:

$$I_{dSat} = K\left(U_{gs} - U_{th}\right)^m \tag{23}$$

In equation (23) the parameter K contains the same information as in the previous model, but this time can be safely assumed to be gate bias independent since the mobility's gate voltage dependence is reflected in the exponent m. The only downside of this model is the

fact that it requires the device to be in the saturation regime, while the entire analysis up to now was based on the idea that the measured TFT was operating in the linear regime. Nevertheless, the gate-voltage-dependent mobility model presented earlier produced a disorder parameter $\gamma \approx 1$, which makes the current dependence on gate bias quadratic. Replacing the mobility in the standard model with the expression (15) and rearranging it so that *K* contains the drain-source voltage and the U_{aa} parameter, e.g.

$$K = \frac{W}{L} C_i \mu_0 \frac{U_{ds}}{U_{aa}^{\gamma}} \tag{24}$$

allows *m* to be written as $m = \gamma + 1$.

With this in mind and replacing U_{gs}-U_{th} with U_g, one computes the following function using the measured *I*-*V* data:

$$H(U_g) = \frac{\int_0^{U_g} I_{dSat}(U_g)\,dU_g}{I_{dSat}} \tag{25}$$

Since the contribution of the integral in the subthreshold region is insignificant, one replaces the lower integration limit with U_{th}, which results in:

$$H(U_g) = \frac{(U_g - U_{th})}{m+1} = \frac{(U_{gs} - 2U_{th})}{m+1} \tag{26}$$

Computing the $H(U_g)$ function as defined in (25) and plotting the resulting data against U_{gs} allows one to determine *m* out of the slope of the graph and U_{th} as one half of the *x*-axis intercept (Figure 12). For the present data set the following values were extracted using this method: U_{th} = -1.37 V and *m* = 1.97, which results in a γ = 0.97, the same value extracted with the gate-voltage-dependent mobility model. With these values of Uth and m the slope of the I_{dSat} vs $(U_{gs}-U_{th})^m$ curve gives the value of the *K* parameter, which in this case is 1.20×10^{-6} A/V$^{1.97}$. And finally, equation (24) results in a mobility μ_0 = 22.14 cm²/Vs, which is fairly close to the value extracted with the gate-voltage-dependent mobility model.

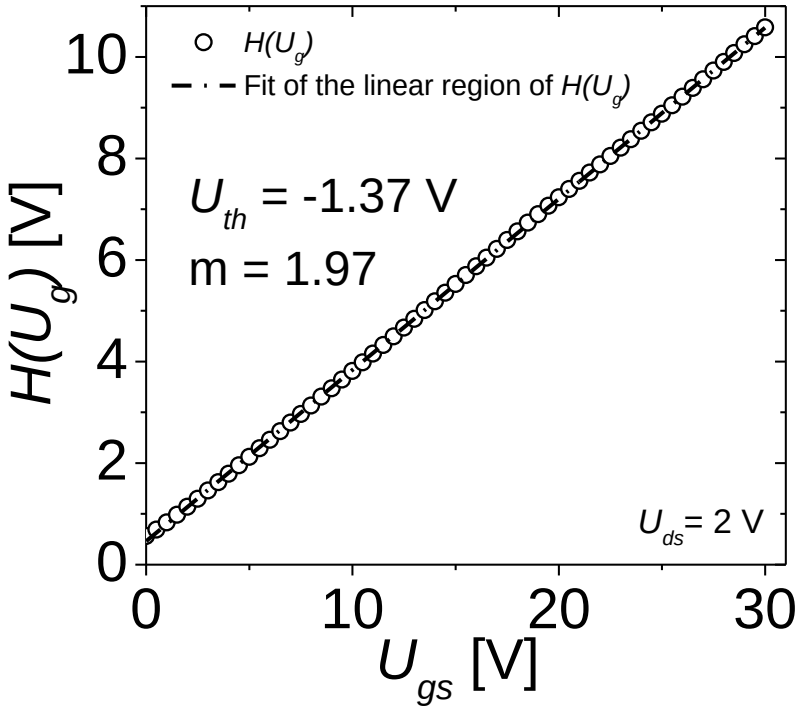

Figure 12. Plot of the computed *H(U$_g$)* function against gate bias for slope and *x*-intercept extraction.

Table 1 summarizes the results of the applied threshold voltage extraction models, together with calculated mobility values, where applicable.

Table 1. Summary of the extracted threshold voltages and charge carrier mobilities were applicable.

Applied model	Threshold voltage [V]	Mobility [cm²/Vs]
Extrapolation in the Linear Region	12.45 ± 0.12	20.04 ± 0.16
Gate-voltage-dependent Mobility	-1.44 ± 0.04	21.11 ± 0.02
Extrapolation of the Transconductance	-1.34 ± 0.02	0.76 ± 0.01
2nd derivative of I_d	0 ± 0.5	-
2nd derivative of ln(I_d)	-1.5 ± 0.5	-
Integral Method (D-function)	3.30 ± 0.04	6.15 ± 0.06
H-function method	-1.37 ± 0.02	22.14 ± 0.01

From the summary in Table 1 one can conclude that the gate-voltage-dependent mobility model produces reasonable values for the μ_0 and U_{th} parameters. It is much easier to implement than the Integral method or the H-function method for example. It does not

introduce additional uncertainties arising from the subjective choice of a fitting region (extrapolation methods). It avoids controversies based on the assumption of the regime of operation (as long as a low enough U_{ds} is applied), like the H-function method for example, which produces apparently acceptable results but is applied in the wrong conduction regime. Therefore the use of this model for the data analysis presented in this work seems justified.

2.2.4. Contact resistance and sheet resistance

The mismatch in Fermi levels of the contacts' and semiconductor materials gives rise to an energy barrier – a parasitic resistance – at the contact-semiconductor interface which interferes with the charge injection. This parasitic resistance is known as contact resistance [37].

Just like with other parameters, there are several methods used to extract the contact resistance out of *I-V* measurements. One method is to replace U_{ds} in the standard model with a corrected U_d which accounts for the voltage drop across the source and drain electrodes, and correct U_{gs} for the voltage drop across the drain electrode [39]:

$$I_d = \frac{W}{L} C_i \mu_n \left(U_g - U_{th}\right) U_d \tag{27}$$

where $U_d = U_{ds} - I_d(R_s+R_d) = U_{ds} - I_d R_{sd}$ and $U_g = U_{gs} - I_d R_d = U_{gs} - I_d R_{sd}/2$, since R_s and R_d are usually considered equal. U_{gs} and U_{ds} are the external applied gate-source and drain-source voltages respectively. Thus equation (27) becomes:

$$I_d = \frac{W}{L} C_i \mu_n \left[\left(U_{gs} - I_d \frac{R_{sd}}{2}\right) - U_{th}\right]\left(U_{ds} - I_d R_{sd}\right) \tag{28}$$

Equation (28) can now be rearranged and used to fit the *I-V* curves to extract the contact resistance. The resulting fit equation however, is the root of a quadratic equation and has a complicated form. If in addition one applies the gate-voltage-dependent mobility model with the corrected gate voltage, then solving the resulting expression for I_d becomes close to impossible. A work-around would be to correct only the drain-source voltage and simplify equation (28) so that it can be used for fitting, but because of this simplification the resulting R_{sd} values often make no sense and are highly susceptible to small variations in U_{th}, μ_0 and γ.

An easier to implement method is the so called *Transfer Line Method* (TLM) [25], [37], [47]. It originates from the idea that the total resistance of a transistor is the sum of the channel resistance and the contact resistances: $R_{tot} = R_{ch} + R_c$, again considering that the source and drain resistances are equal and together form R_c. Therefore one can write:

$$R_{tot} = \frac{U_{ds}}{I_d} = \left[\frac{W}{L} C_i \mu_n \left(U_{gs} - U_{th} \right) \right]^{-1} \tag{29}$$

One normally talks about the width-normalized total resistance, hence both sides of (29) are multiplied with the channel width *W*.

$$WR_{tot} = LR_{sh} + WR_c \tag{30}$$

R_{sh} is the geometry independent sheet resistance, which when multiplied by *L/W* gives the channel resistance R_{ch}. Plotting the width-normalized total resistance against channel length, should result in a straight line whose *y*-intercept is the width-normalized contact resistance with units of length times resistance. The *x*-intercept of this curve yields a correction term for the channel length, ΔL. The slope of the line is then the sheet resistance, with units of resistance, independent on the geometry of the channel, which could serve as a good figure of merit to compare different channel materials. Extracting the total resistance for different channel lengths and gate-source voltages allows extracting the contact and sheet resistances as a function of the applied gate bias. Figure 13 shows the application of the TLM to a set of measured data with the inset illustrating the dependence of the extracted contact resistance on the applied gate bias.

This model though, is also not ideal. For the data collection it is necessary to measure different transistors, which are assumed to be morphologically and structurally identical. This assumption generally does not hold for disordered, solution-processable materials, which introduces rather large measurement errors. Another issue of this model is its resolution. When the contact resistance is very small, this method will often yield physically nonsensical resistance values. Therefore one should remain vigilant about the factors that might influence the outcome of the analysis using this model.

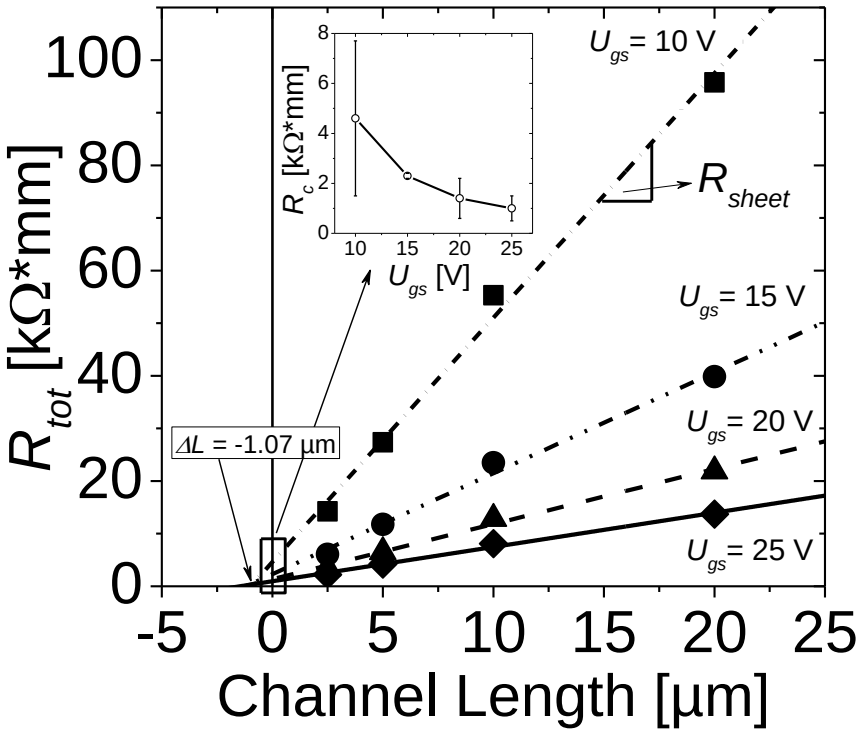

Figure 13. The application of the TLM method to extract the contact and sheet resistance from a given set of measured data.

Other methods of measuring the contact resistance are the four-point and six-point measurement methods, but they require particular measurement set-ups and sample architecture [37].

2.2.5. Subthreshold swing

Another important figure of merit for quantifying the performance of semiconductors is the subthreshold swing, or its reciprocal, subthreshold slope [8], [48], [49]. It represents the quantity which shows how quickly a transistor can be switched on and off, which is very important in high frequency electronics. It can be determined from the equation:

$$S = \left(\frac{d \log(I_d)}{dU_{gs}} \right)^{-1} \tag{31}$$

The value of the subthreshold swing is the inverse of the maximum of the first derivative of the decimal logarithm of the drain-source current with respect to the applied gate bias. It has the units of volts per decade, and shows how much the gate voltage should be increased to produce an order of magnitude increase in the drain-source current level. The value of the

subthreshold swing can be used to determine the density of trap states (N_t) at the interface between the semiconductor and insulator via the following equation [8], [50], [51]:

$$N_t = \frac{C_i}{q}\left[\frac{qS\log(e)}{k_B T} - 1\right] \tag{32}$$

with C_i being the capacitance per unit area of the insulator, q – elementary charge, S is the subthreshold swing from (31), k_B is the Boltzmann constant and T is the temperature.

2.3. Density of states of interface traps

Lee *et al.* [52], [53] and Im *et al.* [54] proposed an optical method to investigate the interfacial trap states and their energetic distribution inside the band gap of a semiconductor. The authors illuminated the conductive channel of the measured TFT with light of different wavelengths, e.g. the energy of the photons ε was varied. Once ε was large enough to reach a trap level below the conduction band minimum (CBM), the electrons trapped in this particular energy level would be excited into the CBM where they could contribute to conduction. The effect of this would be a shift of the threshold voltage depending on the density of electrons in the particular trap level and the energy of the incoming photons:

$$U_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_i} + \psi_{s,\max} + \frac{Q_G}{C_i} \tag{33}$$

In equation (33) $Q_{eff}(\varepsilon)$ is the effective charge that can be excited by the photons of energy ε into the CBM, C_i is the capacitance per unit area of the dielectric material, ϕ_{ms} is the metal-semiconductor work function difference, $\psi_{s,max}$ is the potential due to band bending of the semiconductor and Q_G is the charge induced in the channel by the gate bias.

For an n-type semiconductor the expression of the photo-induced charge is as follows:

$$Q_{eff}(\varepsilon) = q\int_{VBM}^{CBM-\varepsilon} D_{it,e}(E)F(E)dE - qN_b d_{ox} \tag{34}$$

where q is the elementary charge, N_b and d_{ox} are the dielectric bulk trap density and its thickness respectively, $F(E)$ is the Fermi-Dirac distribution and $D_{it,e}$ is the density of states (DOS) of electrons at the semiconductor-insulator interface. To simplify the integration of (34), the authors assume a 0 K step function for $F(E)$ and set it to 1. Since ϕ_{ms}, $\psi_{s,max}$ and Q_G

are independent of the photon energy ε, differentiating both sides of (33) with respect to ε will result in the expression:

$$\frac{\partial U_{th}(\varepsilon)}{\partial \varepsilon} = -C_i^{-1} \frac{\partial Q_{eff}(\varepsilon)}{\partial \varepsilon} \tag{35}$$

Using the definition of $Q_{eff}(\varepsilon)$ from (34), equation (35) becomes:

$$D_{it,e}(CBM - \varepsilon) = \frac{C_i}{q} \frac{\partial U_{th}(\varepsilon)}{\partial \varepsilon} \tag{36}$$

With equation (36) one can calculate the energetic profile inside the band gap under the CBM and visualize it as a function of the incident energy.

One can also apply this method to verify the positions of the activation energies determined from the plots of the natural logarithm of mobility against the inverse temperature (Arrhenius plots) by measuring the mobility as a function of temperature. Since ϕ_{ms}, $\psi_{s,max}$ and Q_G are also temperature independent, one can replace the photon energy ε with thermal energy and go through the derivation to arrive at equation (36). The advantage of this method is that in addition to the position of the trap density maxima in the band gap, one can determine also the magnitude of the density of these trap states. The downside of combining this method with a thermal measurement is that the energetic interval scanned by varying the temperature of the substrate is not as wide as can be achieved with photon energy.

3

State Of The Art

3.1. A brief history of transparent amorphous semiconductors

> ***"High transparency to visible radiation is incompatible with high electrical conductivity in most solid crystalline materials. This condition is also true for amorphous materials." [Hosono et al., 1996]***

In 1996 Hosono *et al.* published an article, starting with the above quote, in which they discussed the possibility to create a transparent conductive material which was much needed in the liquid crystal display and solar cells industries [14]. Such a material should have the following properties:

1. have a wide band gap
2. be transparent to visible radiation
3. have a high conductivity, i.e. (semi-)conductor with high electron mobility
4. be in an amorphous state.

They looked at the ongoing research at that time and noticed that materials partially fulfilling these requirements were mainly *oxides of heavy metal cations* (HMCs). Among these were Indium-Tin-Oxide, Magnesium-Indium-Oxide, Zinc-Gallium-Oxide, Zinc-Aluminum-Oxide and others [14], [55], [56], [57]. All four requirements were fulfilled by amorphous Indium Oxide which started attracting ever increasing attention [58], [59], [60].

Based on their findings, the authors postulated that in order for a material to possess all four properties, the orbitals of the atoms composing it should display a significant overlap and be insensitive to spatial/directional randomness inherent to amorphous materials. Therefore HMCs with the electronic configuration $(n\text{-}1)d^{10}ns^{0}$ should fulfill these requirements, since their spherical orbitals have a large spatial spread and, once in a solid, the necessary overlap. They proposed that the suitable HMC candidates were located in groups 11-15, periods 4-6 in the periodic table of elements (Figure 14). In order to suppress

crystallization it was decided to investigate double cation oxides, and because the identified candidates would result in 105 possible combinations, they focused their research on three combinations: a-$AgSbO_3$, a-Cd_2PbO_4 and a-Cd_2GeO_4.

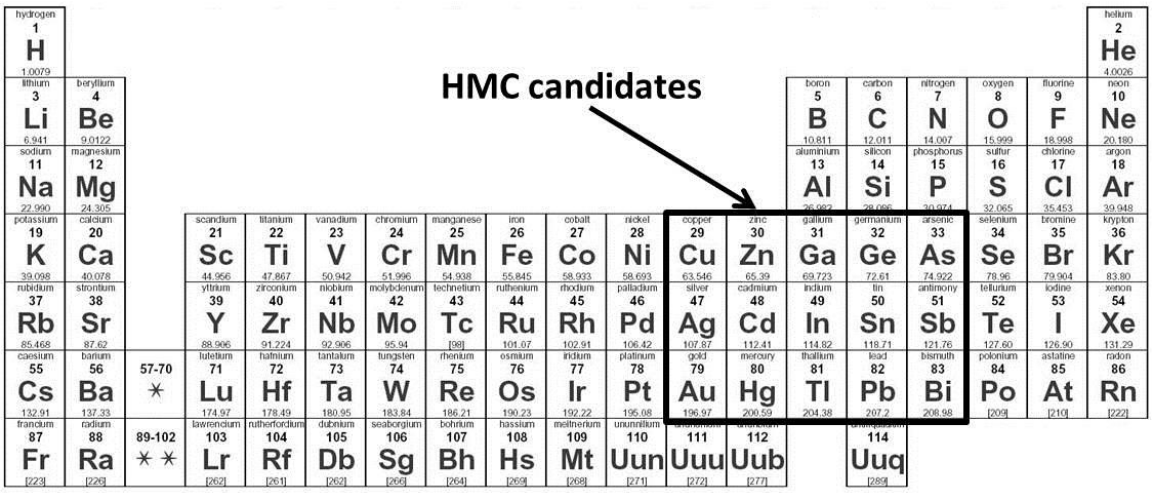

Figure 14. Heavy metal cation candidates for transparent conductive oxides. Figure from [14].

The authors reported high transparency and conductivity for the investigated systems, as well as charge carrier mobilities of ~10 cm^2/Vs, values close to those of a-In_2O_3 and several orders of magnitude larger than those of a-Si:H at that time [14]. Excessive ion implantation or oxygen vacancy formation via thermal annealing were mentioned as methods to increase the charge carrier concentration.

Later Kamiya *et al.* extended the understanding of the physics of conduction in amorphous oxides by explaining how the Madelung potential, formed when an oxygen atom is brought close to a metal atom, is responsible for the good conduction and large band gap [61]. The said potential raises the energy levels of the metal and lowers those of the oxygen, stabilizing the ionized states. The electrons from the metal *ns* orbitals fall into the oxygen's 2p orbitals, which form the valence band maximum (VBM) and the empty cation orbitals form the conduction band minimum (CBM). Due to the spatial spread and overlap of the cations' orbitals, a wide conduction band is formed which facilitates the conduction even in an amorphous material [11].

The research into transparent (semi-)conductors at that time was mainly focused on the development of transparent electrodes and not so much on oxide thin film transistors. There were, however, several papers on the use of metal oxides as the active channel of TFTs published in the years following Hosono's review.

In 1997 Gómez *et al.* published a paper about indium doping of zinc oxide films [62]. They deposited a methanolic solution of zinc acetate "doped" with different indium sources (nitrate, acetate and sulfate) up to 4 at% via *Spray Pyrolysis* (SP) on substrates of different temperatures ranging from 400°C to 525°C. The reported Hall mobility reached a maximum of 12 cm^2/Vs between 450°C and 500°C.

In 1999 Kim et al. reported the deposition of high mobility ITO layers via *Pulsed Laser Deposition* (PLD). Their 170 nm-thick films deposited at 300°C had a Hall mobility of 29 cm^2/Vs.

According to Kamiya and Hosono, several reports on crystalline oxide TFTs with ZnO and $InGaZnO_4$ as semiconductor materials in 2003 marked the beginning of the "oxide TFT fever" [11]. The intensive study of the ZnO TFTs was fueled by its ability to reach Hall mobilities over 200 cm^2/Vs in its single-crystal form, which made it a very attractive research topic.

Hoffman *et al.* for instance, published their findings on ion beam sputtered ZnO on aluminum-titanium oxide as gate insulator [63]. They used rapid thermal annealing at 600°C-800°C to increase the resistivity of the ZnO layer and obtained mobility values from 0.3 to 2.5 cm^2/Vs and threshold voltages from 10 to 20 V, stating that the values increased with temperature. Carcia *et al.* deposited their ZnO films by *radio-frequency magnetron sputtering* (RFMS) onto thermally grown SiO_2 gate insulator at room temperature [64]. They calculated maximum field-effect mobility of 40 cm^2/Vs but at a low on/off ratio of 10^3.

Nomura *et al.* [65] and Ohta *et al.* [66] described a method to grow $InGaO_3(ZnO)_5$ single-crystal layers on a ZnO epitaxial layer deposited by PLD on yttria-stabilized zirconia substrates. The deposition of $InGaO_3(ZnO)_5$ was made via reactive solid-phase epitaxy and the single-crystal phase was obtained by annealing the deposited $InGaO_3(ZnO)_5$ film at 1400°C in an atmospheric electric furnace. Nomura and colleagues then deposited ITO as source/drain and gate electrodes and amorphous HfO_2 as gate dielectric via PLD and fabricated a top-gate coplanar TFT, which had an FET mobility of 80 cm^2/Vs [65]. One year later, Nomura *et al.* describe the deposition of an amorphous $InGaZnO_4$ (a-IGZO) layer via PLD, which exhibited a saturation FET mobility between 6 and 9 cm^2/Vs (in combination with a 140 nm Y_2O_3 layer as gate dielectric and ITO for source/drain electrodes) [12].

Different groups also started publishing intensively their findings on a-IGZO TFTs fabricated via different vacuum techniques. Table 2 shows a comparison of these results based on fabrication technique and temperature, elemental composition of the semiconductor, TFT architecture and dielectric material. All these parameters were shown to have an impact on the TFT performance, i.e. on the calculated charge carrier mobility and device stability.

The results in Table 2 are grouped according to temperature which was used to anneal the TFTs after active layer deposition and regions of the same temperature are delimited with horizontal lines to assist the reader. These data supports the uniformity of the reported results on sputtered a-IGZO systems.

On the side of the material composition itself, there is not much variation observed. The ratio of the individual components in the sputtering target used for the active layer fabrication is usually reported as IGZO 1:1:1 target, or In_2O_3, Ga_2O_3 and ZnO 1:1:1. This raises the question whether both compositions are equivalent or in the letter case the amount of In and Ga atoms is twice the amount of Zn atoms. In any case, this should be kept in mind when reading Table 2, since the latter case was marked as IGZO (2:2:1) and not (1:1:1), as in the respective papers. The charge carrier mobility of all analyzed devices lies between 7 and 20 cm^2/Vs, depending mainly on the nature of the gate insulator. The mobility of the devices having SiO_2 as dielectric are normally in the lower part of this range, and devices whose gate was insulated with Al_2O_3 or SiN_x have mobilities above 14-15 cm^2/Vs, although exceptions are present in both groups.

The post-deposition annealing temperature and deposition technique do not exhibit a significant influence on the performance of the devices. It must be noted that for most of the devices *W/L* is comparably small and a weak inverse dependence of the mobility on the magnitude of this parameter can be observed in Figure 15. Unless stated otherwise, the architecture of these devices was a bottom gate – top contact one, although this parameter has also little influence on the device performance in this summary.

The relatively small spread of the measured mobility values must be due to the effective controllability of the active channel chemistry inherent to the vacuum deposition techniques. These methods normally produce films of high purity and of a well-defined composition attributed to the ability to tune the sputter target and atmosphere chemistries.

Table 2. Summary of the work performed by various research groups on a-IGZO in the period between 2003 and 2012.

Material	Film thickness [nm]	W/L	Gate insulator	Mobility [cm^2/Vs]	Annealing temperature[°C]	Deposition method
IGZO (1:1:1) [67]	40	6.00	150 nm SiO_2	12.6	400*	PLD
IGZO [68]	40	6.00	150 nm SiO_2	10-13	400	PLD
IGZO [69]	90	2.50	200 nm SiN_x	10	350	RFMS
IGZO (2:4:1) [41]	120	3.00	(d) 200 nm SiO_2	7.6	350	Sputtered
IGZO [70]	50	10.00	200 nm SiN_x	11.7	350	DC-sputtering
IGZO (2:2:1) [71]	50	3.00	100 nm SiO_2	9.7	350	RFMS
IGZO (1:1:1) [40]	30	0.7-4.4	(b) 300 nm SiO_2	11.99	330	DCMS
IGZO (1:1:1) [72]	22-28	2.00	(b) 150 nm Al_2O_3	18	300	RFMS
IGZO (1:1:1) [73]	40	10.00	100 nm SiO_2	6.7	300	RFMS
IGZO [74]	50	2.00	(t) 190 nm Al_2O_3	16.5	300	RFMS
IGZO (2:2:1) [75]	70	2.00	400 nm SiN_x	14	300	RFMS
IGZO [28]	30	1.00	(t) 176 nm Al_2O_3	18	300	Sputtered
IGZO (4:4:1) [50]	50	1.40	200 nm TEOS	13.19	300	DCMS
IGZO [76]	5	0.45	80 nm SiO_2	31	250	DCMS
IGZO (2:2:1) [77]	70	6.25	100 nm SiO_2	14.8	250	RFMS
IGZO [78]	-	2.90	SiO_2	19.1 to 22.3	250	DC-sputtering
IGZO [33]	30	6.00	200 nm SiO_2	8.3 - 9.51	200	RF-sputtering
IGZO (2:2:1) [79]	70	10.25	SiN_x	9.2	200	RFMS
IGZO [80]	-	1.18	200 nm SiN_x	8.1	200	DC-sputtering
IGZO [81]	50	-	150 nm SiN_x	15.1	200	DC-sputtering
IGZO (2:1:2) [82]	40	1.00	100 nm SiO_2	57.8	200	Sputtering
IGZO [83], [84]	70	4.00	(d) 400 nm SiN_x	16.2	200	RFMS
IGZO [85]	-	5.00	100 nm SiN_x	19.4	100	DCMS
IGZO (1:1:5) [86]	-	4.00	220 nm Al_2O_3/TiO_x	14	RT	PLD
IGZO [15]	50	2.90	120 nm SiO_2	17.7 to 25.7	RT	DC-sputtering
IGZO (2:2:1) [87]	40	2.00	200 nm SiN_x	3.7	RT	Sputtered

* - wet annealed
(d) - double gated
(t) - top gate - bottom contacts
(b) - bottom gate - bottom contacts

Figure 16 summarizes the performance of these TFTs with respect to the thickness of the active layer. A weak dependence can be discerned which shows that the mobility increases slightly with decreasing thickness of the a-IGZO layer.

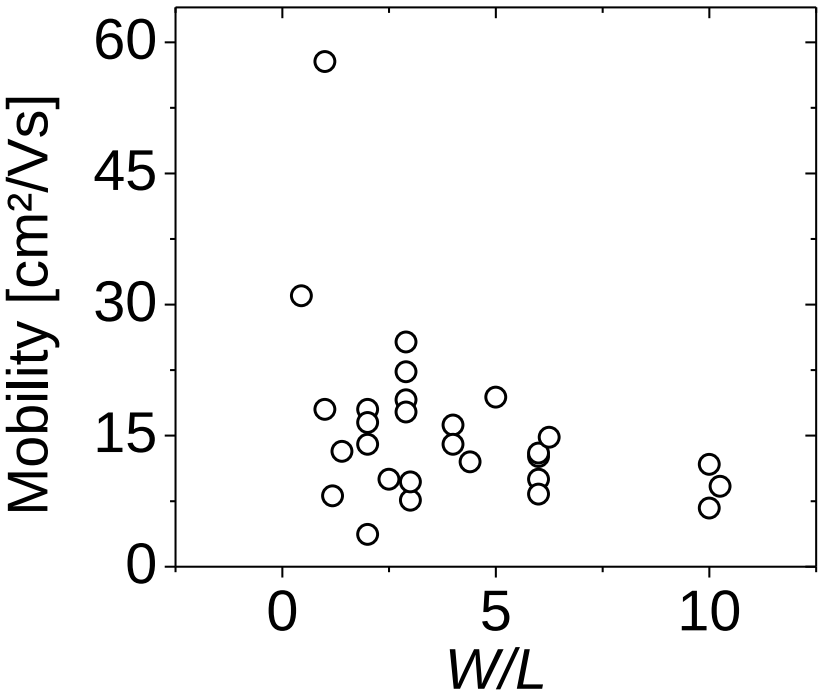

Figure 15. Dependence of the charge carrier mobility on the magnitude of the W/L ratio.

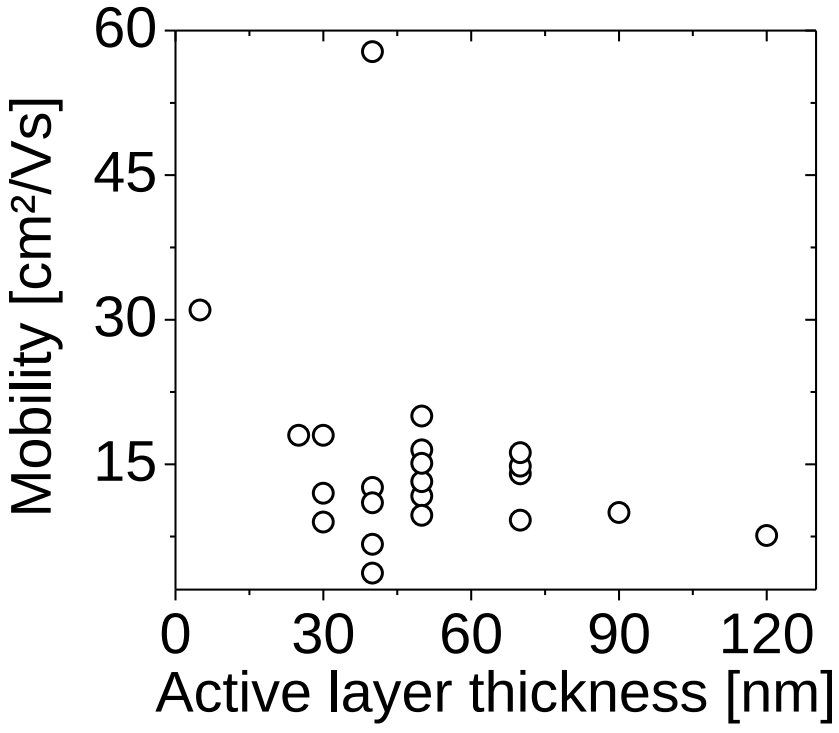

Figure 16. Performance of a-IGZO TFTs as a function of active layer thickness.

Noteworthy are the results of Olziersky *et al.* [82] who used a target with the chemical composition of IGZO – 2:1:2, e.g. half the amount of Ga compared to In or Zn. They also passivated their TFTs with the commercially available SU-8 negative photoresist and

annealed their TFTs at only 200°C. This resulted in FET mobility of 57.8 cm²/Vs, so far highest in the respective class of materials.

Mativenga *et al.* [76] demonstrated a device with a mobility of 31 cm²/Vs by decreasing the thickness of the a-IGZO layer down to 5 nm and using a thin dielectric layer of SiO_2 (80 nm), as well as a bottom gate – top contact configuration with *W/L* = 25/55 µm. They also reported on passivating their TFTs with a 200 nm SiO_2 layer deposited via plasma-enhanced chemical vapor deposition (PECVD), while Olziersky and colleagues claimed that a SiO_2 passivation layer strongly degraded the performance of their TFTs [82].

Some research groups published their findings on other sputtered material systems with a potential similar to that of a-IGZO. These findings are presented in Table 3.

Table 3. Performance of alternative sputtered metal oxide TFTs.

Material		Film thickness [nm]	W/L	Gate insulator	Mobility [cm^2/Vs]	Annealing temperature [°C]	Deposition method
ZnO	[88]	40	2.5	50/100 nm SiO_2/SiN_x	14	375	RFMS
InGaSnO	[89]	50	5.5	100 nm SiO_2	up to 13	330	Sputtered
InZnO	[90]	25	15	SiO_2	25	300	Sputtered
InGeO	[90]	25	15	SiO_2	6	300	Sputtered
InGaO	[90]	25	15	SiO_2	6	300	Sputtered
InSnO	[90]	25	15	SiO_2	inactive	300	Sputtered
ZnO	[91]	-	20	150 nm SiO_2	0.8-2.3	RT	RFMS
ZnO	[92]	100	20	100-150 nm SiO_2	up to 1.6	RT	RFMS
ZnSnO	[93]	60-80	5	220 nm Al_2O_3/TiO_2	10	RT	O_2 Plasma-PLD
InZnO	[94]	30	4.1	220 nm ATO	>100	RT	RFMS

Remarkable are the results reported by Fortunato *et al.* in 2006, in which they report a saturation FET mobility of 107.8 cm^2/Vs for a bottom gate – top contact TFT fabricated at room temperature by RFMS, in which the source and drain contacts were composed of the same material as the active layer (e.g. IZO, Table 3) [94].

The larger spread of the mobility values appearing in Table 3 can be attributed to the variation in the active layer's material composition, in addition to the various structural differences. The various cation systems have different charge carrier concentrations

resulting from different oxygen binding capacities of the constituent atoms [14], which is responsible for the observed mobility spread.

This analysis demonstrates that the mobility is not a very suitable figure of merit to compare devices fabricated by different groups since it cannot be considered a material parameter. It depends on various aspects of the device structure, interface properties, channel geometry, contact material [95] (not discussed here) and even passivation material. It may be used by the same group to compare the performance of their TFTs when systematically varying one of these parameters or the other. However, the complexity of the influence of the entire TFT ensemble on the mobility of the electrons in its conductive channel and the sheer variety of TFT architectures fabricated by different groups makes the intergroup comparison of this figure of merit alone[1] unwise.

3.2. Solution processed metal oxide TFTs

The application of sputtering techniques to fabricate oxide TFTs presents the advantage of strict control over the chemical composition and purity of the deposited films. The ever increasing size of industrially used substrates however makes the implementation of vacuum techniques increase the production costs dramatically. Many research groups have concentrated their efforts on solving the cost issue by developing metal oxides which can be deposited from solution and processed in ambient conditions. This would enable large area processing via printing or slot die coating. Combine these methods with a low temperature process, and one could coat plastic substrates and eventually produce flexible devices in a roll to roll manner. Table 4 illustrates an overview on the work done in this direction in the last five years with an emphasis on the more recent publications.

The results in Table 4 were also grouped according to fabrication temperature and separated by horizontal lines for ease of viewing. An important observation is the fact that the processing temperature for solution processed metal oxides is much higher than for sputtered materials. The reason behind this will be discussed in detail later. At this point it suffices to mention the importance of the processing temperature in the performance of metal oxide TFTs with active layers deposited from solution. This is illustrated in Figure 17, where the charge carrier mobility is plotted against the processing temperature.

[1] Disregarding the structural information of the TFT

Table 4. Overview of the published work on solution processed metal oxide TFTs in the last 5 years.

Material		Film thickness [nm]	W/L	Gate insulator	Mobility [cm²/Vs]	Annealing temperature [°C]
InZnSnO	[96]	-	7	100 nm SiO_2	30*	600
InZnSnO	[96]	-	7	200 nm SiO_2 #	1.2*	600
ZnO	[97]	15	8.30	100 nm SiO_2	9.4	600
IGZO (5:1:2)	[98]	20	5.00	200 nm SiO_2	6.4	600
LIZO	[99]	40	6.60	SiNx	3.86	550
YIZO	[100]	40	14.30	200 nm SiN_x	1.12	550
IGZO (3:1:2)	[100]	40	14.30	200 nm SiN_x	0.46	550
GSZO	[101]	30	NA	NA	1-1.2	500
ZTO	[102]	20	11.10	AlSnOx	5.2	500
IGZO	[103]	30-40	40-4	200 nm SiO_2	6.95	500
ZrIZO	[104]	-	6.60	200 nm SiN_x	0.82	500
ZrIZO	[104]	-	-	200 nm SiO_2	0.4	500
IZO	[105]	10	8.30	120 nm SiO_2	7.30	500
In_2O_3	[20]	-	-	SiO_2	55.26	500
IGZO (1:1:2)	[106]	-	6.70	SiN_x	0.03*	450
IGZO (1:1:2)	[106]	-	6.70	SiN_x	0.96	450
IGZO (5:5:1)	[107]	-	6.66	200 nm SiN_x #	0.96	450
ZnO	[97]	15	8.30	100 nm SiO_2	1.44	400
IZO (7:3)	[17]	-	10.00	300 nm SiO_2	1.54	400
IGZO (63:10:27)	[17]	-	10.00	300 nm SiO_2	0.85	400
IGZO	[108]	40	-	SiN_x	1.25	400
In_2O_3	[109]	30	-	16.5 nm SAND	43.7	400
In_2O_3	[109]	30	-	300 nm SiO_2	0.7	400
IGZO	[49]	20	5.00	ATO	11.2	400
IGZO	[49]	20	5.00	ATO	7.2	350
IGZO	[49]	20	5.00	ATO	2.7	300
ZnSnO	[110]	80	10.00	300 nm SiN_x #	N/A	350
AlInO	[111]	-	10.00	100 nm SiO_2	13.4	350
AlInO	[111]	-	10.00	100 nm SiO_2	0.36	250
IGZO (63:10:27)	[17]	-	10.00	300 nm SiO_2	0.05	250
IZO (7:3)	[21]	20	5.00	100 nm SiO_2	14	250
In_2O_3	[112]	-	20.00	300 mn SiO_2	5.92	400
		-	20.00	300 mn SiO_2	2.3	300
		-	20.00	300 mn SiO_2	9.4	325 (c)
		-	20.00	300 mn SiO_2	6.5	300 (c)
ZTO	[112]	-	20.00	300 mn SiO_2	1.67	400
		-	20.00	300 mn SiO_2	3.03	300 (c)
IZO	[112]	-	20.00	300 mn SiO_2	2.14	400
		-	20.00	300 mn SiO_2	1.37	350
		-	20.00	300 mn SiO_2	3.2	300 (c)

*- InkJet printred

#- Bottom Gate - Bottom Contact architecture

(c)-combustion process

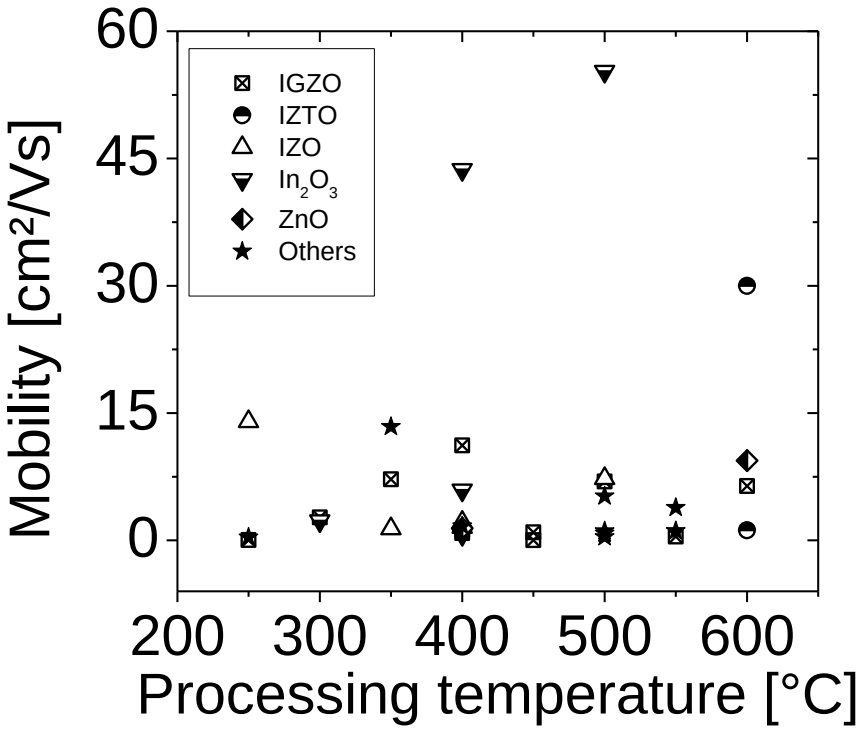

Figure 17. Dependence of solution processed metal oxide TFT performance on processing temperature and composition of the active layer.

The variety of compositions of the metal oxide formulations makes it hard to interpret the data in Table 4, therefore the graphical representation of the dependence of the mobility on temperature was grouped according to material composition to somewhat facilitate the analysis (Figure 17), although the ratio of components in a given material may differ from group to group as well. In general Figure 17 shows that the mobility tends to increase with temperature for any given material, and this is due to 2 main functions that the thermal annealing step has during TFT fabrication using solution processed metal oxides.

A metal oxide formulation is prepared by either dissolving metal compounds or suspending metal oxide nanoparticles in a solvent. In addition to that, very often a stabilizer is added to the formulation in order to stabilize it and prevent precipitation of the solutes. In order to increase the performance of the deposited (be it via spin coating, slot die coating, printing, spray pyrolysis or any other suitable method) film, anything that is not the metal cations or oxygen atoms must go. The solvents and anions of the metal compounds have to decompose and/or evaporate out of the film, which requires an input of energy, usually in the form of temperature.

The second role of the thermal annealing is to consolidate the metal oxide network by providing the necessary energy to form the metal-oxygen bonds. Therefore, the higher the temperature applied to the film, the better the removal of unwanted species from the film and the higher the quality of the metal oxide film.

Unfortunately temperatures of 600°C are incompatible even with glass substrates when it comes to large area application due to warping of the substrate and resulting non uniform processing of the entire substrate. In order to make a solution process industrially viable, it is crucial to decrease the processing temperature as much as possible. Many research groups have set the goal to decrease the processing temperature to values compatible with glass substrates (250°C – 350°C) or even lower, compatible with plastic substrates (100°C – 250°C). This can be achieved by modifying the chemistry of the semiconductor formulation (see Table 4), by introducing additional sources of chemical energy into the film [112], replacing or complementing the thermal annealing by other non-thermal energy sources, such as microwave annealing [113], [114], or ultra-violet radiation [115], [116].

Going back to the summary, there are a few results worth discussing in detail. Lee *et al.* fabricated a metal oxide formulation by dissolving indium, zinc and tin chlorides in an acetonitrile/ethylene glycol mixture [96]. They printed the solution using a DIMATIX (DMP-2800) piezo-inkjet printer and annealed the films at 600°C. The TFTs they fabricated were in a bottom gate – top contact configuration with aluminum contacts and SiO_2 as gate insulator, and showed a field-effect mobility of 30 cm^2/Vs.

Han *et al.* fabricated indium oxide bottom gate – top contact TFTs with SiO_2 as insulator and aluminum contacts [20]. They managed to obtain a charge carrier mobility of 55.26 cm^2/Vs for the devices annealed in air at 500°C. For the same device structure annealed in an ozone rich atmosphere at only 280°C, the TFTs displayed a mobility of >22 cm^2/Vs.

Kim *et al.* studied the influence of the chemical composition of the IGZO formulations on the performance of the TFTs [103]. They fabricated solutions with various ratios of the individual components by dissolving indium and gallium nitrate hydrates and zinc acetate in 2-methoxyethanol with ethanolamine as stabilizer. The TFTs they fabricated were also in bottom gate – top contact configuration with SiO_2 as dielectric and aluminum contacts and annealed at 500°C. One important find that the authors report in their paper is that an

increase in indium content in the thin film leads to an increased mobility. The highest Hall mobility they achieved was 6.95 cm^2/Vs.

The importance of the dielectric material in the performance of a TFT was emphasized by Kim *et al.*, as they fabricated TFTs in bottom gate – top contact configuration with SiO_2 or organic self-assembled nanodielectric (SAND) as gate insulator and gold source/drain contacts [109]. The authors dissolved indium chloride and ethanolamine in 2-methoxyethanol to prepare the semiconductor formulation. After deposition, the active layers were annealed at 400°C in a furnace with atmospheric air. While the In_2O_3-SiO_2 TFTs showed a mobility of only 0.7 cm^2/Vs, the In_2O_3-SAND TFTs displayed an impressive μ_{FET} = 43.7 cm^2/Vs. In addition they mentioned that the role of the ethanolamine in the solution is also a non-trivial one and that it improves the film formation and mobility when the ratio of ethanolamine to In^{3+} ions is up to 10%.

Nayak *et al.* present yet another method to improve the performance of IGZO TFTs deposited from solution [49]. The formulation the authors used was prepared by dissolving indium and zinc chlorides, gallium nitrate hydrate and ethanolamine as stabilizer in 2-methoxyethanol. The solution was spin coated on a substrate with aluminum titanium oxide as dielectric and after annealing the film at 400°C, aluminum top contacts were deposited via e-beam evaporation. Before the annealing step some of the TFTs were dried for 5 min at 80°C on a hot plate and treated with O_2-plasma for 45 seconds. These samples displayed a higher mobility than the non-treated samples, reaching 11.2 cm^2/Vs.

Hwang *et al.* introduce humid annealing of the active layer as a method to increase device performance and lower processing temperature [111]. They prepared a semiconductor formulation by dissolving indium and aluminum acetylacetonates in 2-methoxyethanol due to the low decomposition temperature of indium acetylacetonate. The authors fabricated the TFTs in bottom gate – top contact configuration with SiO_2 as gate insulator and aluminum for source and drain contacts. Devices annealed at 350°C in ambient atmosphere for 2 hours had a mobility of 13.4 cm^2/Vs, while those annealed at 250°C only 0.36 cm^2/Vs. They explain the large difference by the presence of a large amount of In(OH) in the 250°C annealed films. In(OH) decomposes at temperatures above 300°C, therefore 250°C are not sufficient to convert the indium precursor into a high quality metal oxide. However, annealing these devices for an additional hour in an oxygen rich humid atmosphere strongly

promotes the oxidation of the film, increasing the performance of the TFTs to μ_{FET} = 2.37 cm^2/Vs.

Banger *et al.* report on lowering the processing temperature by using metal alkoxides as the cation source for the metal oxide films [21]. They dissolved indium and zinc alkoxides in methoxyisopropanol and 2-methoxyethanol respectively and combined them in different ratios. The films were spin coated under inert atmosphere conditions and the annealing at temperatures between 200 and 275°C was performed under clean room conditions with strictly controlled relative humidity of the ambient air. The architecture of the TFTs was a bottom gate – top contacts one, with SiO_2 as dielectric and tungsten source and drain electrodes. The authors report charge carrier mobilities of 14 cm^2/Vs for indium-rich devices annealed at 250°C.

Kim *et al.* modified the chemistry of the semiconductor formulations so that the necessary conversion energy would be supplied chemically, via a redox reaction, which in turn would allow decreasing the input of thermal energy into the system [112]. The authors dissolved indium and zinc nitrate hydrates and tin chloride in 2-methoxyethanol, to which they added NH_4NO_3 (oxidizer) and acetylacetone (fuel). They compared then the performance of various combinations of cations in formulation, i.e. In_2O_3, IZO, ZTO etc. annealed at different temperatures. One more varied parameter was the presence of the redox components. The TFTs were fabricated in a bottom gate – top contacts configuration with Au source/drain electrodes and SiO_2 for dielectric. The indium based devices displayed the highest mobility values at any given annealing temperature. In addition, the combustion process allowed lowering the annealing temperature down to 200°C and to still obtain functioning TFTs, while the TFTs fabricated with conventional annealing methods lost their functionality at much higher temperatures, i.e. 250-300°C. For example an In_2O_3 device annealed at 325°C via the combustion process exhibited a mobility of 9.4 cm^2/Vs.

Song et al. fabricated semiconductor formulations by dissolving zinc acetate dihydrate and indium nitrate hydrate in 2-methoxyethanol and added β-diketone for solution stability (In:Zn ratio was 55:45) [113]. With this formulation they fabricated bottom gate – top contact TFTs with SiO_2 as dielectric and aluminum source/drain contacts. The active layers were annealed at various temperatures via conventional hot plate annealing and via microwave annealing. The latter method allowed them to measure a mobility of 0.1 cm^2/Vs

for a device annealed at 150°C under microwave conditions, while the hot plate-annealed TFT was inactive. At 300°C the microwave TFT had a mobility of 2.12 cm^2/Vs compared to 0.86 cm^2/Vs for the hot plate-annealed device.

Microwave annealing was also used by Jun *et al.* to fabricate a ZnO TFT which achieved a mobility of 1.75 cm^2/Vs at only 140°C annealing temperature [114]. For comparison, the hot plate annealed TFT showed a mobility of only 0.32 cm^2/Vs. The semiconductor formulation was prepared by dissolving zinc hydroxide in aqueous ammonia and the TFTs (bottom gate – top contacts) had SiO_2 as gate insulator and aluminum source/drain contacts.

Hwang *et al.* proposed UV-photo-annealing as yet another method to lower the TFT processing temperature [116]. The authors fabricated the semiconductor formulation by dissolving zinc acetate and tin chloride in 2-methoxyethanol and added acetylacetone as stabilizer. They deposited the semiconductor films on Si/SiO_2 substrates via spin coating and annealed them for 1 hour either on a hot plate in ambient atmosphere, or on a hot plate under a UV lamp. The UV treated samples were then annealed for an additional 2 hours in vacuum at 250°C. The aluminum top source/drain contacts were deposited via e-beam evaporation to complete the TFT fabrication. The samples that were annealed for 1 hour in ambient air were inactive, and after 6 hours on the hot plate had a mobility of only 0.3 cm^2/Vs. The UV plus vacuum annealed TFTs showed a mobility of 2 cm^2/Vs and conducted much higher currents. However, it is difficult to judge the merits of the sole UV annealing method because of the combination with vacuum annealing.

Kim *et al.* have applied the UV-annealing method at room temperature in a nitrogen atmosphere to TFTs with active channels composed of IGZO, IZO or In_2O_3 [115]. The solutions were prepared by dissolving indium and gallium nitrate hydrates and zinc acetate in 2-methoxyethanol. The TFTs were in bottom gate – top contact configuration with Al_2O_3 as gate insulator and IZO source/drain electrodes. The TFTs fabricated via room temperature photo-annealing displayed the following mobility values: 8.76 ± 0.98 cm^2/Vs for the IGZO channels, 4.43 ± 0.59 cm^2/Vs for the IZO channels and 11.29 ± 1.62 cm^2/Vs for the In_2O_3 TFTs. In comparison, thermal annealing at 350°C produced TFTs with the following mobility values: 6.01 ± 0.75 cm^2/Vs for the IGZO channels, 3.72 ± 0.63 cm^2/Vs for the IZO channels and 10.31 ± 1.55 cm^2/Vs for the In_2O_3 active layers.

As this study has shown, a tremendous amount of work has been done in the last decade on amorphous transparent metal oxide semiconductors. The vast advantage of this class of materials stems from their high charge carrier mobility and transparency in the visible range, which makes them attractive for a wide gamut of electronic applications. The research on sputtered materials is dominated by publications on IGZO systems with a relatively narrow spread of chemical compositions, mainly due to the scarcity of sputtering targets with a varied chemical composition. Another preferred material is zinc oxide, due to its historic merits and high performance of single crystal devices. Other material systems appear in literature as well, but not as often as the a-IGZO (compare Table 2 and Table 3). However, with all their benefits (i.e. high uniformity and controllability of the chemical composition and deposition processes, doping possibilities, high reliability and reproducibility, etc.), the costly equipment that vacuum techniques require makes their implementation on an industrial scale problematic. This issue has triggered considerable research on solution processable metal oxide semiconductors.

The drawback of the solution processed materials is the need to remove solvent and precursor residues out of the semiconductor film and consolidate the metal oxide, which requires a large amount of energy normally supplied in the form of high annealing temperatures. Lowering the processing temperature is being addressed via different methods described above.

The chemical composition of the investigated systems is also a lot more varied. The availability of a wide spectrum of chemicals, which can be used as sources of the metal cations, offers more freedom to adjust the chemistry of the semiconductor formulations. Choosing the correct precursor-solvent(-stabilizer) ensemble demands considering the reactivity, solubility, chemical stability and ease of decomposition of the different components of the formulation. The roles of the individual cations in the active layer has often been discussed and in order to ensure the amorphous state of the material, systems with a minimum of 2 different cations are preferred.

Nevertheless, the results show that whenever pure In_2O_3 is used in the active layer, the performance of the TFTs is superior to the other multi-cation systems. Indium cations are connected via an edge-sharing network of (InO_6) octahedra in a crystal which minimizes the In-In interaction distance and allows them to form the CBM of the semiconductor; these

properties are also maintained in an amorphous state [61]. The charge carrier concentration and consequently the charge carrier mobility in indium oxide are dominated by oxygen vacancies [59], [61], whose amount can be controlled via the annealing temperature [112]. The amount of oxygen vacancies could also be influenced by designing a suitable In-containing precursor formulation for the solution-based process.

On the other hand, the application of multi-cation systems is favored because of several flaws inherent to indium oxide. The conversion of indium hydroxide, which is often formed when certain indium sources come into contact with different solvents, to indium oxide, takes place at temperatures above 300°C [17], [111], which would seem to place a limit on the lowest achievable processing temperature. High concentrations of indium oxide in TFTs have been shown to increase strongly the off-current of the transistor, shift the onset towards negative values and decrease bias stress stability [8], [48], [117], [118].

Electrically stable TFTs are crucial to implementation into the circuitry of real devices. The bias stress stability of metal oxide TFTs is a major topic of interest for both sputtered and solution processed systems. It is usually investigated in dependence on chemical composition of the active layer [119], [120], on deposition and annealing conditions [78], [121], on nature of the semiconductor-insulator interface [15], [74], on oxygen content in the film and surrounding atmosphere [78], [110], [122], and other factors. However, a systematic investigation of bias stress stability on morphological properties of the semiconductor film, such as layer thickness and roughness, is hard to come by. Some authors publish morphological data of the semiconductor layers and discuss them as a consequence of the variation of a certain process parameter [103], [123], but not as a cause of the observed TFT performance variation. Few authors investigate the thickness [124] and/or roughness [125] of the TFT's active layer as a main parameter influencing the performance of the TFTs. Yet these parameters deserve just as much attention because their influence on the TFT performance is far from trivial, especially in a solution based semiconductor.

These issues will be addressed systematically in the current work in an attempt to fabricate amorphous, low temperature solution processable indium oxide-based TFTs with high charge carrier mobility and good electrical stability.

4

Methods

4.1. Substrate structure

All TFTs used in this work were fabricated in a bottom gate – bottom contact configuration. A highly n-doped silicon wafer served as the device carrier and gate electrode. It was covered by a 230 nm thick thermally grown SiO_2 insulator layer. Then the source and drain electrodes consisting of 10 nm of ITO and 30 nm of gold were patterned via optical lithography.

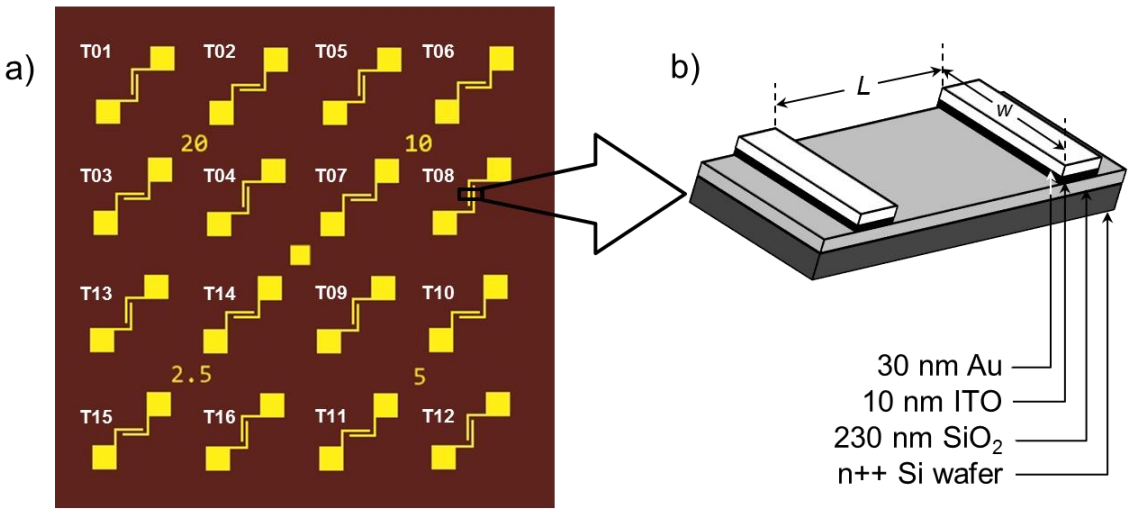

Figure 18. Schematic representation of the TFT substrate (a) and the detailed cross section through the channel of one TFT (b).

Figure 18 (a) illustrates the layout of the TFTs substrate having 16 transistors of varying channel length and relative position of the channel with respect to the center of the substrate. The numbers 20, 10 5 and 2.5 on the substrate indicate the channel length, in microns, of the respective 4 transistors around each of them. The channel width of all transistors was 2000 μm. The labels T01 – T16 next to each transistor are shown here to illustrate the unique name of each transistor, and were not present on the TFT substrate. Figure 18 (b) is a schematic illustration of the cross section through a TFT channel presenting

a detailed view of the structure of the TFTs. The alignment of the channels with respect to the center of the substrate was varied in order to account for its influence on TFT performance resulting from film morphology variation during spin coating.

4.2. Sample preparation

The TFT substrates were covered by a protective polymer layer which had to be removed before the substrate could be used. The cleaning procedure was composed of rinsing the samples with acetone in an ultrasonic bath at room temperature for 3 minutes. After this the samples were transferred into a bath containing a mixture of acetone and isopropanol of high purity. The bath was placed into the ultrasonic bath for 10 minutes at 80°C. After this step, the samples were transferred into DI-water. They were removed out of the water one by one, blown dry with a nitrogen gun and placed on a hot plate at 120°C for at least 30 seconds to dry any remaining water. Each sample was then exposed to a 10 min ozone cleaning step to increase the surface energy of the substrates, e.g. make them more hydrophilic, and to remove any organic residues left on the surface.

The semiconductor solutions were deposited onto the clean substrates via spin coating. The spin coating parameters varied in accordance with the properties of the formulations. The wet films were patterned via mechanical scribing [21] with a blunt object to avoid damaging the SiO_2 insulator. After spin coating the samples were placed on a hot plate at 350°C for one hour, unless stated otherwise. All film depositions and annealing steps were performed in a clean room with controlled ambient parameters, e.g. air humidity and temperature.

4.3. Formulation preparation

The ordered chemicals were used as delivered without any additional purification procedures. The precursors were normally dissolved in a given solvent at room temperature over a stirring plate to form a stock formulation of 0.5M cation concentration. The stock solution was then diluted further to obtain concentrations of interest. The formulations which were clear after fabrication were not filtered. The formulations which contained precursors with limited solubility were filtered through a 200 nm PA filter before use. Unless stated otherwise, the formulations were prepared and stored in ambient atmosphere.

When a percentage is used to describe the amount of an additive in a given solution, it usually describes an added amount, not a part of the total. For example when stating that 10% of zinc ions were added to an indium oxide solution, this means that the content of indium is regarded as 100% and an equivalent 10% amount of zinc is added to the solution, so that the content of indium in the final solution becomes 90.91% and the content of zinc is 9.09% respectively.

4.4. Electrical measurements

All electrical measurements of non-encapsulated TFTs were performed in a nitrogen atmosphere and in the dark, with a measurement setup consisting of a Keithley 2612 System Sourcemeter and a Keithley 3706-NFP Switch/Multimeter. Electrical and temperature stress measurements were performed in ambient atmosphere and the samples were encapsulated with the commercially available Solar Grade passivation via spin coating and annealing for 2 hours at 400°C in ambient atmosphere.

Transfer curves were measured at U_{ds} = 2 V and 10 V, varying the U_{gs} from -20 to 30 V and back in steps of 0.5 V. The output curves were measured at U_{gs} = 0 to 15 V in steps of 5 V and by varying the U_{ds} from -2 to 15 V and back in steps of 0.2 V.

4.4.1. Negative/Positive Bias Temperature Stress measurements

During the tress measurements the applied gate bias had an absolute value of 20 V and its sign was determined by the name of the test, i.e. -20 V for NBTS and +20 V for PBTS. In both stress conditions a drain-source voltage of +5 V was applied to the measured TFTs. At certain time intervals the stressing was shortly interrupted and the transfer characteristics of the TFTs under investigation were measured after which the stressing was resumed. During the entire stress measurement the samples were kept in darkness, in an enclosure containing ambient air at a temperature of 60°C.

4.5. Temperature measurements

The dependence of the TFT performance on temperature was measured with two different setups for reasons that will be explained below.

4.5.1. Measurements below room temperature

A liquid nitrogen cooled cryostat was used in the below room temperature region since lowering the temperature of the substrate in air caused condensation of water on the substrate which influenced negatively electrical measurements. The dry nitrogen atmosphere in the cryostat chamber circumvented that problem. The measurement range of the cryostat allows measurements between ~ -196°C and 450°C. The gate, source and drain electrodes of the TFTs were connected via a tailor made sample holder to the measurement setup and lowered into the cryostat cylinder. The cylinder was filled with nitrogen and cooled down to -163°C. When the desired temperature was achieved, the sample was given 5 minutes to reach thermal equilibrium with the surrounding atmosphere, and then the electrical measurement was commenced. The temperature was increased in steps of 15 degrees and the above described procedure was performed at each temperature. After reaching the maximum allowed temperature, the electrical performance was measured further by decreasing the temperature in steps of 15 degrees in order to investigate the hysteresis of the figures of merit vs. temperature curves. Unfortunately, the material of the sample holder and the insulation of the connecting cables inside the chamber did not allow increasing the temperature above 110°C-120°C. Therefore for higher temperatures a different setup was necessary.

4.5.2. Measurements above room temperature

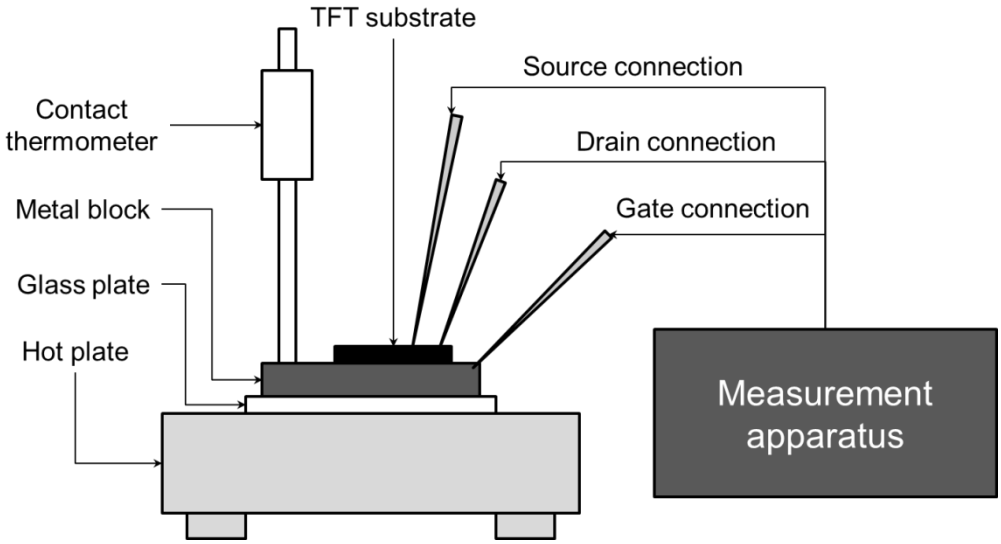

Figure 19. Schematic representation of the measurement setup used in the temperature region above room temperature.

The alternative measurement setup was realized with the help of a hot plate. The metallic surface of the hot plate was first isolated by placing on it a thin glass plate. On top of the glass plate was placed a metal block to serve as the gate connector. The block was connected with the needle of the probe station to the measurement apparatus. The sample to be measured was placed on the metal block and its source and drain electrodes were connected with another 2 probe station needles to the measurement apparatus. The temperature of the metal block's surface (gate temperature) was measured with a contact thermometer (Figure 19). The measurements were initiated at room temperature and performed after each increase of 7 degrees with the methodology described in section 4.5.1.

4.6. Film thickness and roughness measurements

The thickness of the spin coated films was varied by means of formulation concentration and spin coating speed. For most of the TFTs, the thickness of the spin coated films was measured mechanically, using a Nanosurf Atomic Force Microscope (AFM). The edge of the scratch formed during TFT patterning was imaged with the AFM (Figure 20 (a)). The software of the AFM permits extracting the cross sectional height profile of the given image, an example of which is shown in Figure 20 (b). For every film 5 such profiles were measured and the thickness of the film was taken as the average of the resulting values.

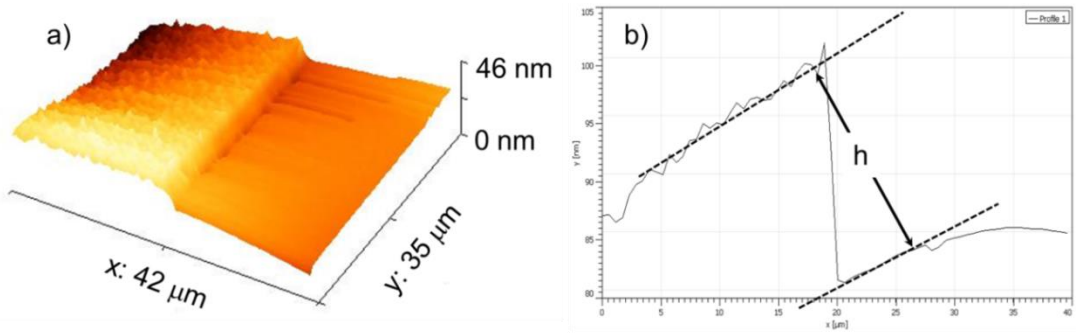

Figure 20.The edge of a semiconductor film imaged with an AFM (a) and the extracted with the AFM software height profile of the step (b).

The roughness of each film was measured by taking a 5x5 µm AFM image of the film surface and in order to compare all images and exclude spin coating artifacts, all images were taken in the same position marked in Figure 21 a). The surface roughness of the films was calculated with the built-in function of the AFM's software according to the following equation:

$$S_{rms} = \sqrt{\frac{1}{MN}\sum_{k=0}^{M-1}\sum_{l=0}^{N-1}\left[z(x_k, y_l)\right]^2} \tag{37}$$

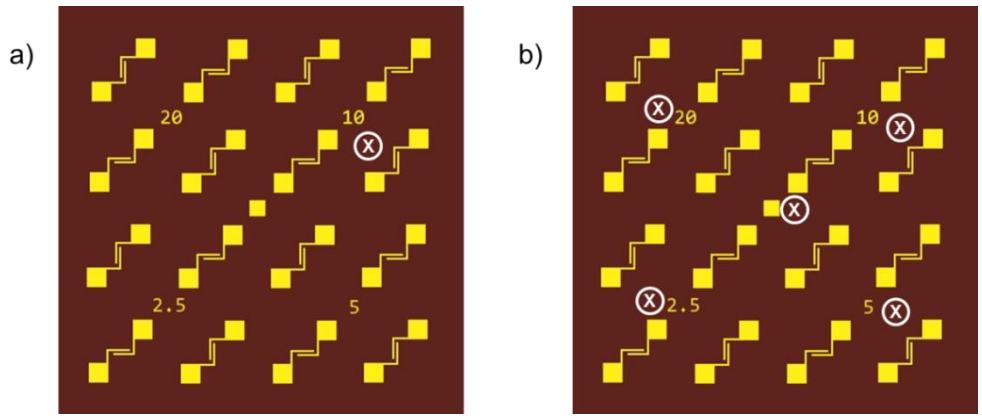

Figure 21. Measurement positions for the film surface roughness with an AFM (a) and surface thickness via ellipsometry (b).

Not every formulation though allowed the application of the mechanical method for film thickness measurements. The fluidity of some formulations prevented achieving a clear scratch edge during mechanical scribing. In such cases the film thickness was measured optically, with an ellipsometer. The measurements were carried out at 5 positions on the substrate (marked in Figure 21 b) and the obtained values were averaged.

A measurement performed on the same set of samples proved that both methods give essentially the same results (Figure 22).

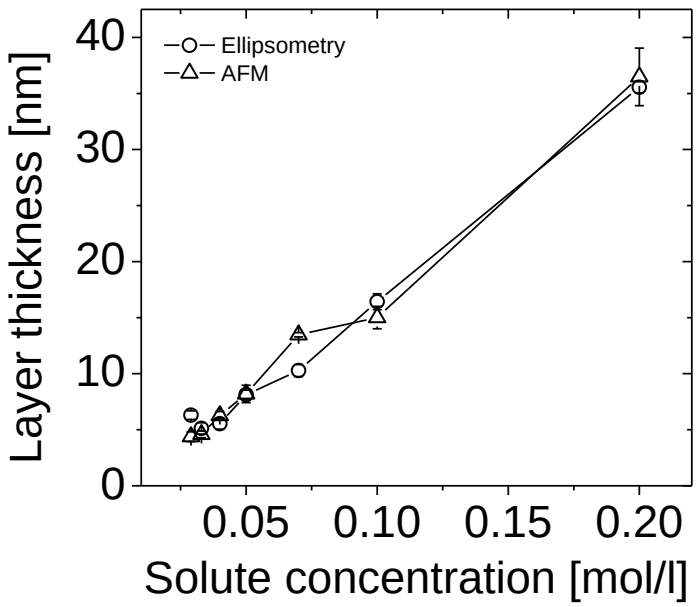

Figure 22. Comparison of the optical and mechanical methods for measuring film thickness.

5

Results

The scientific literature reports on a large variety of semiconductor formulations with a wide spread of performance indicators (see Chapter 3). A formulation is normally prepared by dissolving cation source(s) in a solvent and adding a stabilizing agent if needed. As cation sources most often are mentioned halides [49], [96], [109], acetates [62], [105], , nitrates [17], [98], [100], [103], [106], [107], [108], [112], [113], [120], [126], alkoxides [21], acetylacetonates [111] etc. On the part of the solvent and stabilizer there is not much variation. Usually 2-methoxyethanol and ethanolamine are used respectively. Sometimes a mixture of acetonitrile and ethylene glycol was also used as a solvent [20]. Due to the toxicity of 2-methoxyethanol, it was decided to replace it with a most similar solvent possible. Banger *et al.* dissolved the indium alkoxide complex in methoxyisopropanol (1-methoxy-2-propanol) [21], which is not only similar to 2-methoxyethanol chemically, but it has a similar boiling point as well and is not deemed toxic. The use of any stabilizers was avoided in order not to introduce unnecessary contaminants into the semiconductor formulation.

5.1. Indium source selection

5.1.1. Indium chloride

0.5682 g of $InCl_3$ were dissolved in 5.5 ml of methoxyisopropanol for a concentration of indium ions of 0.5 M. The solution was stirred for 24 h at room temperature. Since not all of the starting material dissolved, the solution was filtered through a 200 nm PA filter. The clear solution was used to prepare a dilution series, where 1 part formulation was dissolved in x parts of its own solvent, with x varying from 0 to 6. Because some amount of starting material was filtered away, it is not possible to talk about the concentration of the material in the formulation; therefore different formulations will be differentiated according to their

dilution factor. TFTs were prepared by spin coating each solution at 3000 rpm for 30 seconds and then annealing the samples for 1 h at 350°C (for more details on TFT fabrication see Chapter 4).

The prepared TFTs were measured electrically and the resulting transfer curves of the best four of these samples are shown in Figure 23 below. Displayed are both the forward and backward sweeps to illustrate the measurement hysteresis. The maximum mobility was less than 0.2 cm^2/Vs, obtained with the 1:3 dilution.

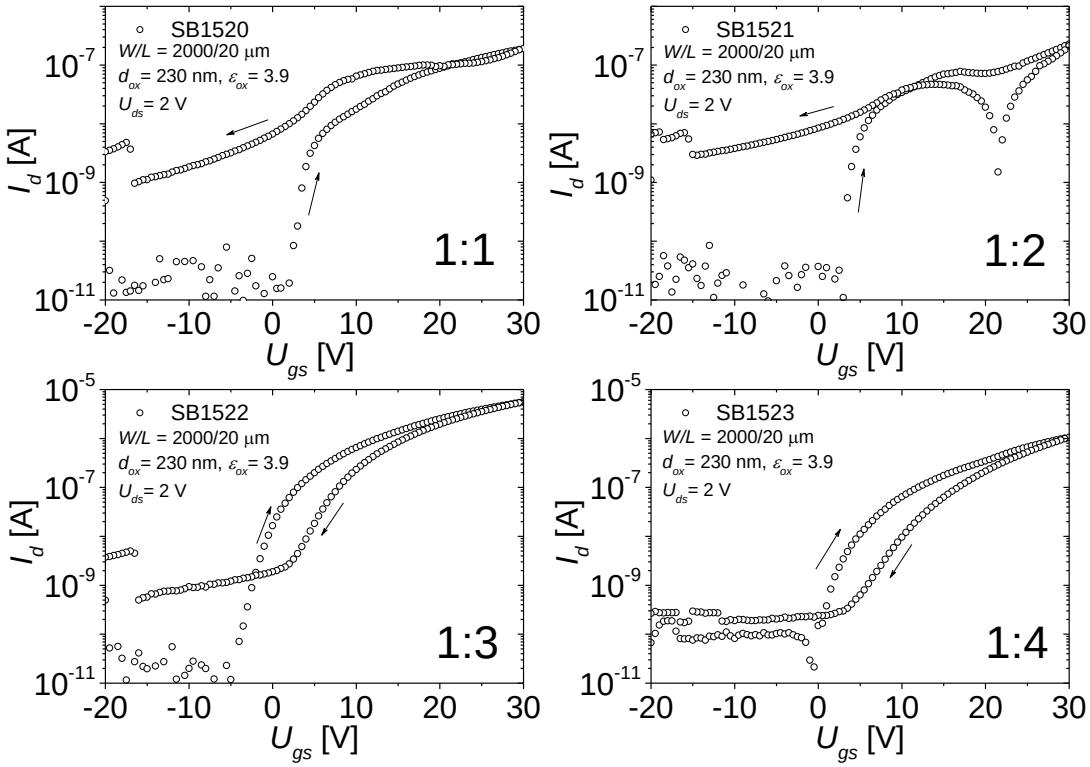

Figure 23. Transfer curves of 4 samples prepared with different concentrations of $InCl_3$ in methoxyisopropanol. Each dilution factor of the original formulation is indicated on the respective graph.

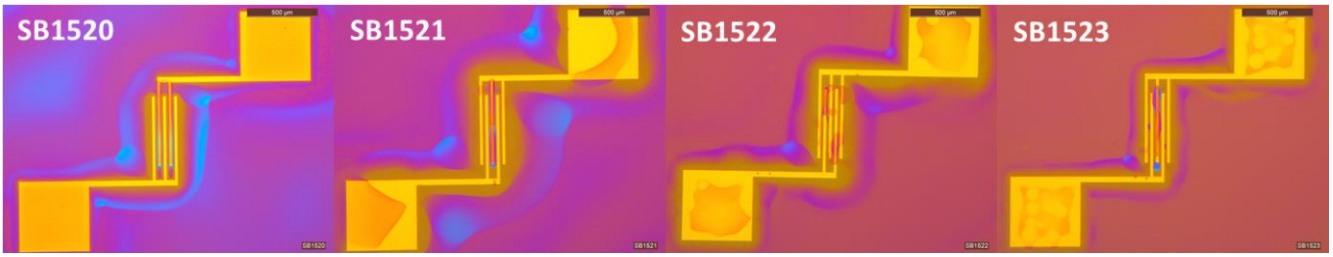

Figure 24. Microscope images of the $InCl_3$-based TFTs.

The most critical reason for such a low performance was the fact that the spin coated films were of a very poor quality, as can be seen in Figure 24.

Figure 24 shows the microscope images of the measured TFTs. One can see that the films appear uniform, without any visible defects, but are strongly damaged around the channel of the TFTs, where their uniformity is most important.

The bad quality of the film around the contacts of the TFT does not leave room for interpretation of the influence of other factors (material choice, annealing temperature, etc.) on the performance of the device. Measuring the thickness of the films in this case becomes irrelevant, due to the visible difference between the bulk film and the film within the channel of the TFT. This results also in a strong morphological difference between the bulk and channel films. Figure 25 shows the surface of the films in the 2 regions for the TFT fabricated with the 1:1 diluted semiconductor formulation, e.g. the thicker film.

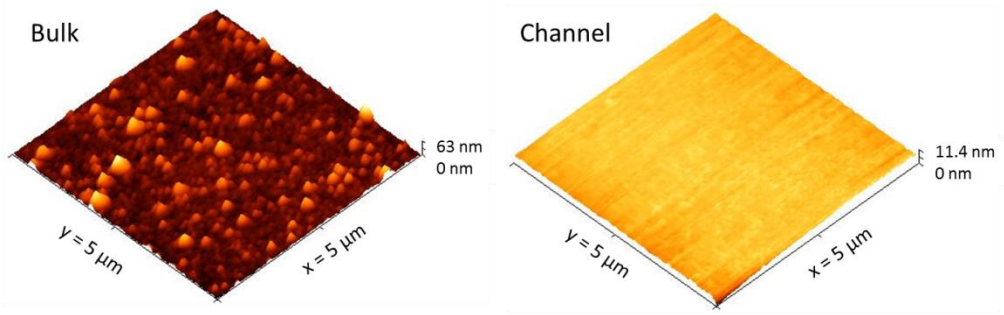

Figure 25. AFM image of the surface of the spin coated film of sample SB1520 away from and between the source/drain contacts. The z-axis indicates the height difference between the highest and lowest measured z-values.

It appears that a thick film has a very grainy structure, while inside the channel where the film is thinner, the formation of these grains is suppressed, and the surface of the film is smoother. The root mean square roughness of the bulk film is 6.22 nm, while inside the channel it is only 0.59 nm. As the dilution factor of the formulation increases, the thickness of the films decreases and their morphology changes and becomes smoother. Already the next dilution factor (1:2) results in films with a comparable roughness of the films in both measurement regions. This however does not improve the performance of the TFTs.

In addition to the morphological issue, some authors report that chlorides are generally a problematic source of cations because the chloride ions are reluctant to leave the films and require very large processing temperatures [127]. If they remain in the TFTs active layer, they behave as mobile ions and influence negatively the transport, their accumulation being especially severe at lower annealing temperatures [62], therefore using chlorides as an indium source will not allow lowering the processing temperature.

5.1.2. Indium acetate

An alternative source of indium mentioned in literature is indium acetate [62], [105]. Gómez *et al.* reported on testing indium acetate, nitrate and sulfate as indium sources to dope ZnO films deposited via spray pyrolysis [62]. They achieved best performance with the indium acetate and worst with sulfate dopants, however, at temperatures above 450°C. The high temperature is not surprising though. The acetate anion also requires very high temperatures to decompose [111], [127]. In addition to that, metal acetates tend to form insulating metal carbonates at temperatures below 400°C, which convert to oxycarbonates above 400°C and eventually to metal oxides at much higher temperatures [128]. One could dismiss this study as evidence for necessary high processing temperature because it was performed on solid salts of rare earth metals, therefore it had nothing to do with a solution system.

Fukui and Iwasawa studied the acetate ions adsorbed on a TiO_2 surface [129]. They mentioned that at temperatures above 520 K, e.g. above 250°C, the acetate ions decompose releasing ketene or acetone molecules, leaving behind either hydroxyl groups or carbonate groups, which are both equally detrimental for the performance of an indium based semiconductor, since $In(OH)_3$ inhibits semiconductor behavior and also requires high temperatures to decompose into the respective oxide [17], [111].

Finally, Choi *et al.* present results of a TGA analysis of an IZO film and state that the weight loss at 350°C corresponds to the decomposition of indium acetate [105].

An attempt to fabricate an indium acetate formulation in methoxyisopropanol was not successful. Firstly, the solubility of indium acetate in the said solvent was very low. Even after several days of stirring, not much of the starting material had gone into the solution. The formulation was filtered through a 200 nm PA filter. The resulting clear solution was then used to prepare a dilution series like in 5.1.1. and TFTs were prepared by spin coating the solutions at 3000 rpm for 30 seconds. Already after spin coating it was observed that the films were extremely thin even for the most concentrated solution. The samples were annealed at 350°C for one hour but were inactive when measured electrically afterwards. This shows that indium acetate is not a proper candidate for the intended semiconductor formulation.

5.1.3. Indium acetylacetonate

Hwang *et al.* proposed indium acetylacetonate as an alternative to indium acetate [111], arguing that it has a better solubility, requires lower decomposition temperatures and no stabilizers.

2.0607 g of indium acetylacetonate were dissolved in 10 ml of methoxyisopropanol for an intended 0.5 M solution. The solution was stirred for 1 week at room temperature. Although somewhat better than indium acetate's, its solubility was still rather low. The formulation was filtered through a 200 nm PA filter and resulted in a clear, slightly yellowish solution. A dilution series was prepared and the solutions were spin coated at 3000 rpm for 30 seconds onto the Si/SiO_2 substrates and annealed for 1 h at 350°C.

The results of the electrical measurements are summarized in Figure 26 below:

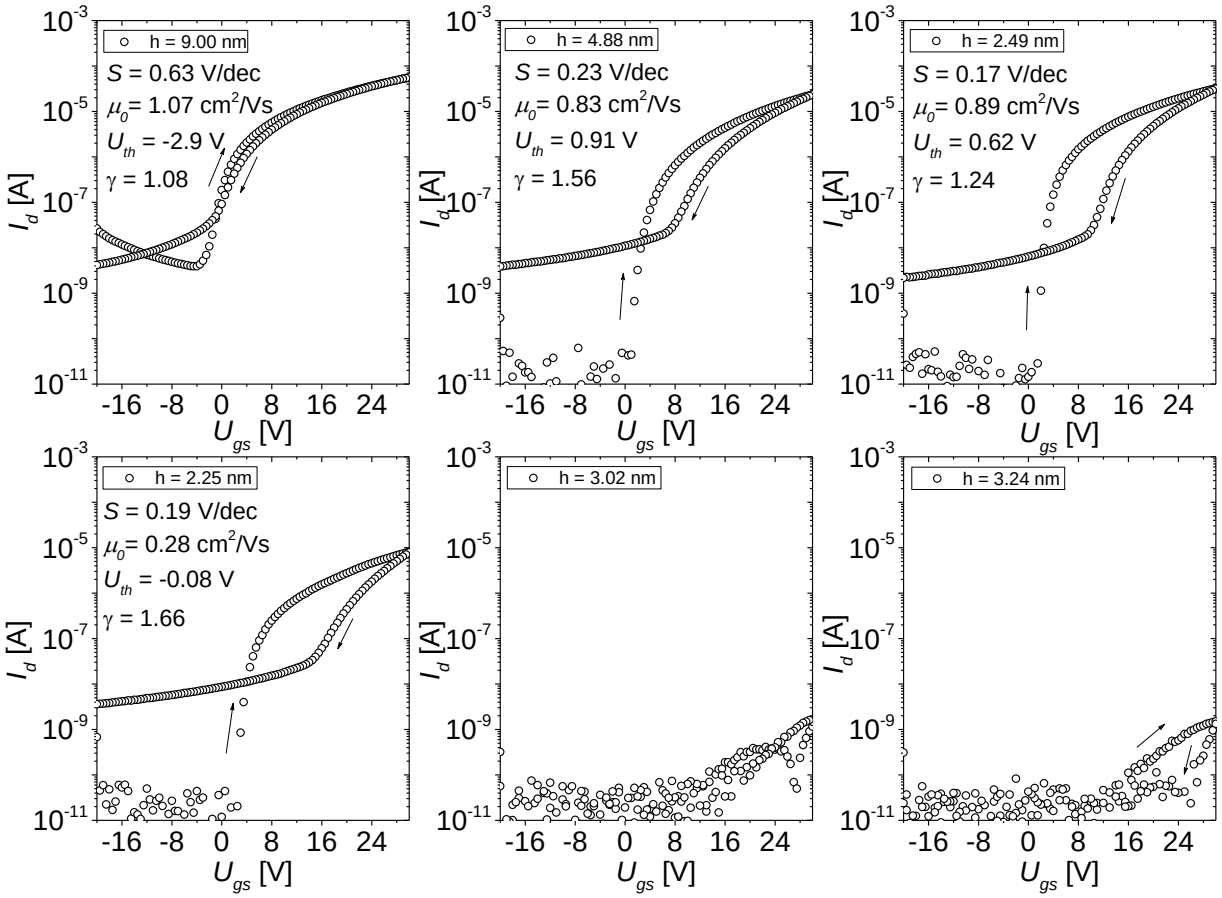

Figure 26. Transfer characteristics of TFTs prepared with the indium acetylacetonate dilution series. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 mm, d_{ox}= 230 nm, ε_{ox}= 3.9.

The corresponding morphological information was collected with the AFM and the thickness measurements were conducted with the ellipsometer. The respective data is collected in Table 5, together with the figures of merit extracted from the electrical measurements.

Table 5. Morphological and electrical performance data of the TFTs fabricated with the indium acetylacetonate in methoxyisopropanol dilution series.

Dilution	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
1:0	9.00 ± 0.02	0.83	1.07	-2.9	1.08	0.63
1:1	4.88 ± 0.04	0.78	0.83	0.91	1.56	0.23
1:2	2.49 ± 0.17	0.85	0.89	0.62	1.24	0.17
1:3	2.25 ± 0.18	0.74	0.28	-0.08	1.66	0.19
1:4	3.02 ± 0.06	0.64	very weak field effect			
1:5	3.24 ± 0.02	0.60				

Out of the fabricated TFTs, the one with the thickest active layer had the highest mobility, but rather large off current and subthreshold slope. Beginning with the next sample already a strong decrease in layer thickness is observed, which is also reflected in a decreasing mobility. The increasing γ signals an increase in energetic disorder and density of trap states. The last statement however appears to contradict the observed improvement in subthreshold slope. One should keep in mind that γ holds information about interface traps as well as bulk traps, while the subthreshold slope is influenced by the semiconductor-insulator interface. As the film thickness decreases and becomes comparable to the surface roughness, the morphological defects create discontinuities in the film, which leads to a decrease in the mean free path of the electrons, e.g. decrease in mobility, and an increase in γ. This does not necessarily mean an increase in the interfacial trap density. The improvement in subthreshold slope could be triggered by the fact that as the films get thinner, it takes less time and effort to accumulate the charge at the semiconductor-insulator interface and open a conductive channel.

Like in the case of $InCl_3$, the thicker films were found to have a grainy structure, which disappeared as the films got thinner, although they were not as rough as the $InCl_3$-based films. The formation of these grains could be the result of either the film thickness or the concentration of the formulation. Since the two are strongly interrelated, using dilution series to resolve this issue is inappropriate. However, taking one solution of a given concentration and spin coating it at different speeds would result in different film thickness

at the same concentration of the formulation. Figure 27 illustrates the result of this experiment.

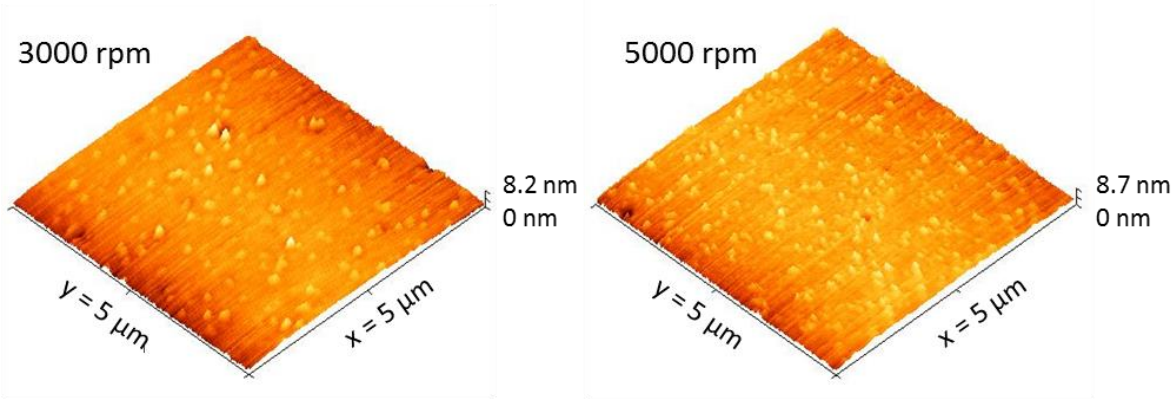

Figure 27. Surface morphology of 2 films deposited from the same solution but at different spin coating speeds.

As Figure 27 shows, the film deposited at a higher spin coating speed, having a thickness of (7.32 ± 0.04) nm and S_{rms} = 0.87 nm, has more but smaller grains and less observable defects on the surface than the sample spun at a lower rate and having a thickness of (9.00 ± 0.02) nm and a lower roughness of S_{rms} = 0.83 nm. That is also reflected in the worse performance of the TFT fabricated with the thinner layer U_{th} = -3.85 V, γ = 1.31 and S = 1.33 V/dec. Considering the possibly higher number of grain boundaries, it was unexpected that the mobility of the thinner samples is larger, e.g. μ_0 = 1.29 cm²/Vs. Since both samples were prepared with the same formulation, it can be assumed that the formation of the grains is a result of film thickness and can be controlled by its adjustment.

The overall low performance of the indium acetylacetonate formulation requires that other cation sources be investigated.

5.1.4. Indium isopropoxide

Banger *et al.* introduced the use of metal alkoxides as cation sources claiming that these compounds are highly reactive and therefore suitable candidates to lower the processing temperature of metal oxide TFTs [21]. They prepared the formulations and spin coated the TFTs inside a glove box due to the reactivity of the alkoxides with the water molecules out of the ambient atmosphere. The prepared TFTs were then annealed in air to promote the hydrolysis of the solute in the thin films and the formation of the M-O-M bonds.

In this work the semiconductor formulation was prepared in the glove box by dissolving 0.7450 g of indium isopropoxide in 6 ml of methoxyisopropanol, corresponding to a 0.425 M solution. The solution was stirred for 24 h at room temperature and filtered through a 200 nm PA filter because not all of the starting material had dissolved. Unlike reported in [21], the TFTs were processed and annealed in ambient air. The transfer characteristics and extracted figures of merit are presented in Figure 28 as a function of film thickness and the morphological information collected with the AFM is summarized in Figure 29.

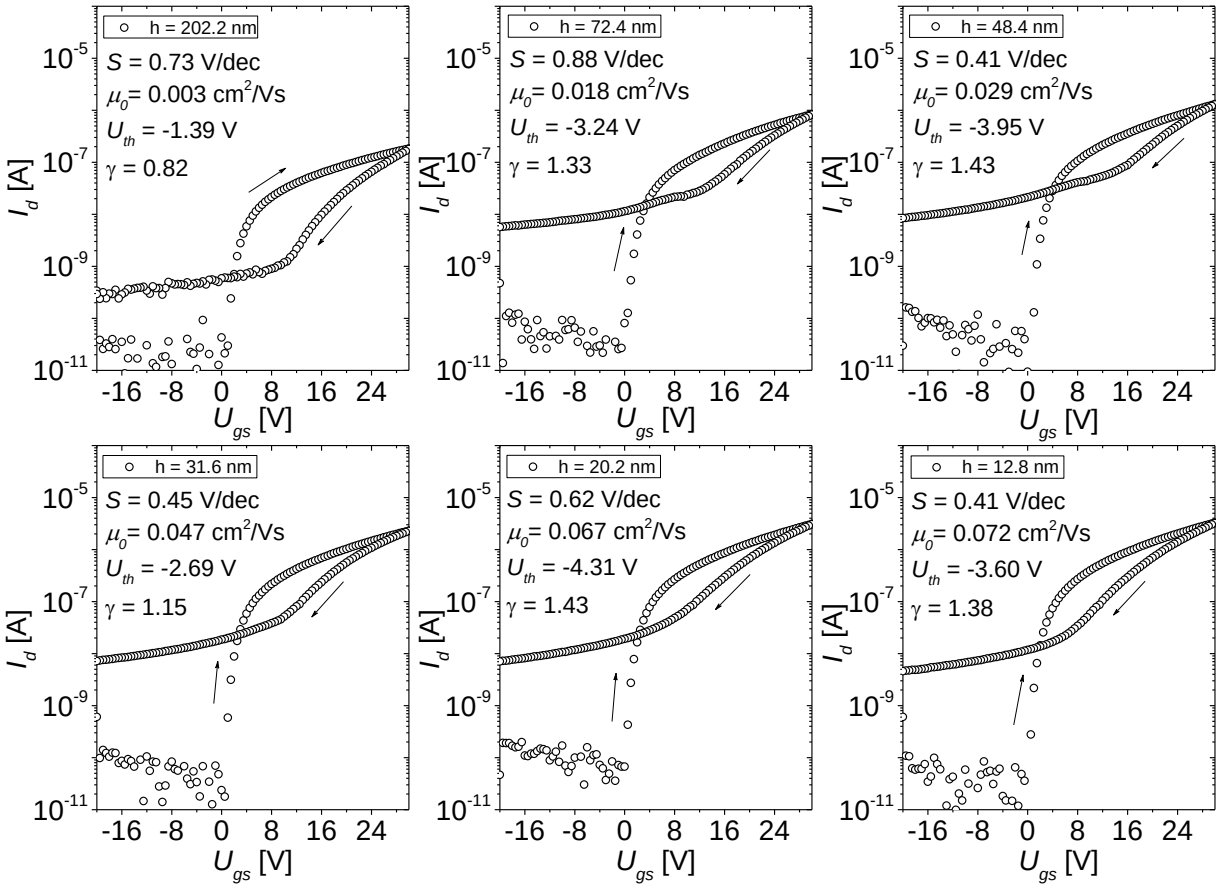

Figure 28. Transfer characteristics of TFTs prepared with the indium isopropoxide dilution series from the 0.425 M stock solution. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 μm, d_{ox}= 230 nm, ε_{ox}= 3.9.

The data presented in Figure 28 shows that the TFTs fabricated with the indium isopropoxide solutions have an utterly low performance. Although the forward transfer curve has a very good subthreshold slope for every TFT, the curve measured in the backward sweep displays a very large subthreshold slope and off current. The reason for this behavior can be seen in Figure 29. In addition to being very thick, the films have a very grainy structure. It is plausible that during the forward sweep of the gate bias the grain boundaries become negatively charged, which hinders the overall transport. In the backward sweep

these charged grain boundaries act as scattering centers resulting in a drop of the on current, shift of the onset to the right and inability to completely deplete the conductive channels and switch the transistor off.

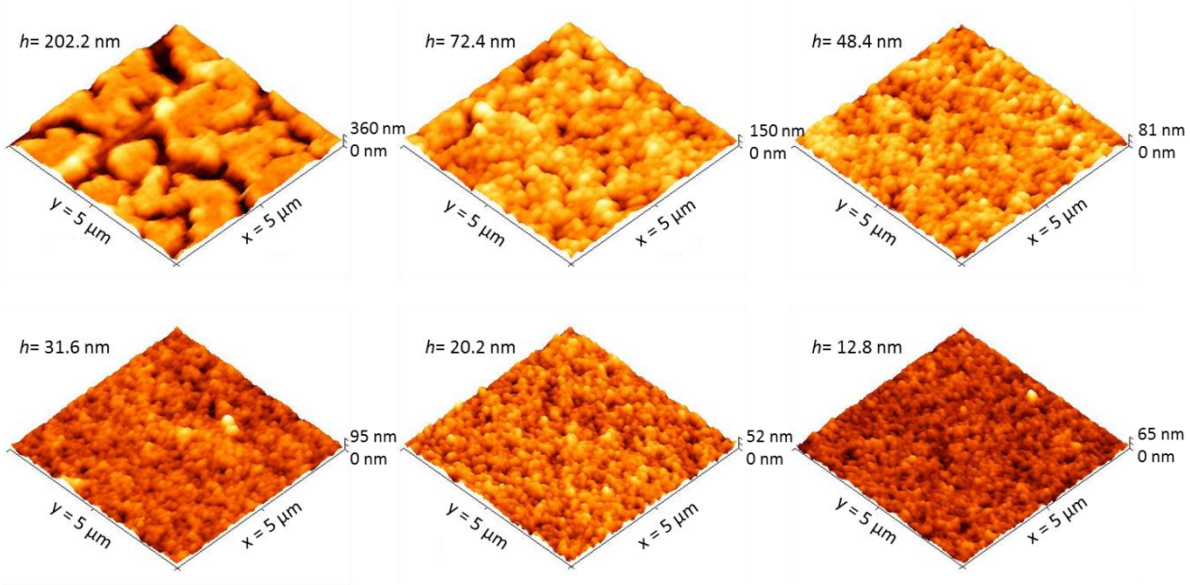

Figure 29. Surface morphology as a function of film thickness for thin films spin coated from indium isopropoxide in methoxyisopropanol formulations.

Table 6. Morphological and electrical performance data of the TFTs fabricated with the indium isopropoxide in methoxyisopropanol dilution series prepared from the 0.425 M stock solution.

Dilution	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
1:0	202.2 ± 10.3	62.8	0.003	-1.39	0.82	0.73
1:1	72.4 ± 2.5	18.9	0.018	-3.24	1.33	0.88
1:2	48.4 ± 2.2	10.3	0.029	-3.95	1.43	0.41
1:3	31.6 ± 1.4	9.3	0.047	-2.69	1.15	0.45
1:4	20.2 ± 1.6	6.4	0.067	-4.31	1.43	0.62
1:5	12.8 ± 1.6	5.4	0.072	-3.60	1.38	0.41

As it was shown earlier, the size of the grains and their presence can be influenced by the film thickness, therefore a new formulation was prepared with a starting concentration of 0.073 M by dissolving 0.2141 g of indium isopropoxide in 10 ml of methoxyisopropanol, which is similar to the 1:5 dilution of the previous formulation. The solution was stirred for 24 h at room temperature and filtered through a 200 nm PA filter. A dilution series was prepared and used to fabricate TFTs as described above. The transfer characteristics and extracted figures of merit are presented in Figure 30 as a function of film thickness and the morphological information collected with the AFM is summarized in Figure 31.

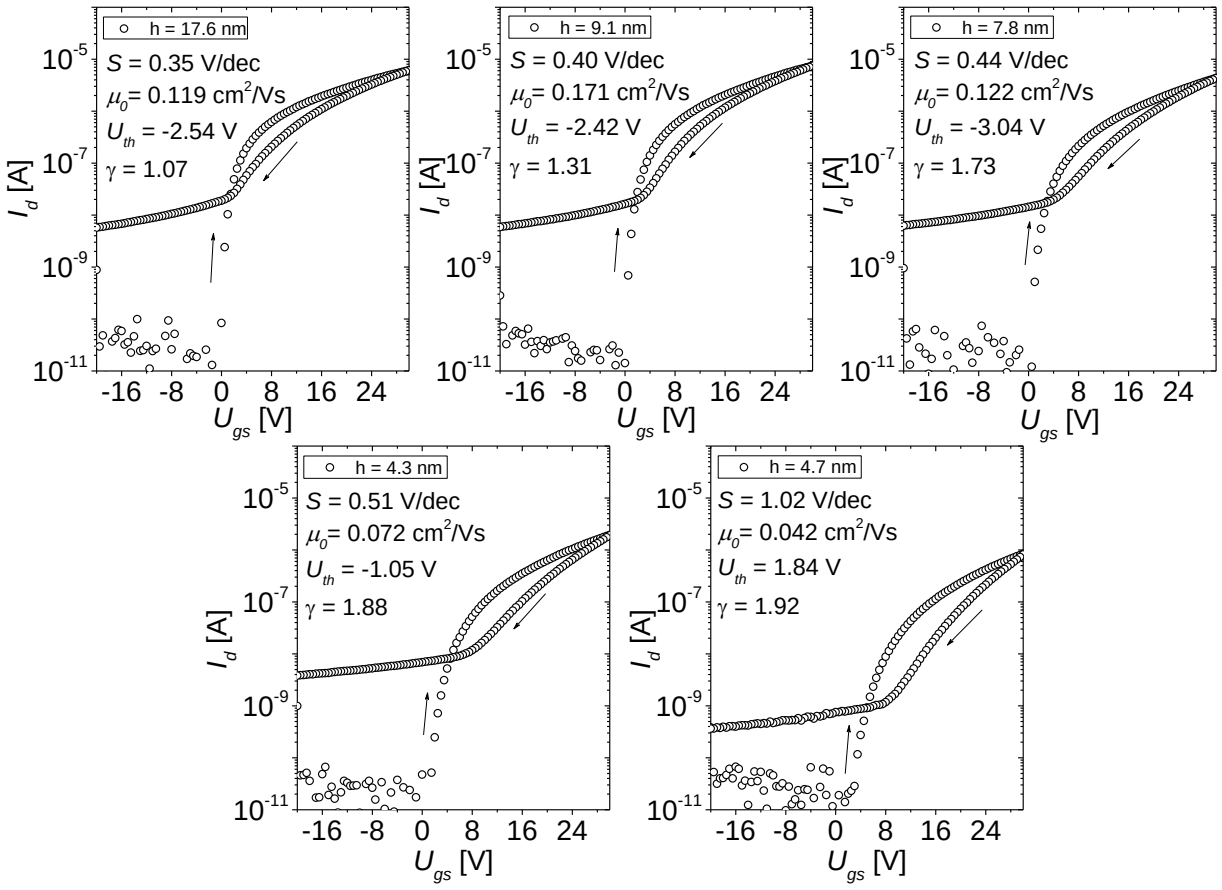

Figure 30. Transfer characteristics of TFTs prepared with the indium isopropoxide dilution series prepared from the 0.073 M stock solution. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 μm, d_{ox}= 230 nm, ε_{ox}= 3.9.

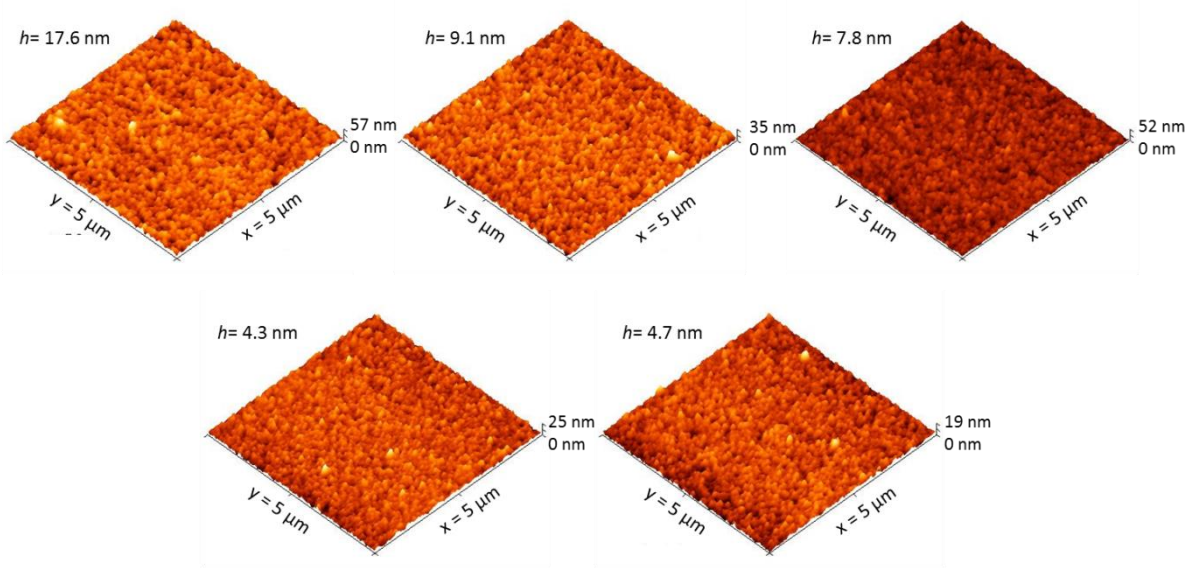

Figure 31. Surface morphology as a function of film thickness for thin films spin coated from the indium isopropoxide in methoxyisopropanol formulations prepared from the 0.073 M stock solution.

The performance of the thinner films was much better than that of the thicker ones, which can be attributed to the improved film morphology (Figure 31 and Table 7).

Table 7. Morphological and electrical performance data of the TFTs fabricated with the indium isopropoxide in methoxyisopropanol dilution series prepared from the 0.073 M stock solution.

Dilution	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
1:0	17.6 ± 0.8	5.8	0.119	-2.54	1.07	0.35
1:0.5	9.1 ± 0.3	3.5	0.171	-2.42	1.31	0.40
1:1	7.8 ± 0.2	3.0	0.122	-3.04	1.73	0.44
1:2	4.4 ± 0.4	2.2	0.072	-1.05	1.88	0.51
1:3	4.7 ± 0.2	1.9	0.042	1.92	1.92	1.02

In addition, the film thickness is now in a range where the results can be compared with the ones obtained from TFTs fabricated with the other cation sources. Even though the performance of the TFTs improved compared with the thicker indium isopropoxide-based films, it remains significantly lower than even that of the transistors fabricated with the $InCl_3$ formulations. The reason for the low overall performance could be that the TFTs were processed in ambient atmosphere, not in a glove box, like described in the work of Banger *et al.* [21]. Since the goal of this work is to develop a semiconductor material that can be processed in ambient atmosphere, this material can be dismissed from the list of candidates for such a formulation.

5.1.5. Indium oxoalkoxide

Evonik Industries AG has developed a novel indium-based precursor for solution processable electronics. The material is an indium oxoalkoxide. Considering the poor processability in ambient atmosphere and its low overall performance of indium isopropoxide, it is hard to imagine the advantage this new material has to offer.

The main difference of this material to an alkoxide is that its molecule already contains an In-O-In bond, which should dramatically lower the needed input energy to consolidate the metal oxide layer by forming additional indium-oxygen bonds.

A formulation was prepared by dissolving 1.03 g of the precursor in 17.6 ml of methoxyisopropanol in a glove box, stirring the solution for 24 h at room temperature and filtering it in the end through a 200 nm PA filter. This resulted in a clear, bright orange formulation. A dilution series was prepared as with other materials described above and used to fabricate TFTs in ambient atmosphere. The measured transfer characteristics and extracted figures of merit are presented in Figure 32 as a function of film thickness and the morphological information collected with the AFM is summarized in Figure 33.

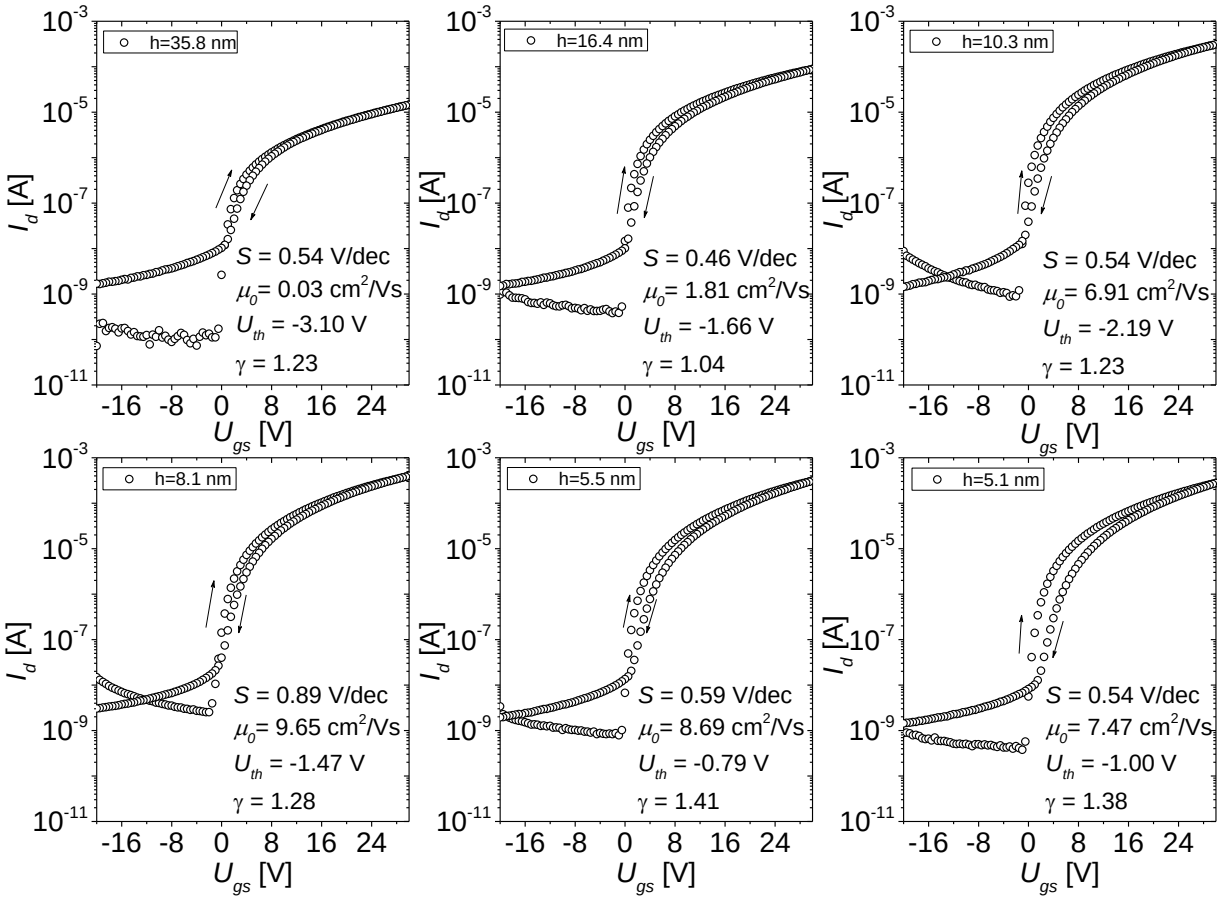

Figure 32. Transfer characteristics of TFTs prepared with the indium oxoalkoxide dilution series. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 μm, d_{ox}= 230 nm, ε_{ox}= 3.9.

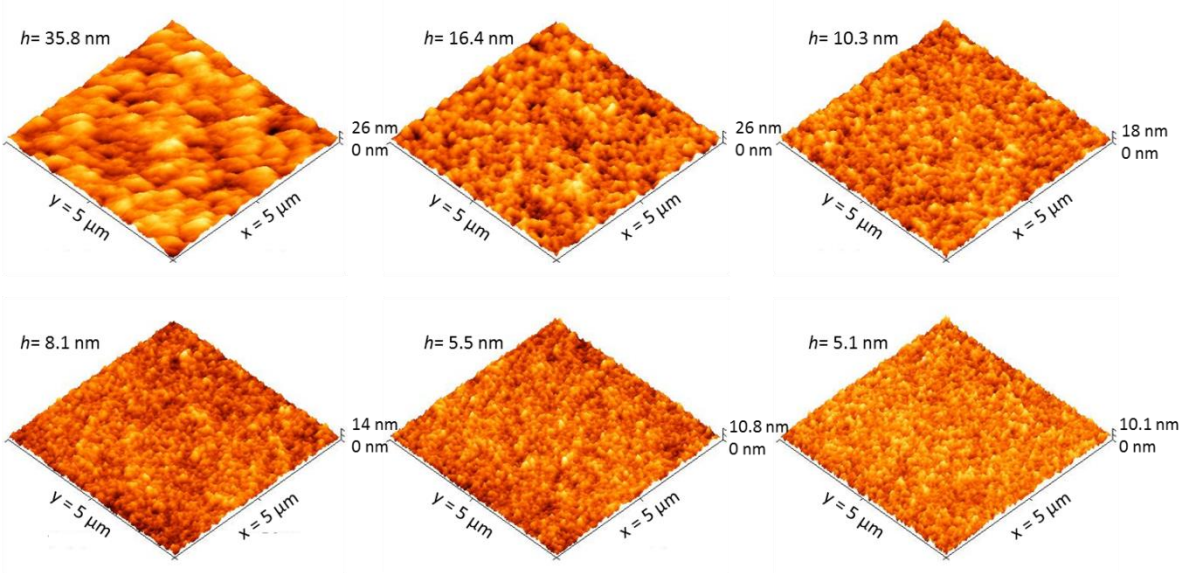

Figure 33. Surface morphology as a function of film thickness for thin films spin coated from indium oxoalkoxide in methoxyisopropanol formulations.

Table 8 summarizes the electrical performance data and the film morphology results for an easier analysis and comparison.

Table 8. Morphological and electrical performance data of the TFTs fabricated with the indium oxoalkoxide in methoxyisopropanol dilution series.

Dilution	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
1:0	35.8 ± 0.5	3.24	0.03	-3.10	1.23	0.54
1:1	16.4 ± 0.7	3.20	1.81	-1.66	1.04	0.46
1:2	10.3 ± 0.5	2.07	6.91	-2.19	1.23	0.54
1:3	8.1 ± 0.4	1.56	9.65	-1.47	1.28	0.89
1:4	5.5 ± 0.5	1.28	8.69	-0.79	1.41	0.59
1:5	5.1 ± 0.5	1.20	7.47	-1.00	1.38	0.54

The morphology of the resulting films is similar to the indium isopropoxide solutions, the difference being the surface roughness, which is lower for the oxoalkoxide TFTs even though a grainy structure is characteristic for both types of material (Figure 33). Nevertheless the semiconductor from Evonik Industries AG achieved a staggering mobility of almost 10 cm²/Vs for films below 10 nm thickness (Table 8) and processed at only 350°C. The TFTs based on this material also have a good subthreshold slope and slightly negative threshold voltage and the lowest hysteresis among the tested materials so far. The high off current however is something which needs to be improved for this material to have a chance to be considered for electronic devices, which should be achievable with an appropriate structuring method for the semiconductor, such as wet etching for example.

5.1.6. Indium nitrate hydrate

Indium nitrate hydrate is by far the most often mentioned cation source in the scientific literature on solution processable indium-based TFTs. Among its advantages are its high solubility in almost any organic solvent and low decomposition temperature (250°C) of the anion compared to other compounds [127]. The nitrate anion also proves useful to drive combustion processes [112], circumventing the need to introduce additional nitrate sources into the semiconductor formulation which might have an adverse effect on the TFT performance, especially at low temperature where it might not be high enough to evaporate the additive residues out of the thin films.

The semiconductor formulation was prepared by dissolving 1.91 g of $In(NO_3)_3 \cdot H_2O$ in 12 ml of methoxyisopropanol. The solution was stirred for 1 hour and was completely clear, therefore was used without being filtered. A dilution series was prepared and used to fabricate TFTs as described above. The measured transfer characteristics and extracted

figures of merit are presented in Figure 34 as a function of film thickness and the morphological information collected with the AFM is summarized in Figure 35.

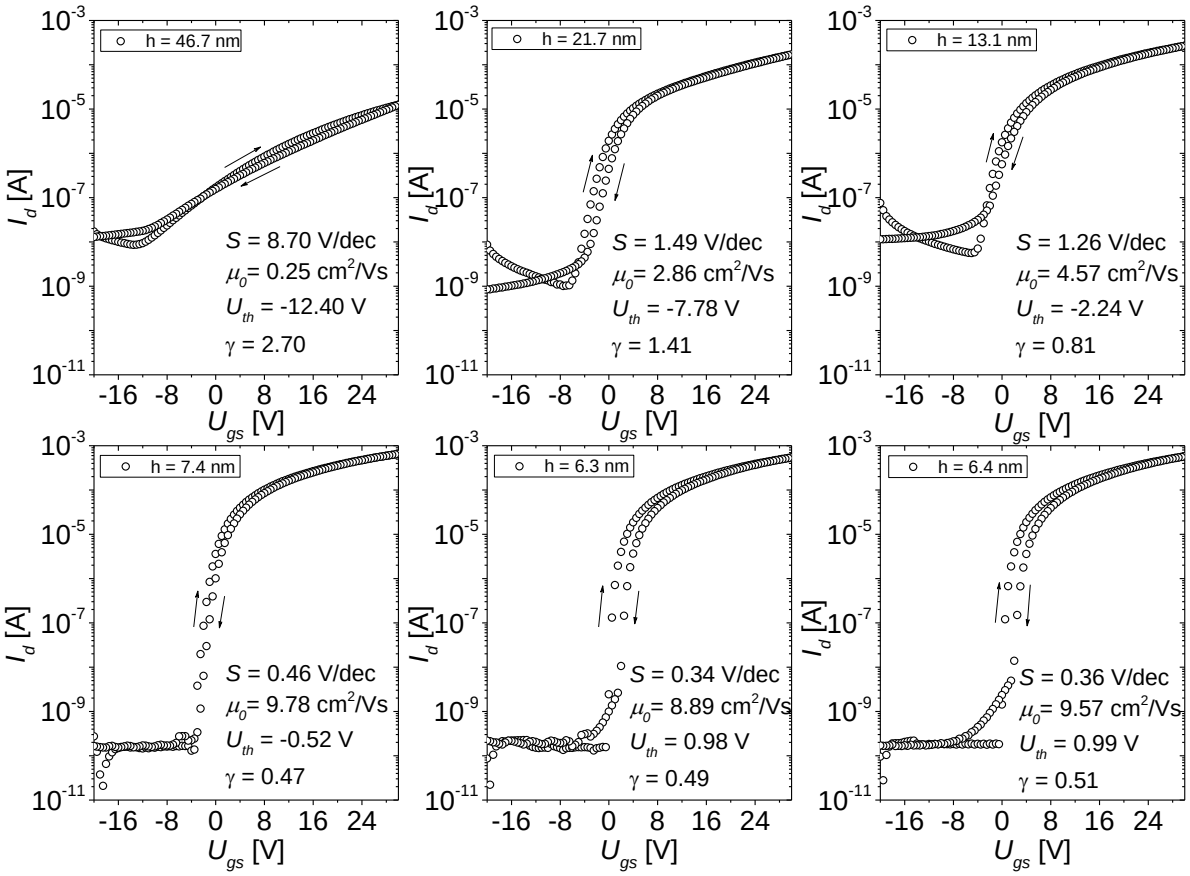

Figure 34. Transfer characteristics of TFTs prepared with the $In(NO_3)_3 \cdot H_2O$ dilution series. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 µm, d_{ox}= 230 nm, ε_{ox}= 3.9.

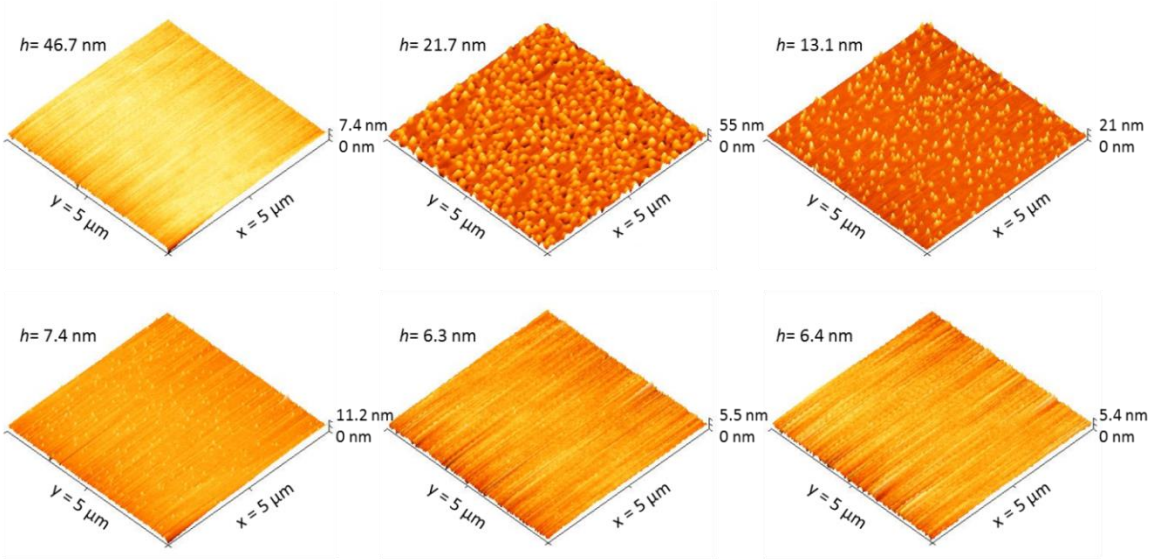

Figure 35. Surface morphology as a function of film thickness for thin films spin coated from $In(NO_3)_3 \cdot H_2O$ in methoxyisopropanol formulations.

The extracted parameters from the electrical and AFM measurements are collected in Table 9 for ease of analysis and comparison.

Table 9. Morphological and electrical parameters of the TFTs fabricated with the $In(NO_3)_3 \cdot H_2O$ in methoxyisopropanol dilution series.

Dilution	h [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	S [V/dec]
1:0	46.7 ± 1.9	0.64	0.25	-12.40	2.70	8.70
1:1	21.7 ± 0.9	6.75	2.86	-7.78	1.41	1.49
1:2	13.1 ± 0.2	1.94	4.57	-2.24	0.81	1.29
1:3	7.4 ± 0.2	0.65	9.78	-0.52	0.47	0.46
1:4	6.3 ± 0.8	0.44	8.89	0.98	0.49	0.34
1:5	6.4 ± 0.2	0.44	9.57	0.99	0.51	0.36

In Figure 35 one can see for thick layers the appearance of the same isolated grains observed in films fabricated with $InCl_3$ or acetylacetonate. The behavior of these grains depending on film thickness is not straight forward. Firstly, the thickest film appears to have a smooth surface, which does not exclude the possibility that these grains are not large enough to protrude through the surface of the film and are therefore present, but completely engulfed by the film.

The next sample has a very rough surface, with numerous grains showing out of the film, although they appear as grains only due to the aspect ratio set by the imaging software for clarity. In reality these grains have a diameter of 150 – 200 nm. Considering the scale of the image (55 nm) and the film thickness (21.7 nm), it means that they are 3 to 10 times wider than high, making the term islands more appropriate. These islands can be seen to cluster around craters, which disrupt the uniformity of the bulk of the film. The poor film quality is also reflected in a poor electrical performance.

As the film thickness decreases, so does the size of the islands, the films close up and become smooth and uniform at a dilution of 1:4, corresponding to a concentration of 0.1 M of indium ions in the solvent. At the same time the performance of the TFTs increases with decreasing film thickness and improving film quality, reaching the same performance as the oxoalkoxide from Evonik Industries AG and having in addition a lower hysteresis, a slightly positive onset and much lower off currents. A lower γ also indicates a better quality of the films and a better subthreshold slope is evidence of a higher quality of the semiconductor-insulator interface.

All this is not surprising considering the chemistry of the two materials. Apart from the solvent which was the same in both cases, the oxoalkoxide contains a relatively large fraction of carbon impurities originating from the alkoxide groups, which may or may not leave the film during thermal annealing. The nitrate, on the other hand, does not introduce any carbon impurities which one needs to worry about. Plus the nitrate anion may provide additional oxygen atoms to support the formation of the metal oxide network, and if not, readily decomposes at temperatures below 300°C [127]. What one should worry about though, are the water molecules bound to the indium nitrate, which can form hydroxide species that are hard to remove with low temperature processes and degrade the performance of TFTs [17]. Alternatively water molecules in a metal oxide film are thought to form deep trap levels with an acceptor-like behavior [130], which would also hinder the TFT performance.

With this in mind, $In(NO_3)_3 \cdot H_2O$ has shown a potential for solution-based TFT fabrication similar to that of the oxoalkoxide from Evonik Industries AG and by far superior to the other tested precursors, potential worth cultivating.

5.2. Performance of indium nitrate hydrate formulations

5.2.1. Solvent selection

The solvent used for the selection of the indium-containing precursor was selected based on literature considerations and kept the same for all tested materials in order to minimize the variables in the chemistry of the semiconductor formulation and compare different materials. The methoxyisopropanol molecule, however, is rather bulky and has a large carbon to oxygen ratio, e.g. C:O = 2:1. In an attempt to improve the quality of the semiconductor formulation, it was decided to test several different solvents and compare their influence on the performance of the TFTs fabricated with these solutions.

The candidates to replace methoxyisopropanol as solvent were the following:

- Ethanol – smaller molecule (should result in denser films), lower boiling point (should evaporate easier and more thoroughly out of the film upon thermal annealing), is also an alcohol and has the same carbon to oxygen ratio as methoxyisopropanol;

- Deionized water – has no carbon at all (should completely eliminate carbon-related impurities), promotes good dissociation of ionic species due to its high polarity [131], high performance of $In(NO_3)_3 \cdot H_2O$ in di-water TFTs has been reported with mobilities as high as 13.26 cm^2/Vs at only 250°C processing temperature [132];

- 3% solution of hydrogen peroxide in di-water – for all the advantages of the aqueous environment described above and additionally, the high reactivity of the peroxide;

- Ethylene glycol diacetate – has a higher oxygen content pro molecule and a lower C:O ratio than methoxyisopropanol and ethanol, does not contain hydroxyl groups which should circumvent the formation of indium hydroxide in the active layer;

- Acetonitrile – has a slightly higher boiling point than ethanol and a more than 2 times its dipole moment [133], which should influence positively the solubility of the precursor. The absence of oxygen in the solvent could provide an answer to the question whether it is necessary to use an oxygen bearing solving at all. It was also used by Han et al. to fabricate high performance TFTs with a charge carrier mobility as high as 55.26 cm^2/Vs [20].

Each stock formulation was prepared in an ambient atmosphere with a nominal concentration of 0.5 M of indium ions in solution, except the ethylene glycol diacetate one, which had a concentration of 0.42 mol/l. The ethanol, methoxyisopropanol, water and hydrogen peroxide solutions required less than one hour stirring at room temperature to completely dissolve the $In(NO_3)_3 \cdot H_2O$ and become clear. The ethylene glycol diacetate solution became clear after 72 hours of constant stirring at room temperature. Contrary to expectations, $In(NO_3)_3 \cdot H_2O$ did not dissolve completely in acetonitrile and even after prolonged stirring the solution remained turbid and had to be filtered through a 200 nm PA filter. Dilution series of all formulations were prepared and used to fabricate TFTs (see Chapter 4). Again, the acetonitrile solution behaved unexpectedly. When the clear stock solution was diluted further with acetonitrile, after some time the diluted formulation started forming white flakes of precipitate. The precipitate could easily be redissolved when a less than 10% volume of di-water was added to the solution. This means that some of the dissolved $In(NO_3)_3 \cdot H_2O$ lost its water molecules and became insoluble in acetonitrile, or formed with the solvent some insoluble complex. When filtered, the resulting clear solution

was in a metastable equilibrium and adding more acetonitrile shifted the equilibrium of the system to the right, e.g. more water molecules were lost and more insoluble product was formed. On the other hand, adding a small amount of water shifted the equilibrium to the left, providing enough water molecules for the indium nitrate to stay soluble. Since the interest was in the pure acetonitrile solution and not a mixture of water and acetonitrile, the dilution with acetonitrile was prepared fresh just before the fabrication of the TFTs and used before precipitation occurred.

The film thickness of each sample was measured with an ellipsometer and the surface roughness was determined with an AFM. Transfer characteristics of each TFT were measured in a glove box and in darkness. From each series of TFTs corresponding to the different solvents were chosen one with a thick active layer and one with a thin active layer, so that their thickness would be comparable across samples. The morphology of these samples is summarized in Figure 36.

Regardless of the solvent used, the thick layers formed the islands discussed above which differed in size and density. The aqueous and alcohol-based solutions also formed craters among the clusters of islands which affected the uniformity of the films. The aqueous solutions had a much denser island growth, while the acetonitrile formulation formed only isolated clusters of islands. The size of the islands formed by the ethylene glycol diacetate solution was considerably larger than that of the other formulations.

According to these results it is hard to speculate on what actually influenced the size and distribution of these islands. The size of the solvent molecules could not be the cause since water, having the smallest molecules, did not form the smallest islands. The acetonitrile islands formed scattered clusters and not a uniformly distributed film as observed in the other cases, probably as a result of having a thinner film compared to the rest of the samples. All the thinner films, apart from the ethylene glycol diacetate film, had a smooth, island-free surface (Figure 36).

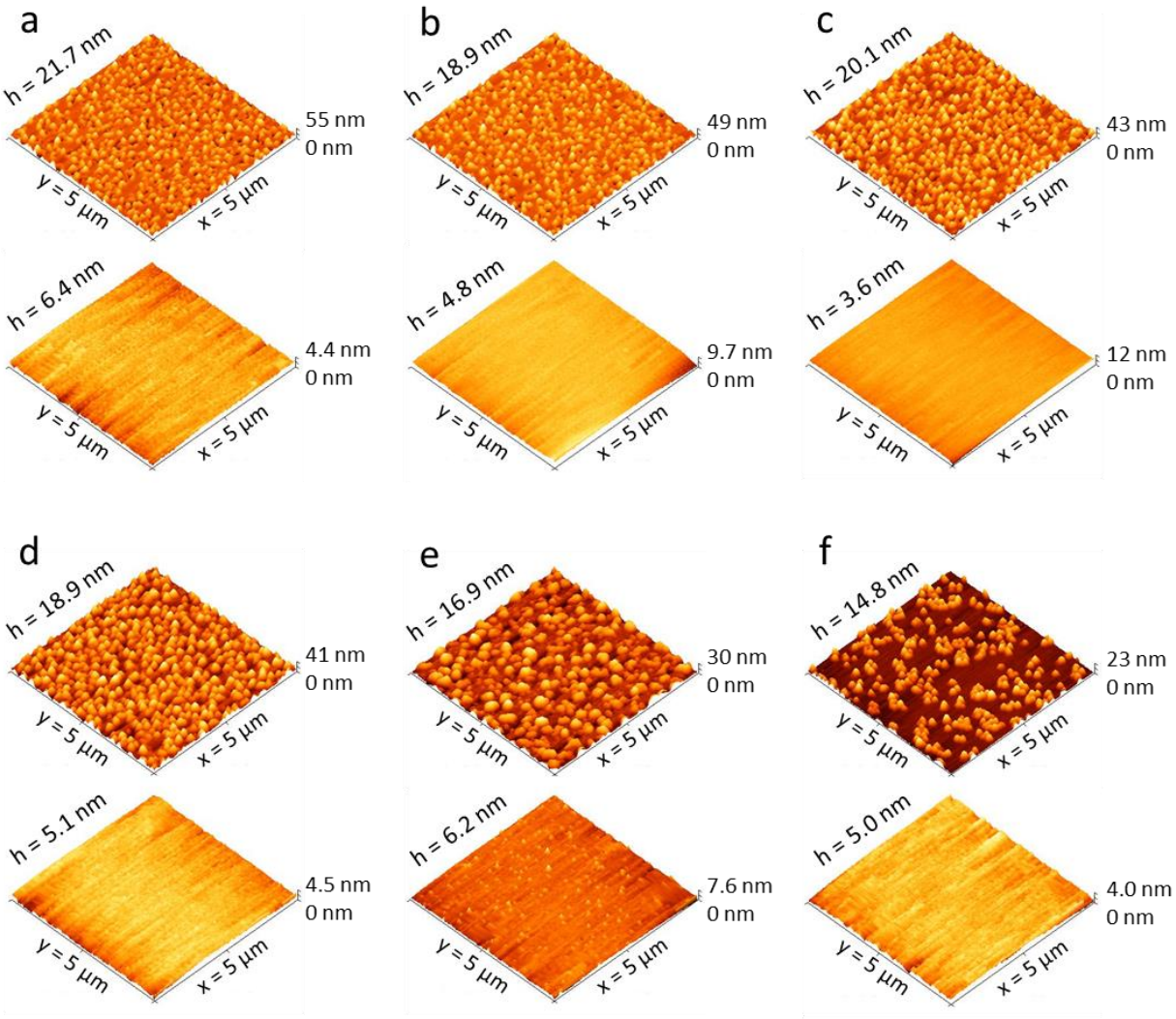

Figure 36. Surface morphology of the active layer of one thick and one thin film depending on the solvent of the semiconductor formulation: a) methoxyisopropanol, b) ethanol, c) di-water, d) 3% H_2O_2 in di-water, e) ethylene glycol diacetate, f) acetonitrile.

The transfer characteristics of the TFTs depicted in Figure 36 are plotted in Figure 37 for comparison.

The charge carrier mobility, threshold voltage, the disorder parameter γ and subthreshold slope were extracted from the data in Figure 37. To facilitate their comparison, these parameters were grouped in Table 10 next to the active layer thickness and surface roughness.

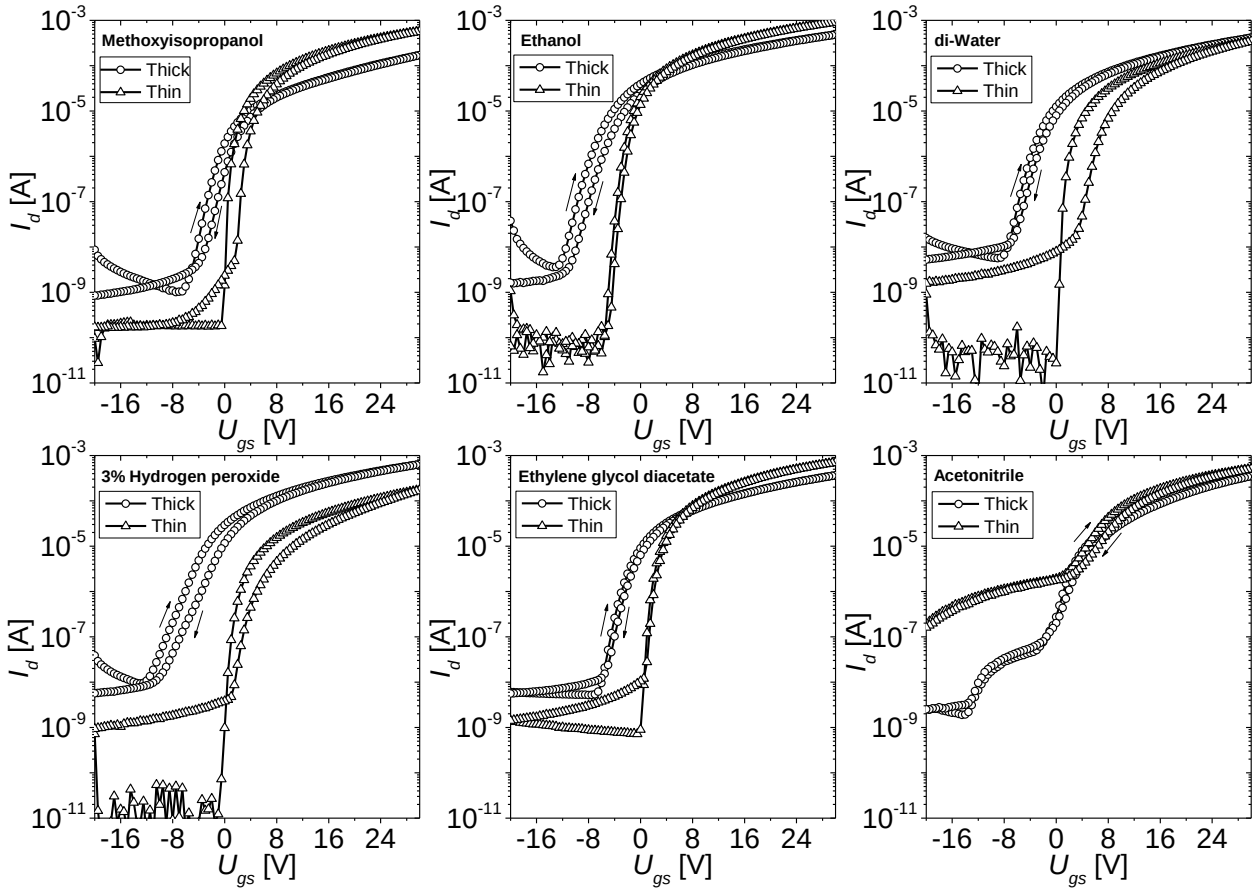

Figure 37. Transfer characteristics of TFTs prepared with $In(NO_3)_3 \cdot H_2O$ dissolved in various solvents, depending on film thickness. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 µm, d_{ox}= 230 nm, ε_{ox}= 3.9.

Table 10. Summary of the morphological and electrical performance data depending on the film thickness and solvent of the $In(NO_3)_3 \cdot H_2O$ formulations.

Solvent	h [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	S [V/dec]
Methoxyisopropanol	21.7 ± 0.9	6.75	2.86	-7.78	1.41	1.49
(MIPA)	6.4 ± 0.2	0.44	9.57	0.99	0.51	0.36
Ethanol	18.9 ± 0.9	5.94	5.55	-8.43	0.64	1.71
	4.8 ± 0.5	0.44	12.50	-2.51	0.48	0.55
Di-water	20.1 ± 1.4	6.47	5.91	-5.42	0.81	1.58
	3.6 ± 0.1	0.65	6.75	0.84	0.73	0.29
3% H_2O_2 in di-water	18.9 ± 1.5	6.49	8.50	-6.33	0.74	2.72
	5.1 ± 0.1	0.60	3.46	0.02	0.84	0.43
Ethylene glycol diacetate	16.9 ± 5.1	4.75	5.27	-4.84	0.77	1.31
(EGD)	6.2 ± 0.2	0.52	11.83	1.87	0.45	0.47
Acetonitrile	14.8 ± 0.2	3.91	7.62	-0.79	1.04	1.96
	5.0 ± 0.4	0.41	8.73	3.78	0.35	4.40

Table 10 and Figure 37 illustrate how the performance of the TFTs depends on the solvent of the semiconductor formulation. For each solution it is true that the thinner films produce better results. That is not surprising, since the thinner films also have a better morphology,

meaning lower film roughness. Figure 38 displays the dependence of the charge carrier mobility (a) and the subthreshold slope (b) of the fabricated TFTs on surface roughness. It shows that the smoother the film, the higher the performance. All TFTs with the thinner layers had comparable roughness, however a distinct separation of mobility values as a function of formulation solvent can be observed in Figure 38 a).

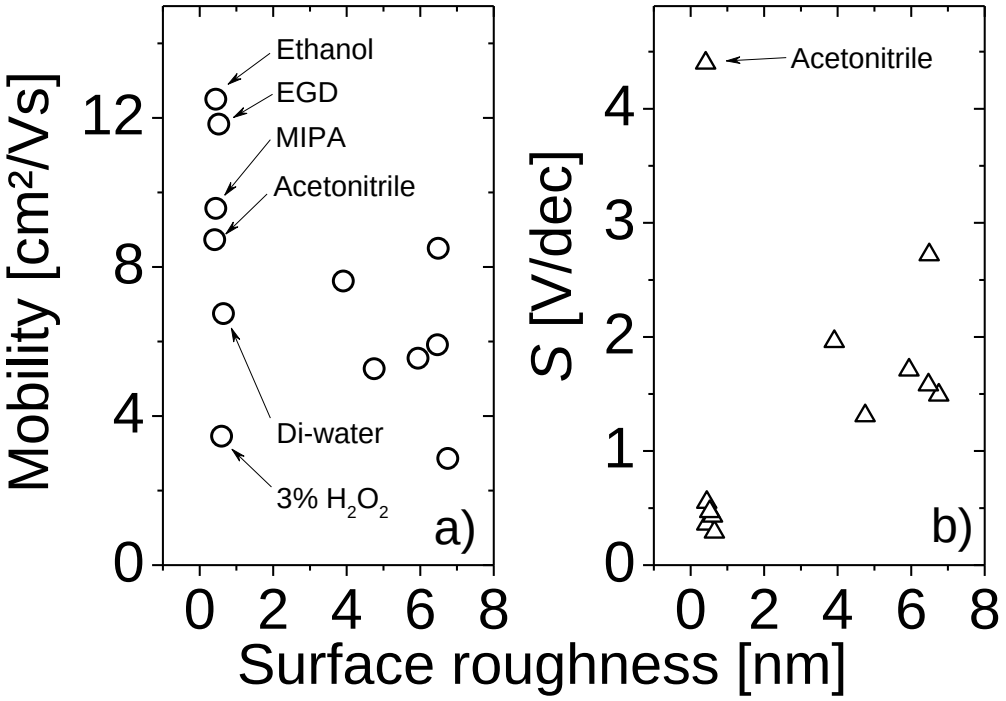

Figure 38. Charge carrier mobility a) and subthreshold slope b) of TFTs depending on the surface roughness of the active layer deposited from different $In(NO_3)_3 \cdot H_2O$-based solutions.

Out of the tested solvents the ones containing oxygen proved superior. Even though acetonitrile produced TFTs with high mobility, their off-current was unacceptably high, as well as the subthreshold slope. The shoulders in the transfer curves (Figure 37) signal the existence of an additional, low mobility active channel within the film, probably opened by an abundance of oxygen vacancies formed as a result of an oxygen deficient material.

The aqueous solutions performed the worst in comparison with the rest of the formulations, despite their advantage of no carbon contamination and reactivity in the case of the hydrogen peroxide formulation. Although the forward sweep of the gate voltage produces a well behaved transfer curve with low off-current, clear onset and small subthreshold slope, the backward sweep returns a noticeable hysteresis and does not close the channel completely, indicating charging effects taking place within the semiconductor.

At the same time the mobility could be inhibited by an excessive amount of unconverted hydroxyl groups.

The best performance was obtained with the alcohol- and EGD-based solutions. The ethanol and EGD solutions showed better mobility and a negligible hysteresis, but the ethanol formulation resulted in a negative onset and the EGD-based TFT had a slightly higher off-current. $In(NO_3)_3{\cdot}H_2O$ rate in MIPA produced enhancement mode TFTs with a low off-current, small hysteresis and a good mobility, which means that this formulation has the potential of becoming a semiconductor source for solution-based electronics.

5.2.2. Contact and sheet resistance

The contact and sheet resistances of the TFTs fabricated with the $In(NO_3)_3{\cdot}H_2O$ in MIPA formulation were evaluated using the TLM method. The respective values were analyzed with respect to film thickness and applied gate bias. A summary of the extracted data is presented inFigure 39.

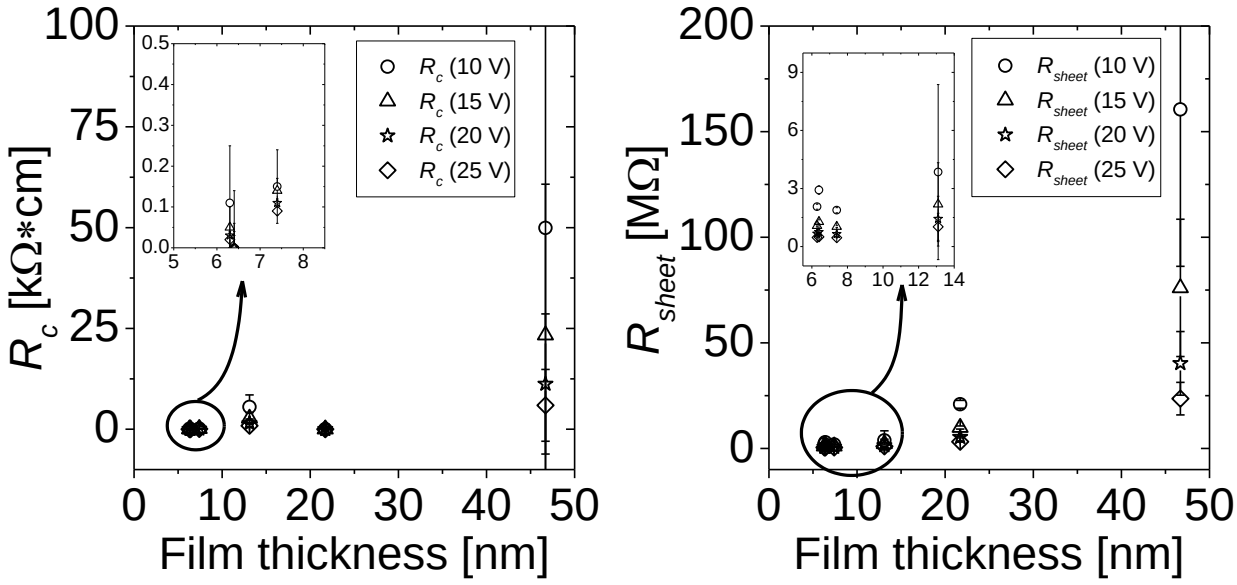

Figure 39. Contact and sheet resistance as a function of semiconductor film thickness of and applied gate voltage to the indium oxide TFTs fabricated with the $In(NO_3)_3{\cdot}H_2O$ in methoxyisopropanol formulation.

The values of the contact and sheet resistances measured with the indium oxide based TFTs are lower than values reported for sputtered IGZO with Mo contacts [134], sputtered IGZO with Cu, Al or Ti contacts [135], and sputtered ZnO, ZIO or IGO with Al contacts [136]. One can also see well that the resistances drop with decreasing film thickness and increasing

applied gate voltage via a power law. The TFTs with channel layers below 10 nm display contact resistances below 100 Ω·cm and sheet resistances in the order of 1 MΩ.

The decrease of the resistances with increasing gate voltage is understandable. Higher gate bias lowers the potential barriers at the contacts thus lowering the contact resistance, and increases the conductivity of the channel by inducing more charge, thus lowering the sheet resistance.

The behavior of the resistance with increasing semiconductor thickness is somewhat puzzling though. The sheet resistance is the channel geometry independent parameter which when multiplied with *L/W*, results in the channel resistance, which in turn is inversely proportional to the thickness of the conductive channel, under the assumption that the entire layer thickness is the conductive channel (Equation (38)),

$$R_{channel} = R_{sheet} \cdot \frac{L}{W} = \rho_{sheet} \cdot \frac{L}{W \cdot h} \tag{38}$$

where ρ_{sheet} is the resistivity of the material and *W*, *L* and *h* are the channel's width, length and height respectively. Equation (38) shows that if one plots the inverse of the sheet resistance determined experimentally using the TLM method against film thickness, one should obtain a straight line. This should be true for as long as the layer thickness is smaller or equal to the conductive channel. Beyond the conductive channel thickness this dependence should break. Since the charge distribution beyond the conductive channel does not decay as a step function, the portion of the film above the conductive channel should retain a certain conductivity and the total $1/R_{sheet}$ should continue to raise with film thickness, somewhat slower or approach asymptotically a saturation value.

Provided that the conduction through the semiconductor happens only inside the conductive channel, a film thicker than the conductive channel should not deteriorate the total resistance of the ensemble. If one views the additional thickness as a layer with a very high resistivity, connected in parallel with the conductive channel between the source and the drain electrodes, the total film resistance should decrease if anything. This is another argument to support the claim that the inverse of the sheet resistance should keep increasing as the thickness of the film raises beyond the conductive channel thickness.

Figure 40 illustrates the dependence of the calculated reciprocal sheet resistance on the semiconductor film thickness for the TFTs fabricated with the $In(NO_3)_3 \cdot H_2O$ in methoxyisopropanol dilution series. One can see that below 10 nm $1/R_{sheet}$ increases with thickness, as expected, however due to poor resolution and lack of data points in this region, it is hard to evaluate the dependence mathematically. Contrary to what was expected, $1/R_{sheet}$ decreases rapidly beyond 10 nm, meaning a rapid increase in channel resistance with film thickness. The reason for this behavior is not yet understood.

Nevertheless, the data from Figure 40 permits to infer that the thickness of the conductive channel in the active layer of the given material is around 7.4 nm. It would be more correct to place it in the interval 7.4 nm – 13.1 nm, since due to lack of data it is unclear how the reciprocal sheet resistance behaves in this region.

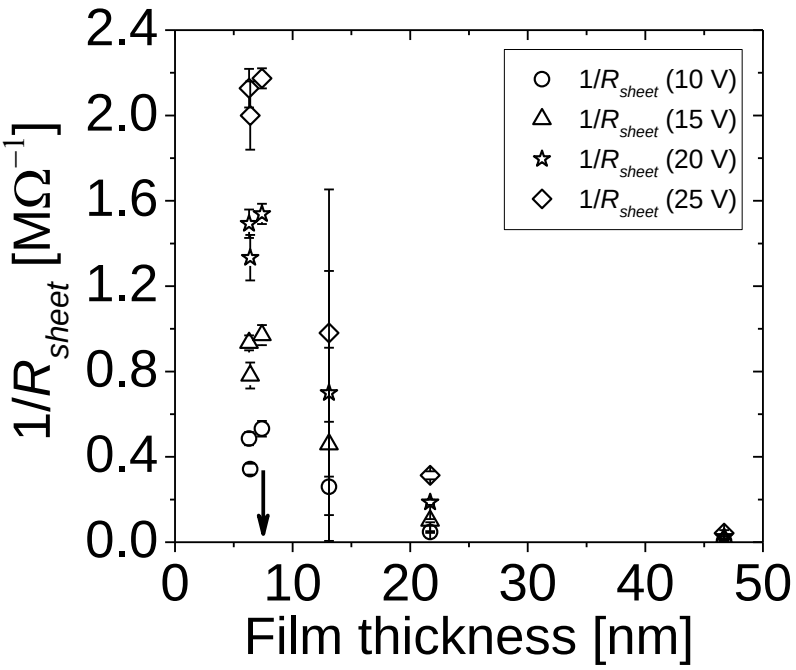

Figure 40. The dependence of the reciprocal sheet resistance on the active layer film thickness of the indium oxide based TFTs fabricated with the $In(NO_3)_3 \cdot H_2O$ in methoxyisopropanol formulation.

5.2.3. Potential for a low temperature process

Indium nitrate hydrate in methoxyisopropanol proved to be a very good semiconductor formulation when processed at 350°C. Because of these results it was decided to test the potential of this semiconductor at lower processing temperatures. The initial experiments were performed with the concentration of indium ions in the solvent which provided the

best results at 350°C, e.g. 0.083 mol/l. However at 250°C the performance of this solution was low. The TFTs had a very large hysteresis and a low mobility.

The cause was initially erroneously attributed to the fact that the semiconductor formulation might be susceptible to aging. Retesting it at 350°C again disproved this hypothesis because the results were similar to the ones obtained before. This has another important implication, namely that the given semiconductor formulation is stable even when stored in ambient atmosphere. There were no crystals or precipitate formed in the solution container over months of storage in ambient atmosphere.

Nevertheless it was decided to formulate a new dilution series and investigate the influence of the film thickness of the channel layer on the performance of the TFTs at 250°C annealing temperature. After spin coating the films, the TFTs were annealed for 1 hour at 250°C on a hot plate in ambient atmosphere, then measured unencapsulated inside a glove box. The results of this experiment are summarized in Figure 41 and Figure 42, which show the transfer characteristics of each TFT with their extracted figures of merit and the morphology of the films respectively.

Comparing Figure 35 with Figure 42, one can see that the film topology was similar for both dilution series, as well as the thickness of the films corresponding to the individual dilution factors. The striking result was that the maximum performance at 250°C shifted in the direction of a thicker layer (Table 11), resulting in mobility, threshold voltage and subthreshold slope values of 4.61 cm^2/Vs, 0.18 V and 0.26 V/dec respectively, for a (11.3 ± 0.5) nm thick channel layer. This maximum performance was obtained despite the particulate structure of the film and a higher surface roughness compared with thinner layers. Nevertheless, this result is one of the highest so far obtained for TFTs annealed for 1 hour at 250°C in ambient atmosphere and processed from solution, by adjusting only the film thickness of the active channel, not involving any additional annealing techniques, passivation, architectural improvements or chemical additives with increased reactivity.

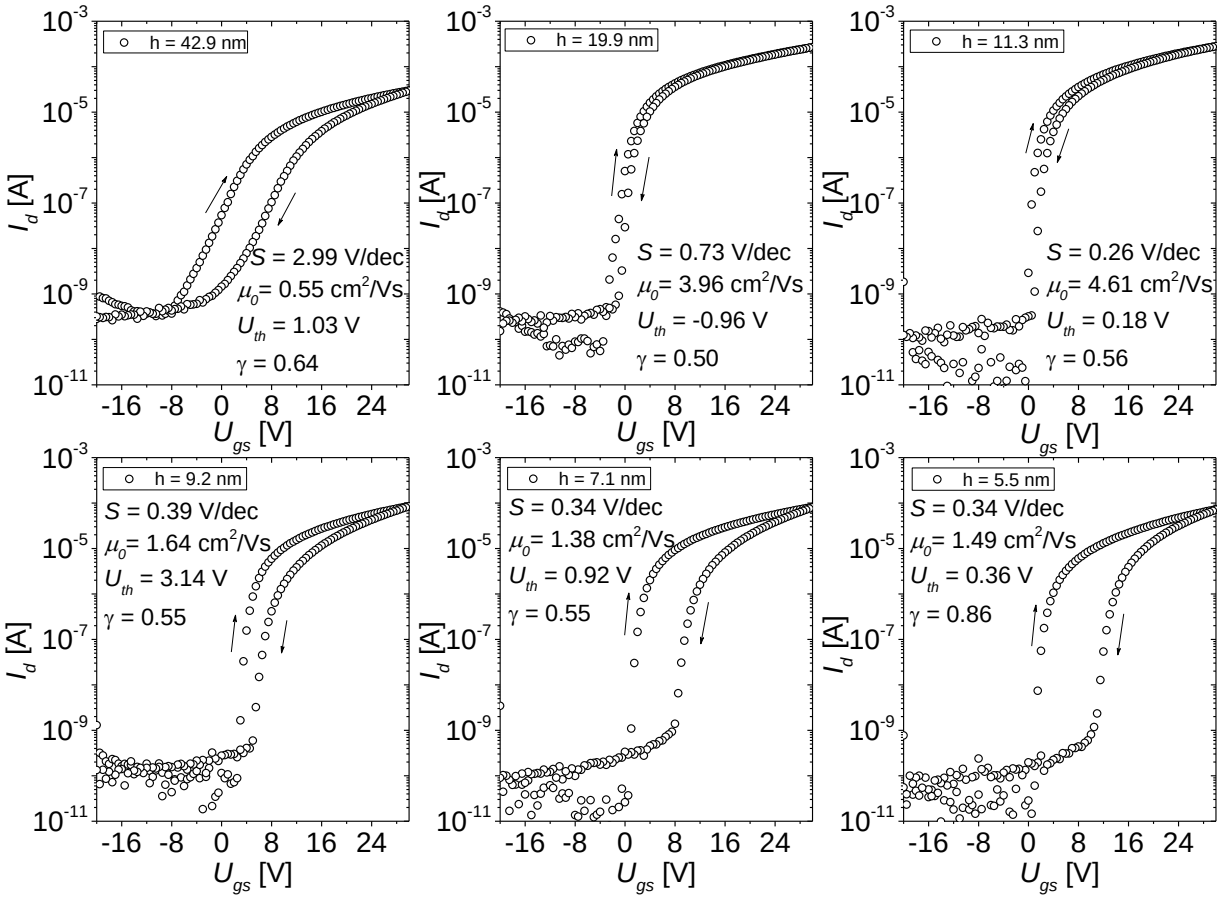

Figure 41. Transfer characteristics of TFTs prepared with $In(NO_3)_3 \cdot H_2O$ dissolved in MIPA, depending on film thickness. The measurements were made at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 μm, d_{ox}= 230 nm, ε_{ox}= 3.9.

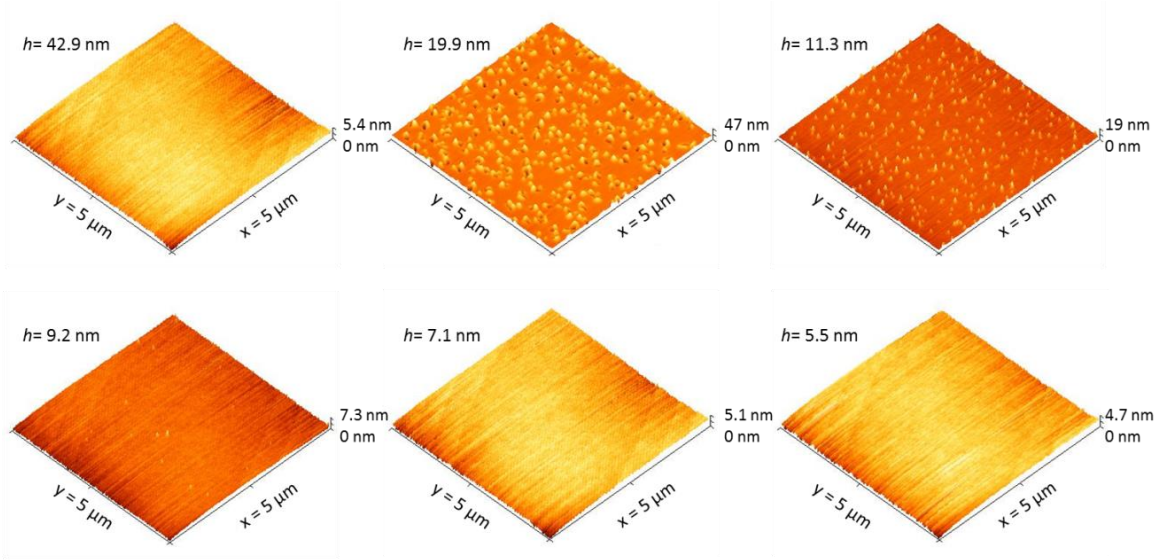

Figure 42. Surface morphology as a function of film thickness for thin films spin coated from $In(NO_3)_3 \cdot H_2O$ in MIPA formulations and annealed at 250°C.

Table 11. Morphological and electrical parameters of the TFTs fabricated with the $In(NO_3)_3 \cdot H_2O$ in MIPA dilution series at a processing temperature of 250°C.

Dilution	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
1:0	42.9 ± 1.6	0.66	0.55	1.03	0.64	2.99
1:1	19.9 ± 1.0	4.55	3.96	-0.96	0.50	0.73
1:2	11.3 ± 0.5	1.21	4.61	0.18	0.56	0.26
1:3	9.2 ± 0.5	0.54	1.64	3.14	0.55	0.39
1:4	7.1 ± 0.4	0.63	1.38	0.92	0.55	0.34
1:5	5.5 ± 0.2	0.60	1.49	0.36	0.86	0.34

5.2.4. Electrical stability

In order for a new semiconductor to have a practical value, the TFTs fabricated with it should be stable with respect to operating conditions, which means their figures of merit should change the least possible, or better yet, not change at all under conditions of constant operation. One of the methods often used to test the stability of TFTs is the Positive/Negative Bias Temperature Stress measurement (PBTS and NBTS respectively, depending on the sign of the applied gate bias), which simulates conditions of long term operation of a device [137].

TFTs fabricated with the 0.083M $In(NO_3)_3 \cdot H_2O$ in MIPA formulation, which provided the highest performance when annealed at 350°C, were subjected to both NBTS and PBTS measurements. In order to avoid reciprocal interference of the two measurement conditions on the same TFT, separate samples were prepared for each individual measurement. Both samples were fabricated concomitantly to ensure their similarity. Each sample was stressed with the corresponding parameters at 60°C for 4000s, starting after giving the samples enough time to reach thermal equilibrium with the surrounding atmosphere. Transfer characteristics were measured just before (t = 0 s), and during the stress measurement (at t = 100 s, 400 s, 1000 s, 2000 s and 4000 s). For a detailed description of the stressing procedure and parameters see section 4.4.1 and Figure 43.

The results of the two stress measurements are summarized in Figure 43 (transfer characteristics) and Figure 44 (figures of merit). Even though both samples were fabricated under equal conditions, there is a large difference between their performance parameters. The first noticeable issue is the fact that the mobility of one TFT is almost twice the mobility of the other.

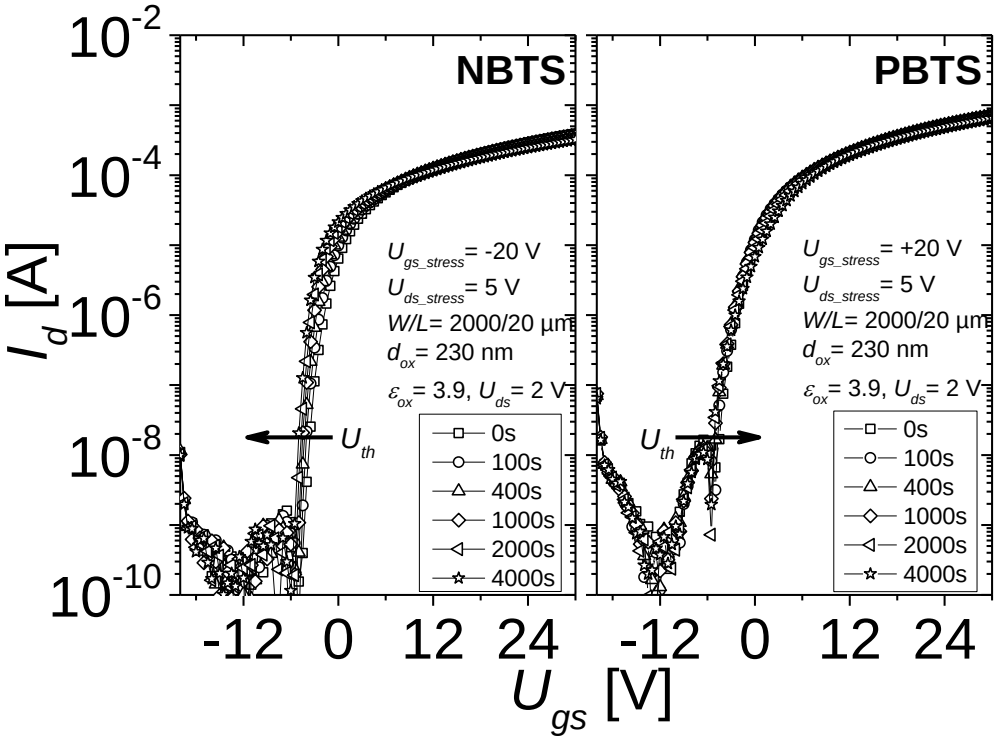

Figure 43. Transfer characteristics, stress parameters and structural information of the TFTs subjected to the NBTS and PBTS conditions.

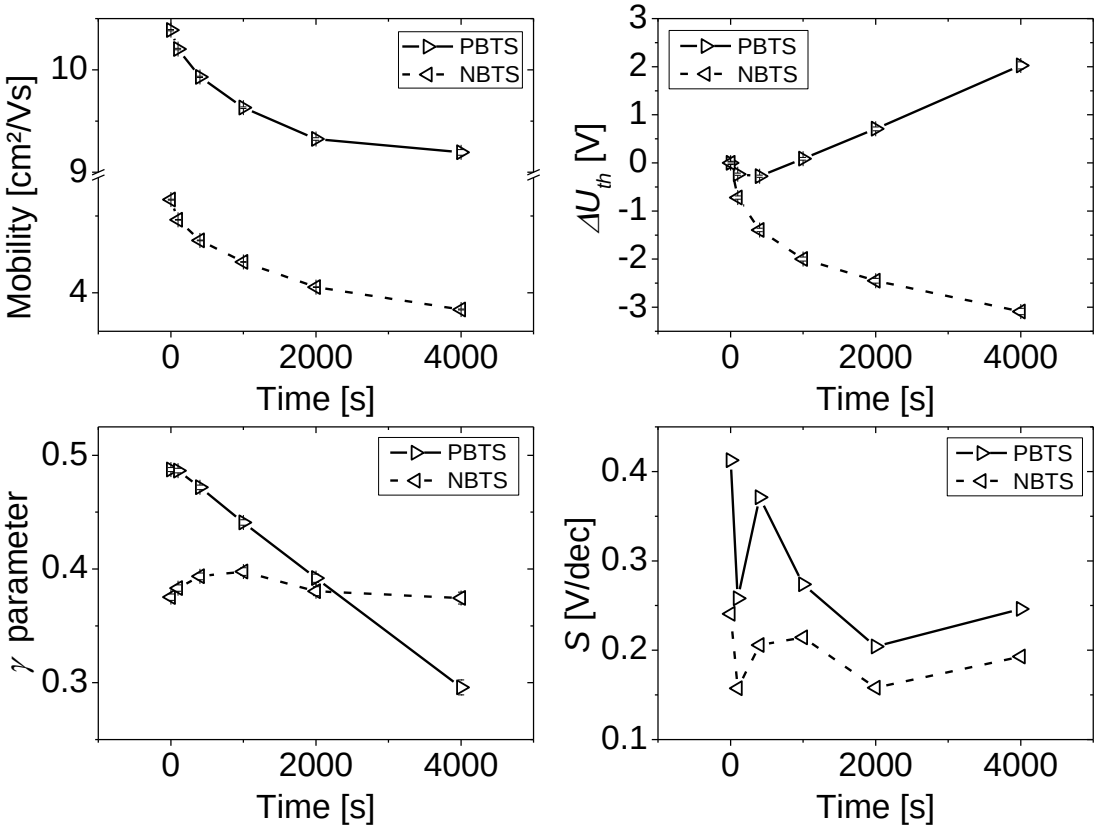

Figure 44. Figures of merit extracted from the transfer characteristics of the TFTs subjected to PBTS and NBTS conditions.

One could initially assume that the difference originated from the different stress conditions, but the fact that it was already there at t = 0 s, before the stressing had started, easily disproves this assumption. Furthermore, the completely discrepant behavior of the γ parameter and values of the subthreshold slope indicate an energetic dissimilarity of the two conductive channels, which might be a consequence of the possibly inadequate passivation material. The TFT that was stressed with the NBTS conditions has a lower subthreshold slope and disorder parameter, indicating a higher quality of the channel and less trap states at the semiconductor-insulator interface. But this result appears to contradict the observation of this TFT having a lower mobility. The passivation might diffuse into the semiconductor layer and indeed passivate the defects, improving the subthreshold slope, but at the same time act as an impurity within the film, decreasing the mobility.

Regardless of the stress conditions, both TFTs show reasonable stability. Their threshold voltage shifted by $|\Delta U_{th}|$ = 3 V after 4000 s under NBTS conditions and $|\Delta U_{th}|$ = 2 V after 4000 s under PBTS conditions. This is comparable to results reported in the literature on oxide TFTs fabricated via vacuum techniques [9], [138] and slightly better than solution processed TFTs [22], [101], [139].

5.2.5. Charge transport mechanism

The behavior of the TFTs under different bias stress conditions can be understood by having a closer look at the charge transport mechanism within the semiconductor material. It is thus worth taking a closer look at the energetic profile of the band gap of the semiconductor, because it should reveal the position of defects that can act as donors or acceptors and influence the performance of the TFTs.

One method that fulfills this purpose was described in section 2.2.2., and involves measuring the transfer characteristics of a transistor at different temperatures. The temperature dependence of the different figures of merit extracted from the transfer characteristics, especially of the charge carrier mobility, should reveal the position, nature and magnitude of the density of trap states responsible for the observed gate voltage and temperature dependence of the charge transport.

5.2.5.1. Inert atmosphere measurements

TFTs fabricated with the 0.083M $In(NO_3)_3 \cdot H_2O$ in MIPA solution and passivated as described in section 4.4. were lowered into the chamber of a liquid nitrogen cooled cryostat. The temperature of the chamber was lowered to -140°C and after the desired temperature was reached, the setup was allowed 10 minutes to reach thermal equilibrium before commencing electrical measurements. The same was performed at each measurement step after raising the temperature in 15°C intervals. All collected data was fitted with the gate voltage-dependent mobility model. The parameters of interest ($\ln(\mu_0)$, U_{th} and γ) were extracted from both forward and reverse sweeps of the gate bias and plotted against the inverse temperature and are displayed in Figure 45.

According to Lee *et al*., if there are charge traps at the semiconductor-insulator interface, they have to be first filled before they can be freed to participate in the charge transport [53]. This is the reason why the gate bias is swept in both directions. The filling of the traps happens as the TFT is turned on by gradually increasing the gate voltage from -20 to 30 V. When all the traps have been filled and the sweep of the gate bias is reversed, in the case of a multiple trap and release charge transport, the thermally activated charges will now participate in conduction, causing an apparent increase in charge carrier mobility.

The values of the logarithms of the extracted mobilities in Figure 45 however, are almost equal up to about room temperature. Their almost perfect linear dependence on the reciprocal temperature, corresponding to an activation energy of ΔE_a = 13.8 meV, and the small difference between them could be a sign that the density of states at this energy level is small. The similar behavior in both measurement directions means that either the traps had already been filled, before the measurement was started, or the trapping and release of the charges was very fast. Either way, the trapped charge was available for conduction in both measurement directions.

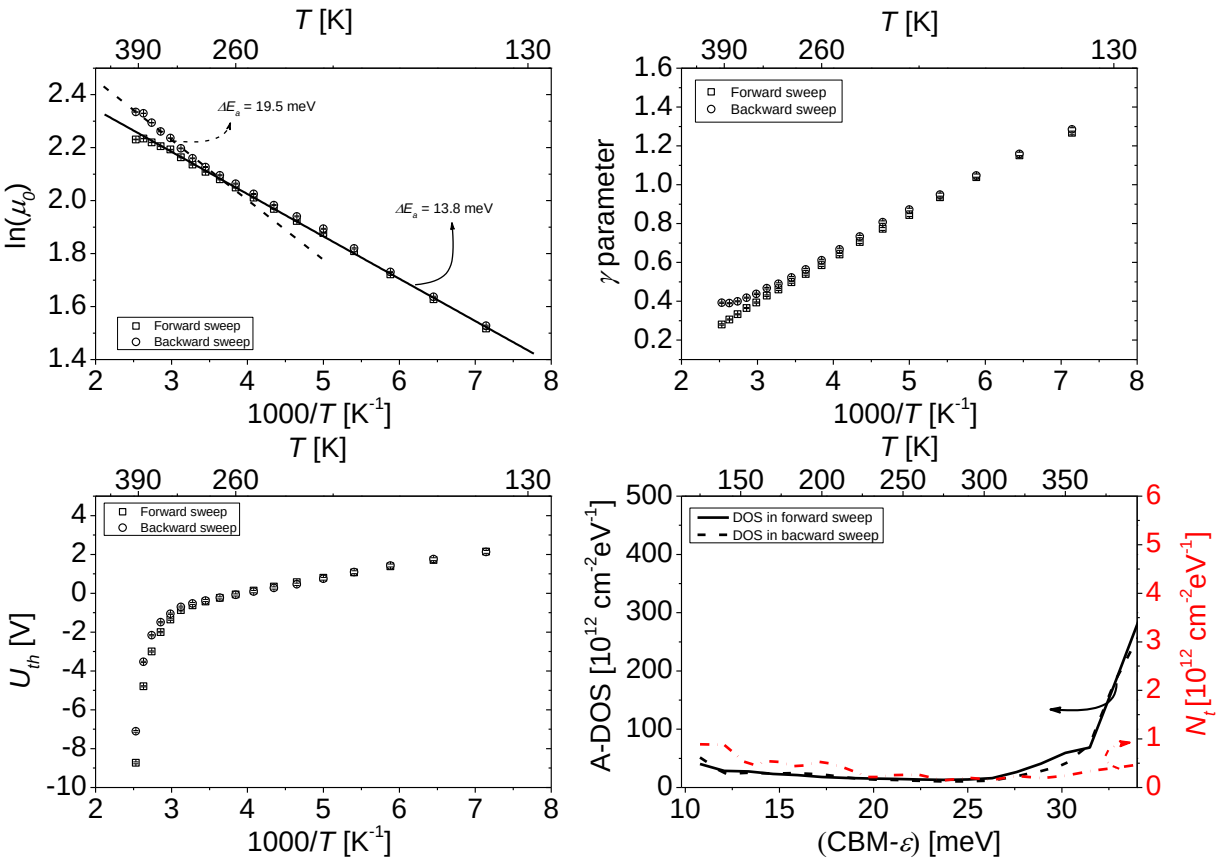

Figure 45. Temperature dependence of the figures of merit of a TFT fabricated with the $In(NO_3)_3 \cdot H_2O$ in MIPA solution as semiconductor. Measurements performed under nitrogen.

The disorder parameter γ shows a linear behavior with respect to reciprocal temperature (Figure 45), in very good agreement with the description by Vissenberg and Matters [140], with a characteristic T_0 parameter equal to 222.7 K, obtained from the linear fit of the dependence as the slope of the resulting line. Stallinga's description of the significance of the γ parameter [31] could provide more insight into the observed phenomena. According to Stallinga and co-authors, γ is an indicator of the ratio of free charge to trapped charge in the active layer. If the concentration of free charge depends exponentially on the position of the Fermi energy in the following way:

$$p_f = p_{f0} \exp(-aE_F) \tag{39}$$

and the concentration of the trapped charge in a similar way:

$$p_t = p_{t0} \exp(-bE_F) \tag{40}$$

then γ would have the expression:

$$\gamma = \frac{a}{b} - 1 \tag{41}$$

If so, the decrease of γ with increasing temperature would mean an increase in the concentration of free charges within the film and the decrease in the amount of trapped charge. Since the amount of traps should be independent on temperature, unless the semiconductor suffers severe structural changes and generates new defects to act as traps, the exponential increase in mobility with temperature is very well supported by the behavior of the γ parameter.

The behavior of the mobility and the γ parameter also supports the decreasing threshold voltage. U_{th} becomes more negative as the amount of available, thermally activated charge in the channel rises with increasing temperature. As the temperature increases above ~60°C (= 333 K), the threshold voltage plummets into the negative direction. A similar effect was observed by Park *et al*. when the authors annealed IGZO based TFTs in a nitrogen atmosphere [75].

A possible explanation to this observation might be the following: since the thickness of the semiconducting layer is about (6.4 ± 0.2) nm and the conductive channel is assumed to be thicker than 7 nm (see section 5.2.2), any changes happening on the surface of the semiconductor would have a strong impact on the performance of the TFT. The indium oxide surface, exposed to a nitrogen atmosphere, finds itself in a strong non-equilibrium state and starts losing the loosely bound oxygen atoms despite the passivation layer shielding it from the atmosphere. This effect is additionally aggravated by the constant supply of thermal energy. The oxygen atoms ejected from the surface of the semiconductor leave behind a positively charged site (known as an oxygen vacancy) and two free electrons located on the neighboring indium atoms [141]. In equilibrium the electrons shield the oxygen vacancy and the whole system remains in a neutral state.

According to Medvedeva and Hettiarachchi, the neutral oxygen vacancies V_o^0, in their ground state, are located energetically deep inside the band gap, below the Fermi energy and cannot contribute to conduction [141]. In order for an oxygen vacancy to become conductive, it has to be excited into a singly ionized state, marked with V_o^+, which requires a relatively large amount of energy. This amount of energy cannot be supplied by

temperature; therefore it would seem that oxygen vacancies could not be responsible for the increased conductivity observed above 60°C.

Medvedeva's analysis, however, extends over bulk phenomena. In the bulk of the semiconductor the oxygen vacancy is stabilized by the charge of the neighboring atoms which lower its energy. At the surface of the semiconductor an oxygen vacancy could be destabilized, its equilibrium energy level raised and its ionization energy lowered. Higher temperatures, combined with applied gate bias, could now easily cause the formation of new ionized oxygen vacancies. Assuming that neutral vacancies are formed by increased temperature, the positive gate bias ionizes them as the transistor is turned on. In the backward sweep of the gate voltage the ionized oxygen vacancies start behaving as trap centers, which manifests itself via a lower current and more positive threshold voltage (increasing clockwise hysteresis), as well as slightly higher γ parameter values of the backward swept transfer curves (Figure 45).

Another option to consider is the substitution of oxygen atoms by nitrogen atoms either on the surface of the semiconductor, or in its bulk, or both. The smaller effective mass and lower band gap of indium nitride [142] could explain the abruptly increasing conductivity observed above 60°C. However, the low reactivity of the nitrogen gas and instability of indium nitride itself speak against the prospect of substitution of oxygen by nitrogen atoms in the given semiconductor.

An attempt to evaluate the magnitude and position of the newly created trap states was made by applying two models for determining interfacial density of trap-states. The first well known model requires the calculation of the subthreshold slope from the transfer characteristics measured along the temperature range. The values of the subthreshold slope are then converted into the N_t via equation (32). Plotting N_t versus the applied thermal energy to the system (k_BT) shows that N_t did not vary much (Figure 45), over the entire temperature range, suggesting that there were no or very few traps generated a the semiconductor-insulator interface.

The second method, proposed by Lee *et al*. [52], involved the investigation of the U_{th} variation with respect to applied energy to the system, by replacing the energy of the photons with thermal energy. This method failed to produce sensible results due to several

reasons. First of all, during the derivation of the model formula the authors simplify the integration of equation (34) by setting the Fermi distribution equal to 1, corresponding to the 0 K distribution. In this work the temperature was the main parameter that varied the energy input into the system, and apart from not being equal to 0 K, was also varying, which introduces an error into the derived model equation. This model uses the density of charge to determine the density of trap states and is highly susceptible to charge variation, in this case due to oxygen vacancy formation. Lastly, this model assumes that the excited charge is confined within the conductive channel, which ideally is confined in 2 dimensions at the semiconductor-insulator interface. In this case the conductive channel is as large as the whole channel layer, meaning that the model predicts not only the interfacial density of traps, but traps in the entire thin film, i.e. traps formed by the oxygen vacancy sites. This results in a strongly overestimated areal density of states (Figure 45) with a questionable validity.

5.2.5.2. Ambient atmosphere measurements

Because of the temperature limitations imposed by the sample holder and the severe generation of oxygen vacancies at temperatures above 60°C in a nitrogen atmosphere, higher temperature measurements had to be performed using a different setup and in ambient atmosphere. In this experiment the temperature could be risen from RT to 220°C, beyond which the measurements were distorted by increased contact resistance of the probe station needles and the contact pads of the TFTs.

A similar summary to the one performed for the nitrogen atmosphere experiment (section 5.2.5.1) of the extracted figures of merit from the measured transfer characteristics is presented in Figure 46.

A first glance at Figure 46 shows that the effects observed at lower temperatures became more pronounced as the temperature of the TFT was raised further. The behavior of the TFT in the range from RT to 380 K (overlapping with the measurements in the nitrogen atmosphere at low temperatures) is different from that illustrated in Figure 45. The difference was attributed to the fact that the measurements were performed in air, which in addition to oxygen contains also water molecules. Both oxygen and water can be adsorbed on the surface of the semiconductor and negatively influence the performance of the TFT,

especially when the conductive channel is exposed to the ambient atmosphere, if the passivation layer does not form a dense enough protective film.

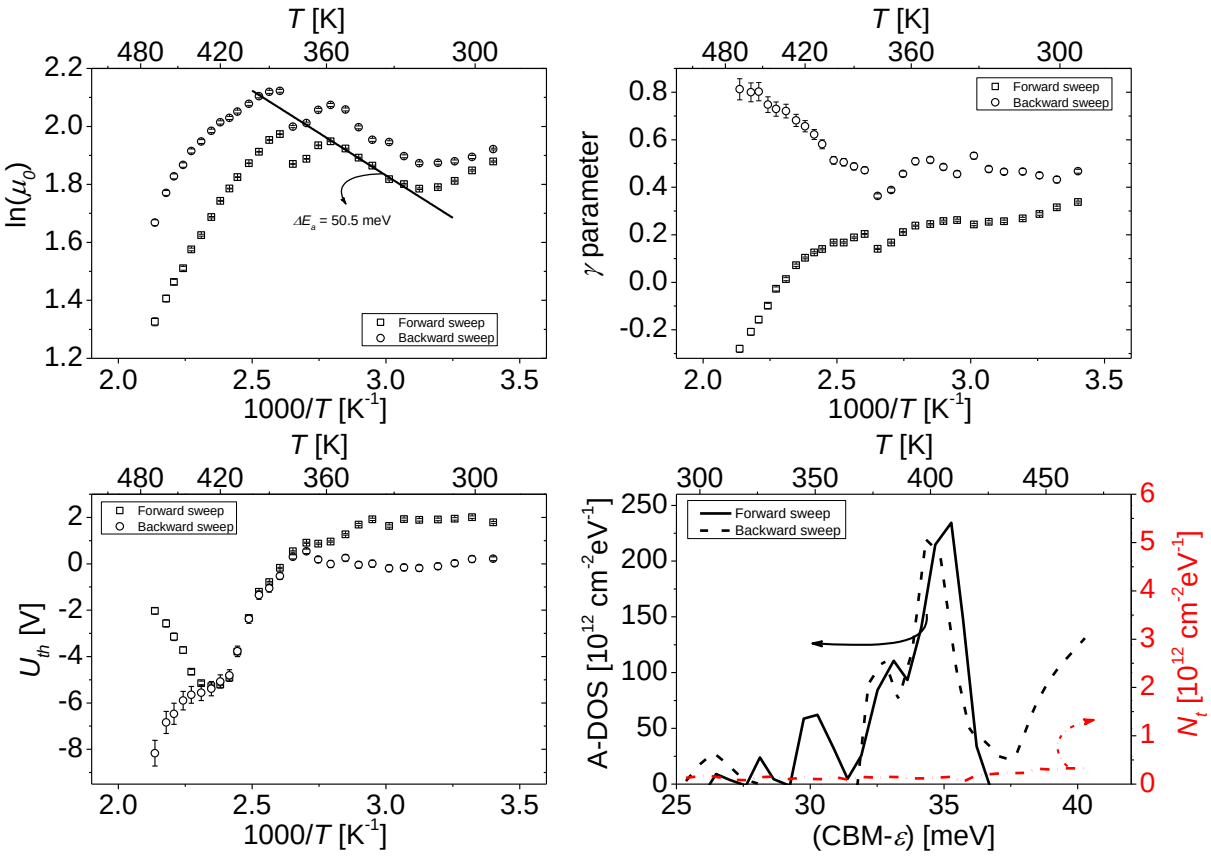

Figure 46. Temperature dependence of the figures of merit of a TFT fabricated with the $In(NO_3)_3 \cdot H_2O$ in MIPA solution as semiconductor. Measurements performed in air.

The values of the γ parameter coincided well with the corresponding temperature region measured in the nitrogen atmosphere, consistent with a similar ratio of free to trapped charge. Nevertheless the large difference between the values extracted from the forward and backward gate voltage sweeps indicated the existence of a large amount of traps. The nature of these traps appeared similar to the neutral oxygen vacancies which could be emptied during the forward gate voltage sweep, thus a larger γ value, and refilled during the backwards sweep. But this rationalization contradicts the observation that the mobility values were higher and the threshold voltage lower for the backwards sweep of the gate voltage, which would indicate exactly the opposite. The somewhat constant behavior of the U_{th} up to ~100°C suggests that the concentration of these traps remained constant and no additional traps were generated.

Above 100°C a large amount of additional charge was generated, presumably in the form of oxygen vacancies. The γ parameter extracted from the forward transfer curves started to decrease fast indicating a large buildup of charge, which then suddenly became trapped as the gate voltage was swept backwards and the γ parameter suddenly increased. The large charge concentration caused the threshold voltage to decrease suddenly. The large density of trap states made the mobility appear to decrease.

The density of interfacial trap states calculated from the subthreshold slopes of the transfer curves remained relatively constant – a sign of a good quality of the semiconductor-insulator interface. The areal density of states calculated from the U_{th} shift once more reflected the generation of charges above 100°C.

5.3. Performance of oxoalkoxide formulations

So far the indium nitrate hydrate precursor has shown a formidable performance compared to other investigated indium sources for an indium based precursor formulation. The nitrate system was optimized for processability in ambient atmosphere at 350°C and characterized morphologically and electrically. It also proved to have the potential to be applicable in processes involving annealing temperatures as low as 250°C.

Section 5.1.5 described the morphological and electrical properties of a different indium source, an indium oxoalkoxide produced at Evonik Industries AG, with a similarly high performance as the optimized nitrate system. Despite having a larger surface roughness of the semiconductor layer, the TFTs fabricated with this precursor showed comparatively large mobilities, threshold voltages, slightly larger subthreshold slopes and γ parameters, which is understandable considering the morphology of the active layers. It was assumed that by improving the surface of the channel layer, it would be possible to increase the performance of the TFTs fabricated with the indium oxoalkoxide formulations.

5.3.1. Solvent selection

A similar solvent screening as for the nitrate system was performed on the oxoalkoxide precursor. Since alkoxides hydrolyze at the slightest contact with water, the aqueous systems were omitted from testing. The performance of the methoxyisopropanol formulations is described in Figure 32 and Figure 33, and summarized in Table 8 in section

5.1.5. The TFTs fabricated with formulations based on acetonitrile or ethanol achieved at best half the mobility attainable with the methoxyisopropanol system. The reason behind such poor performance lies with the fact that the respective formulations resulted in defectuous films (Figure 47).

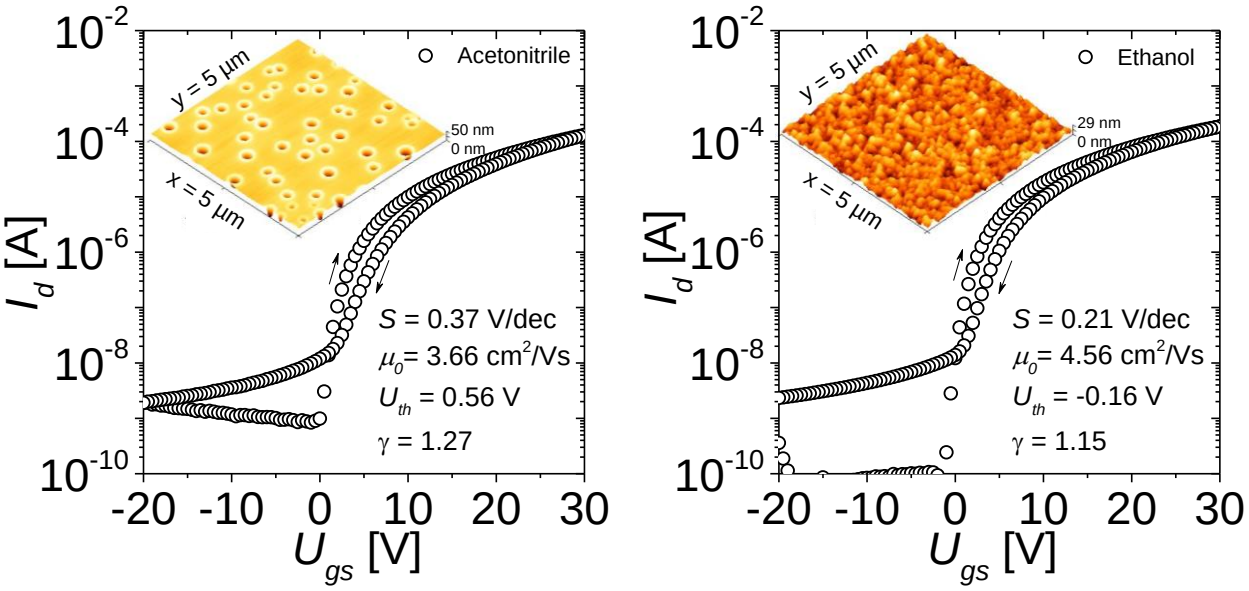

Figure 47. Performance of TFTs fabricated with indium oxoalkoxide in either acetonitrile or ethanol as semiconductor precursor formulations. Transfer curves measured at U_{ds} = 2V. The TFTs had the following structural parameters: W/L = 2000/20 µm, d_{ox}= 230 nm, ε_{ox}= 3.9.

While the thin films resulting from spin coating the ethanol solutions on the TFTs' substrate had a larger surface roughness despite a similar structure compared to the methoxyisopropanol based films, the acetonitrile solution based thin films were disrupted by large craters whose diameter exceeded 300 nm.

The damage to the films could not have been caused during film deposition because the wetting of the substrate was very good. There was no observable tension in the wet films. They appeared smooth and defect-free immediately after spin coating, which means the defects must have formed during annealing. The low boiling point of the solvent might have caused a violent evaporation event which dried the film instantaneously preventing it to relax and form a uniform and smooth layer.

It was then decided to try a higher boiling point solvent – tetrahydrofurfuryl alcohol (THFA) – for having a boiling point of 178°C, good wetting properties, a rather small molecule and a good ability to dissolve the oxoalkoxide.

5.3.2. Figures of merit as a function of film thickness

A stock solution was prepared by dissolving 0.5 g of the indium oxoalkoxide in 10 ml of THFA and stirred for 24 hours at room temperature. The formulation was then filtered through a 200 nm PA filter and resulted in a clear dark orange solution. The color of the solution gave the impression that it was more concentrated than the methoxyisopropanol formulation.

A dilution series was prepared as with all previously tested materials. Surprisingly, the diluted formulations produced extremely thin films and the respective TFTs showed a very low performance, which suggested that the stock solution was actually thinner compared to the methoxyisopropanol formulation. The thickness of the films was then varied by means of changing the spin coating speed. In this manner it was possible to systematically decrease the semiconductor layer thickness from (17.3 ± 0.2) nm down to (5.7 ± 0.5) nm.

The fabricated spin coated films were then annealed for 1 h at 350°C in ambient atmosphere and measured in a glove box after that. The resulting transfer characteristics and the extracted figures of merit are collected in Figure 48. The morphological characteristics of the thin films were collected with the AFM and are summarized in Figure 49 and Table 12.

As expected, employing a higher boiling point solvent for the precursor formulation fabrication produced very smooth films with a surface roughness at the AFM's resolution limit of 0.5 nm. The curved lines appearing on the images displayed in Figure 49 were initially thought to be a spin coating artifact, waves produced during the coating procedure. It was then discovered that they appeared in exactly the same fashion regardless of the measurement position and direction on the TFTs' substrate. This means the lines were a product of the measurement setup.

Due to the fluidity of the spin coated films, the patterning of the semiconductor via mechanical scribing was not very effective, which resulted in high off currents (Figure 48). Applying a more appropriate patterning technique might solve this problem and lower the off current considerably. Yet, in comparison with other tested formulations, this precursor solution achieved an astonishing mobility of 15.12 cm^2/Vs, at a subthreshold slope of 0.72 V/dec and threshold voltage of -2.36 V.

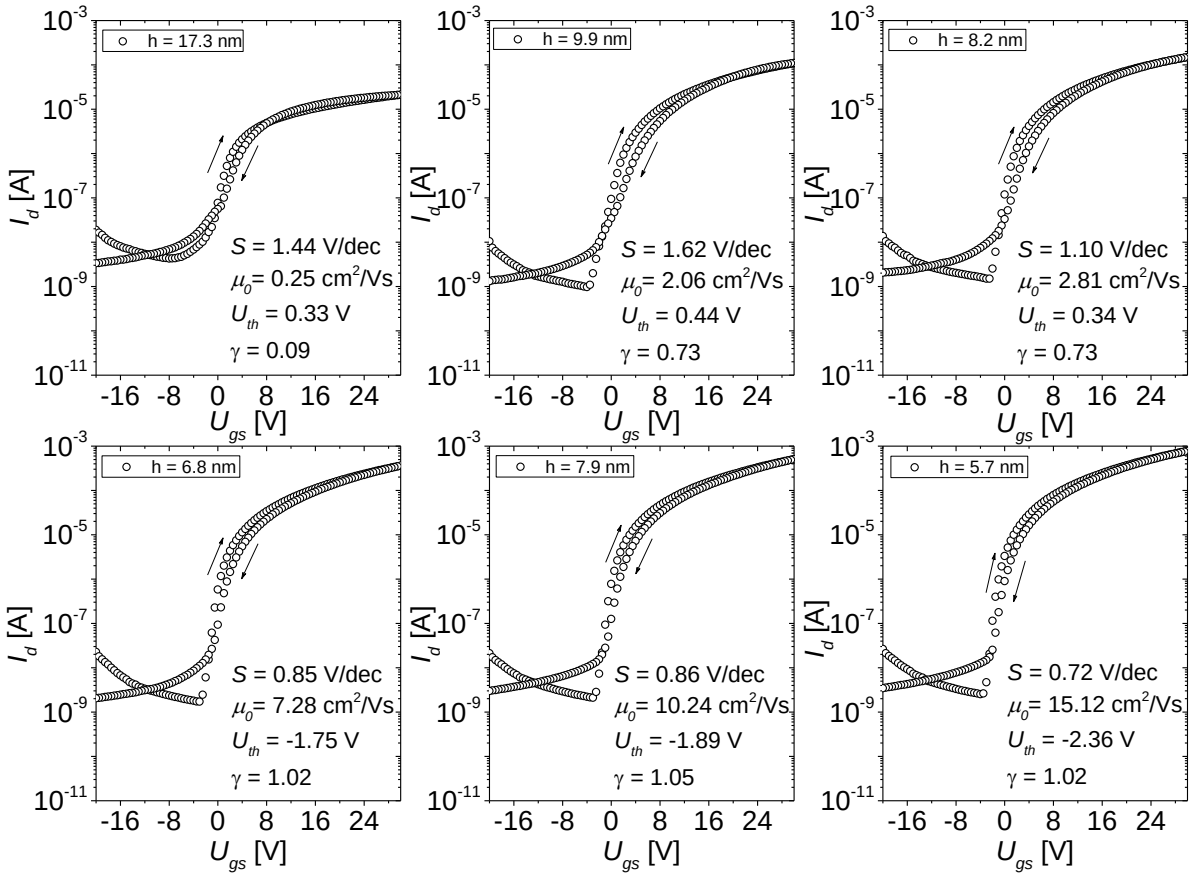

Figure 48. Transfer characteristics of TFTs prepared with the indium oxoalkoxide in tetrahydrofurfuryl alcohol formulation. The measurements were conducted at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 μm, d_{ox}= 230 nm, ε_{ox}= 3.9.

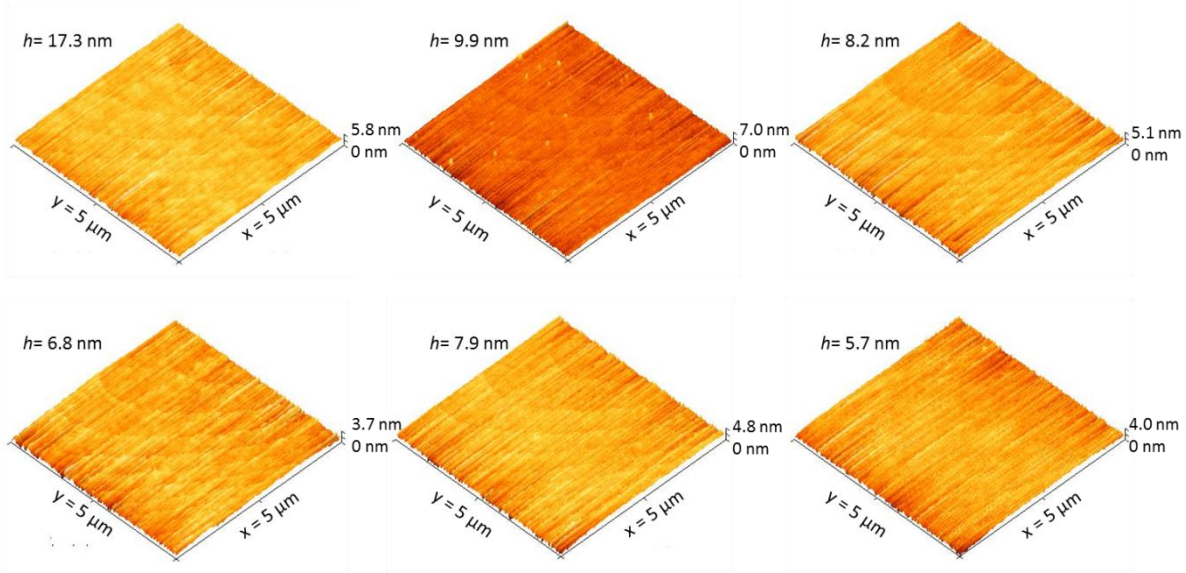

Figure 49. Surface morphology as a function of film thickness for thin films spin coated at different speeds from indium oxoalkoxide in tetrahydrofurfuryl alcohol formulation.

The γ parameter was slightly lower than that of TFTs fabricated with the other oxoalkoxide solutions, indicating a lower concentration of trapped charge with respect to its

free charge, explaining the better performance. The same trend is not observed though within the series of samples with varying semiconductor layer thickness.

As the films became thicker, γ decreased significantly; this should have triggered a better performance for the thick layers, but the opposite was observed. The large subthreshold slope suggests that even though the concentration of charge increased due to the thickness of the thin films, as well as the ratio of free to trapped charge described by γ, so did the concentration of trap states at the semiconductor-insulator interface, which had a detrimental effect on the charge carrier mobility.

Table 12. Morphological and electrical performance data of the TFTs fabricated with the indium oxoalkoxide in methoxyisopropanol dilution series.

Speed [rpm]	*h* [nm]	S_{rms} [nm]	μ_0 [cm^2/Vs]	U_{th} [V]	γ	*S* [V/dec]
2000	17.3 ± 0.2	0.49	0.25	0.33	0.09	1.44
3000	9.9 ± 0.7	0.52	2.06	0.44	0.73	1.62
4000	8.2 ± 0.3	0.51	2.81	0.34	0.73	1.10
5000	6.8 ± 0.3	0.42	7.28	-1.75	1.02	0.85
6000	7.9 ± 0.4	0.50	10.24	-1.89	1.05	0.86
7000	5.7 ± 0.5	0.47	15.12	-2.36	1.02	0.72

Plotting the mobility against semiconductor film thickness, one observes a behavior which is well described by a lognormal distribution (Figure 50 a). The same behavior was shown by the TFTs fabricated with the indium oxoalkoxide in methoxyisopropanol formulations, but not by the $In(NO_3)_3{\cdot}H_2O$ in MIPA (Figure 50 b).

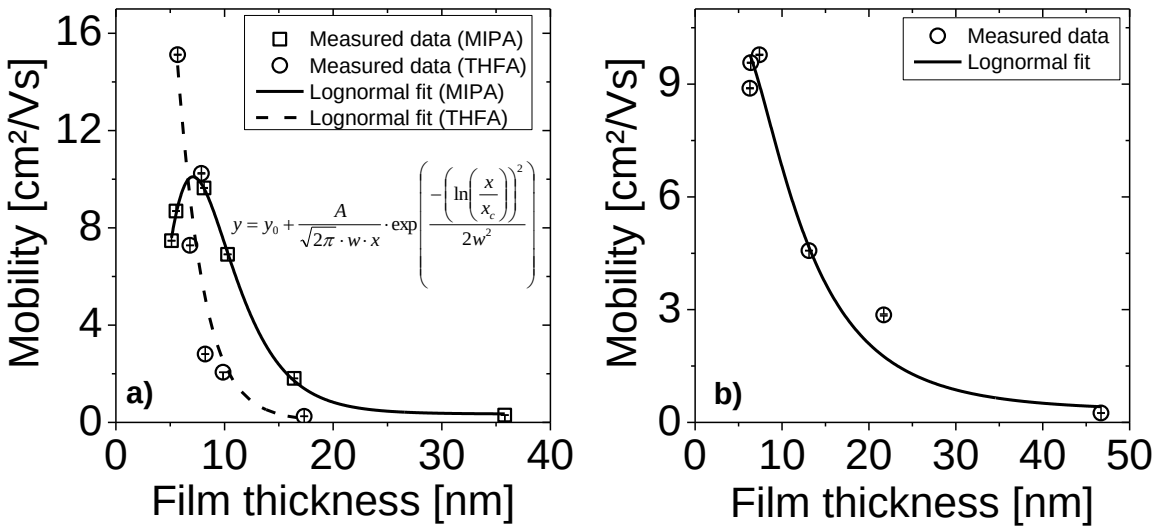

Figure 50. Dependence of the charge carrier mobility on film thickness and solvent of the oxoalkoxide formulations a) compared to $In(NO_3)_3{\cdot}H_2O$ based TFTs b).

The fitting equation of the lognormal distribution is also shown in Figure 50 a. In this equation y_0 is the offset of the curve, A is the area under the curve, w is the standard deviation and x_c is the position of the mean value along the x axis.

A lognormal distribution of a quantity, in this case the mobility, with respect to a parameter, here film thickness, means that the quantity depends exponentially on another quantity which is normally distributed with respect to the parameter. Therefore, the mobility should depend exponentially on a quantity normally distributed along the spectrum of semiconductor film thicknesses. In the case of MTR transport [31] the mobility depends exponentially on the activation energy of the trapped electrons (equation (12)). One could look at the activation energy in a different way.

The semiconductor films of some of the oxoalkoxide formulations have shown a grainy structure. Where there are grains, are also grain boundaries to be found. It is well known that grain boundaries present an energetic obstacle for charge carriers during conduction [29]. The barrier the grain boundaries pose depends on the quality of the interface between the grains, which in turn depends, among others, on their size. Larger grains have a smaller contact area, thus a larger energetic barrier. Smaller grains may have a larger contact area, with lower barrier energy, but their overall amount could still introduce a considerable obstacle for the charge transport. Viewing ΔE_a as the sum of the contributions from all grain boundaries, a few large grains could end up having the same ΔE_a as many small grains.

It was shown here that the size of the grains can be influenced by the thickness of the semiconductor. As the films are made thinner, their number increases slowly and the energy of the individual grain boundaries ($\Delta\varepsilon_i$) decreases fast as the packing of the grains improves. The total ΔE_a decreases up to a point where the number and size of the grains result in a minimum total energy. After this point the number of grains increases faster than $\Delta\varepsilon_i$ decreases, which results in an increase in ΔE_a. Thus ($-\Delta E_a$) would have a peak shaped, very likely a normal distribution along film thickness and would validate the observed dependence of the charge carrier mobility.

This rationale would describe well those formulations, which resulted in grainy films, like indium oxoalkoxide in ethanol or methoxyisopropanol. The THFA based system did not show any grains; at least none were detected with the AFM, and the μ vs. h curve had a shape that

could be fitted with other functions as well, i.e. a power law, a high degree polynomial, an exponential, as long as the physics of charge transport through the semiconductor would be accurately described. The main difficulty in this particular case is the generation of meaningful data for very thin semiconductor layers for a thorough analysis, which allows only speculations about the physics behind the observed phenomena at this time.

5.3.3. Contact and sheet resistance

The TLM method was applied to the two oxoalkoxide systems to extract the contact and sheet resistance of the respective TFTs. Figure 51 illustrates the dependence of the contact and sheet resistance of the TFTs fabricated with the methoxyisopropanol formulations on film thickness and gate voltage.

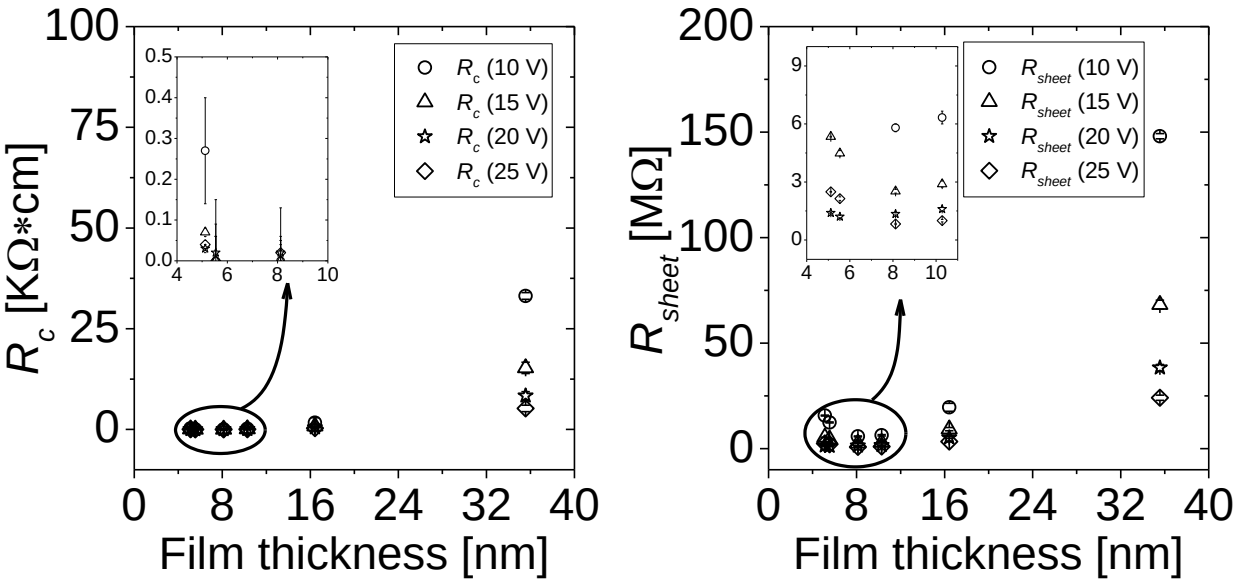

Figure 51. Contact and sheet resistance as a function of semiconductor film thickness of and applied gate voltage to the indium oxide TFTs fabricated with the indium oxoalkoxide in methoxyisopropanol formulation.

A comparison with Figure 39 which contains the respective data for the $In(NO_3)_3 \cdot H_2O$ precursor solution shows that the contact resistance of the oxoalkoxide system is just as low as of the nitrate based films, indicating high quality ohmic contacts. The sheet resistance appears to be only slightly higher for the oxoalkoxide based material, which could be attributed to the presence of carbon contaminants from the alkoxide chains, since both formulations had the same solvent.

The same analysis was performed on the TFTs fabricated with the THFA formulations. The extracted resistance values were plotted against film thickness for different gate voltages in Figure 52.

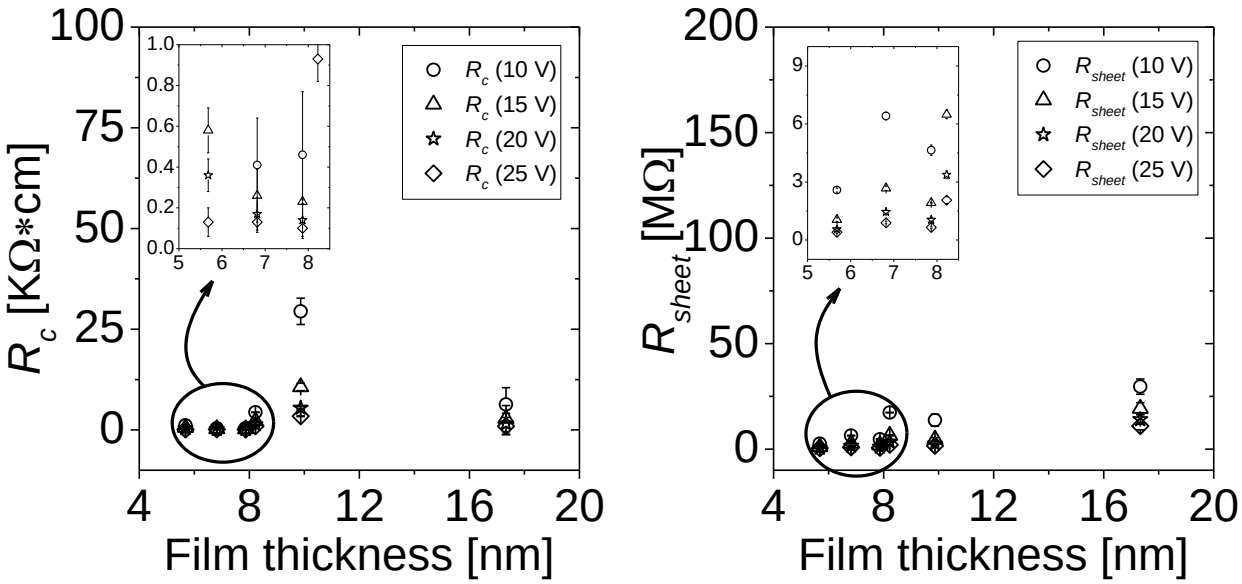

Figure 52. Contact and sheet resistance as a function of semiconductor film thickness of and applied gate voltage to the indium oxide TFTs fabricated with the indium oxoalkoxide in tetrahydrofurfuryl alcohol formulation.

The THFA system appears to result in larger contact resistance compared to the MIPA formulations. This might be caused by the higher spin coating speed used for semiconductor deposition, which could strain the films at the source/drain contacts.

The sheet resistance however has comparable values to the other oxoalkoxide system, indicating that the resulting films are essentially equivalent. Following the rationale from section 5.2.2. on the dependence of the reciprocal sheet resistance on conductive channel thickness, $1/R_{sheet}$ was calculated for both indium oxoalkoxide systems and plotted against film thickness h for different gate voltages in Figure 53.

Figure 53 a) shows the data extracted from the TFTs fabricated with the MIPA formulation. Regardless of the gate voltage, when the film thickness was below 10 nm, the inverse of the sheet resistance increased linearly with h, in very good agreement with the predicted behavior. Above 10 nm $1/R_{sheet}$ dropped rapidly, best described by a power law, e.g. $1/R_{sheet} = ah^b$, just like in the case of the $In(NO_3)_3{\cdot}H_2O$ solutions. Both linear and nonlinear regions of the graphs were fitted with the corresponding functions, and the points

were these intersected fell on a straight line, assumed to correspond to the thickness of the conductive channel.

The shape of the $1/R_{sheet}$ vs. h curves in Figure 53 a) resembles closely the relationship of the mobility with film thickness shown in Figure 50 a). However the attempt to fit the data with the lognormal distribution function failed, resulting in a low correlation.

Unfortunately the lack of data from very thin layers deposited from the indium oxoalkoxide in THFA formulation rendered this analysis inapplicable, as in the case of the nitrate system. All values of the reciprocal sheet resistance appeared to decay with film thickness over the entire range of h values (Figure 53 b). This could mean that the conductive channel in this material was thinner than (5.7 ± 0.5) nm.

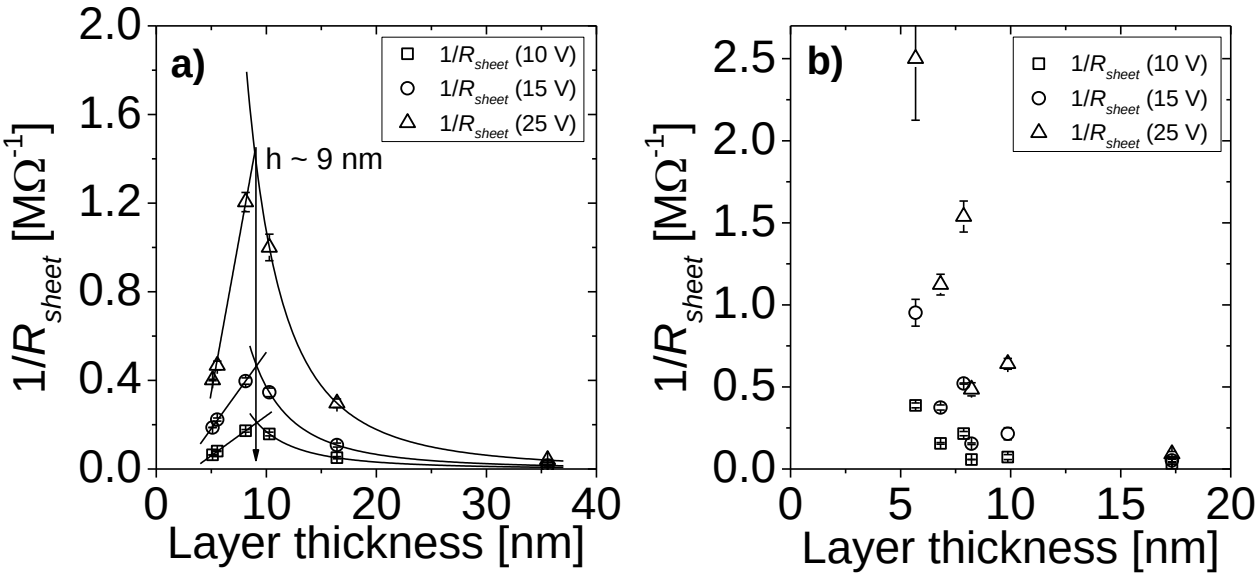

Figure 53. The dependence of the reciprocal sheet resistance on the active layer film thickness of the indium oxide based TFTs fabricated with the indium oxoalkoxide in methoxyisopropanol a) and in tetrahydrofurfuryl alcohol b) formulations.

5.3.4. Electrical stability

The electrical stability of the oxoalkoxide formulations was also tested similarly to the $In(NO_3)_3{\cdot}H_2O$ in MIPA solution. The TFTs fabricated with the formulations having the optimal concentration of the oxoalkoxide and with the corresponding spin coating parameters were passivated and then subjected to NBTS and PBTS measurements at 60°C in air.

The transfer characteristics of the stressed TFTs based on the MIPA formulation are presented in Figure 54. Compared to the transfer characteristics of the $In(NO_3)_3{\cdot}H_2O$ based

TFTs, the shifts of the threshold voltage in both positive and negative directions larger for the oxoalkoxide in MIPA system. The NBTS conditions caused the U_{th} to shift by 4 V into the negative direction, while the PBTS conditions shifted U_{th} by almost 6 V into the positive direction. These values are two times larger than those obtained with the $In(NO_3)_3 \cdot H_2O$ based TFTs (Figure 44).

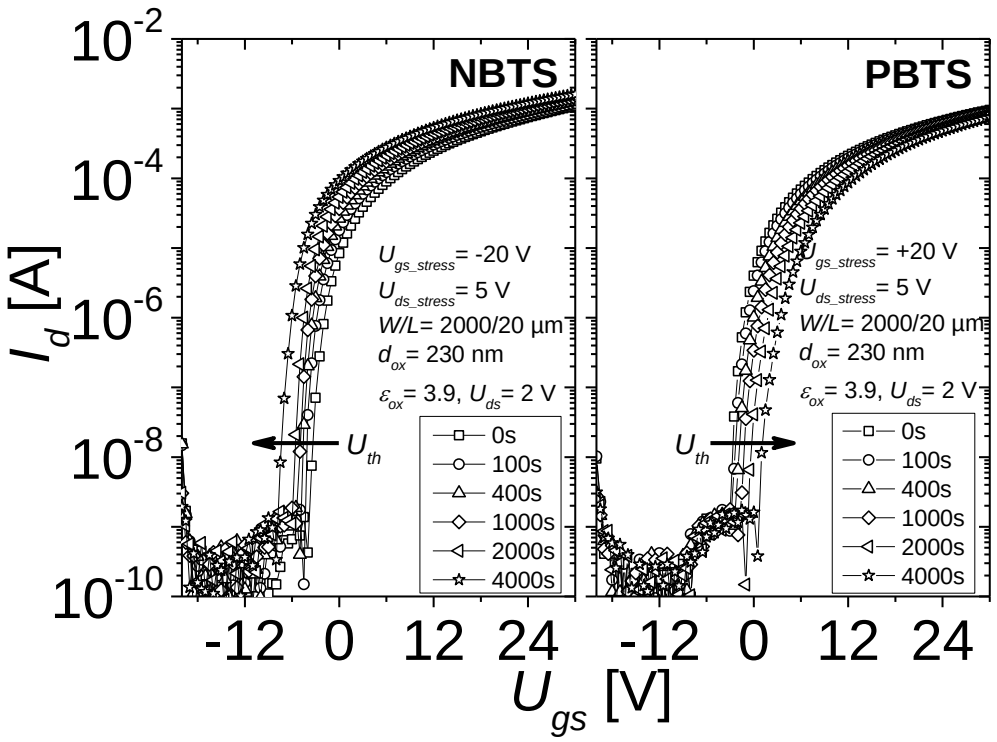

Figure 54. Transfer characteristics, stress parameters and structural information of the TFTs subjected to the NBTS and PBTS conditions (oxoalkoxide in methoxyisopropanol as semiconductor formulation).

The extracted from the transfer characteristics figures of merit were summarized in Figure 55. Worth taking notice of is the fact that after passivation, the charge carrier mobility almost doubled for the indium oxoalkoxide in MIPA formulation. In comparison there was almost no change (or even a decrease) in mobility registered for the $In(NO_3)_3 \cdot H_2O$ in MIPA based TFTs. The magnitude of this effect shows how important the surface of the semiconductor exposed to the atmosphere is for good functionality. A smooth surface has fewer defects that need passivation, as a result the change between a passivated and a nonpassivated sample is not large. A rough sample however, having a much larger surface exposed to the atmosphere, can be strongly improved via passivation of surface defects.

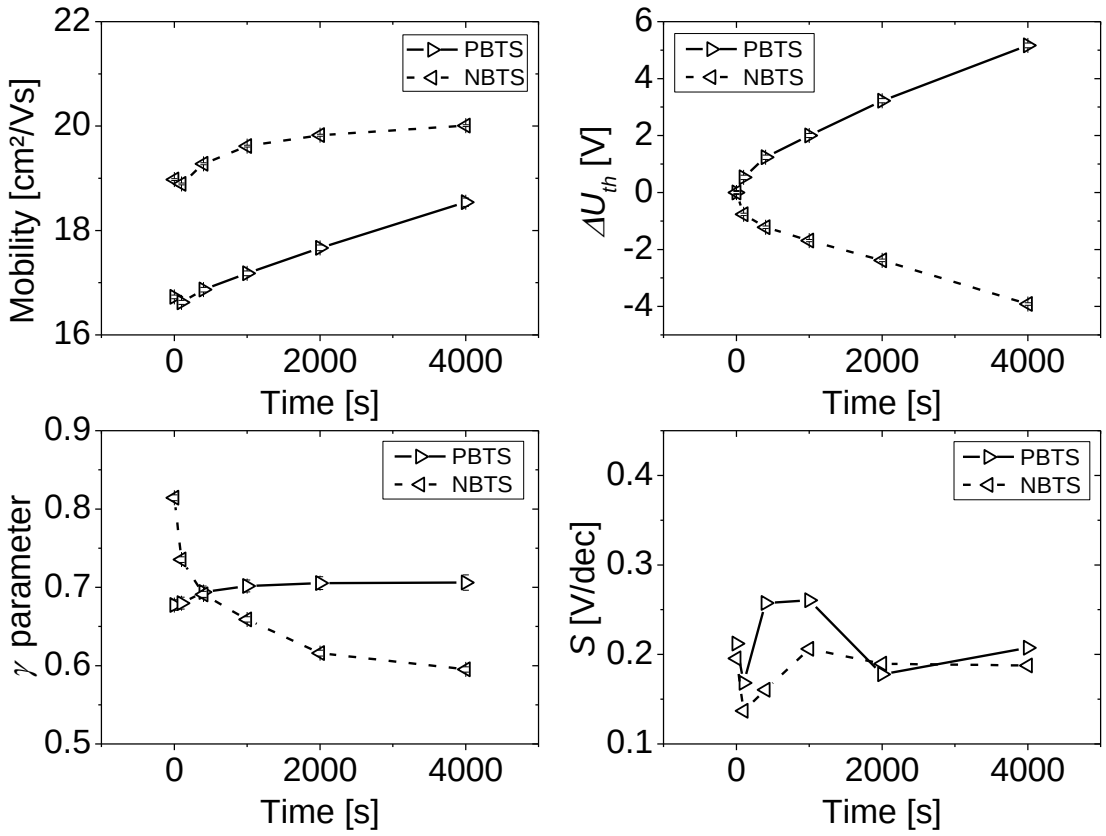

Figure 55. Figures of merit extracted from the transfer characteristics of the TFTs subjected to PBTS and NBTS conditions (oxoalkoxide in methoxyisopropanol as semiconductor formulation).

The results of the NBTS and PBTS measurements conducted on the TFTs fabricated with the oxoalkoxide in THFA formulation were grouped in Figure 56 and Figure 57. The stressed TFTs show a very good stability; the threshold voltage shifted by less than 2 V in either direction regardless of the stress conditions.

The insignificant improvement in mobility fits the correlation between surface roughness and performance improvement via passivation discussed above. The values of the subthreshold slope show the same high quality semiconductor-insulator interface as the other oxoalkoxide formulation, while the lower γ parameter is an indicator that the current system has a smaller concentration of traps than the films based on the other oxoalkoxide formulation. However due to higher values of the γ parameters overall, the oxoalkoxide system appears to have less free charge, or more trap states, or both, in comparison to the indium nitrate system. This could be because of carbon contamination from side groups' residues, or because the oxoalkoxide derived films don't lose oxygen and form oxygen vacancies as readily as the nitrate based films.

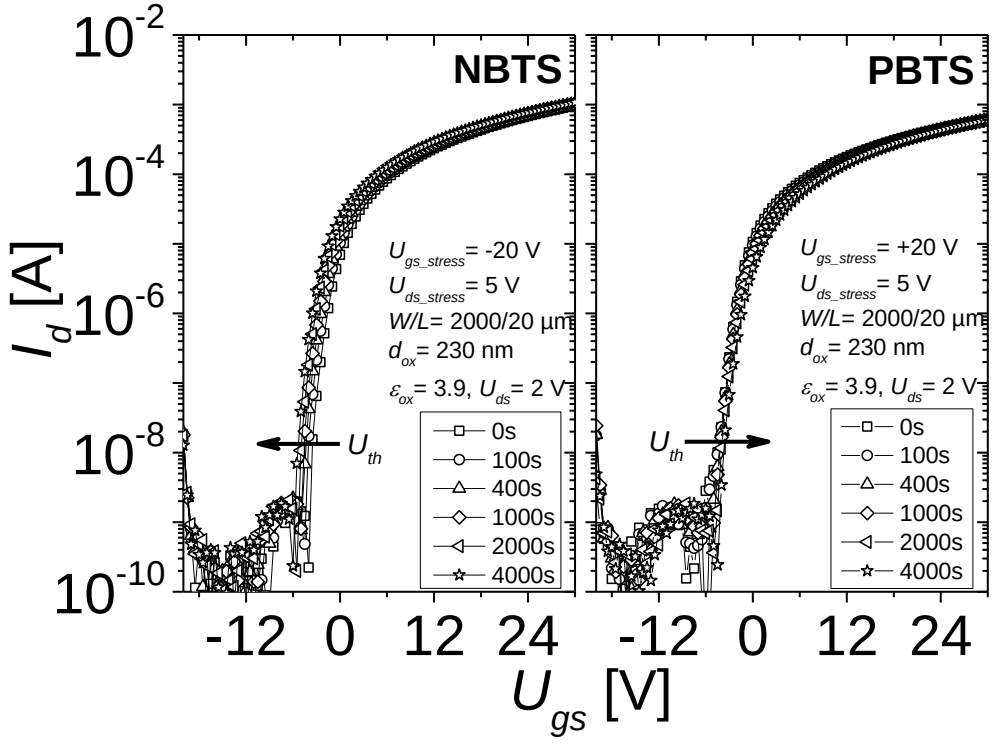

Figure 56. Transfer characteristics, stress parameters and structural information of the TFTs subjected to the NBTS and PBTS conditions (oxoalkoxide in THFA as semiconductor formulation).

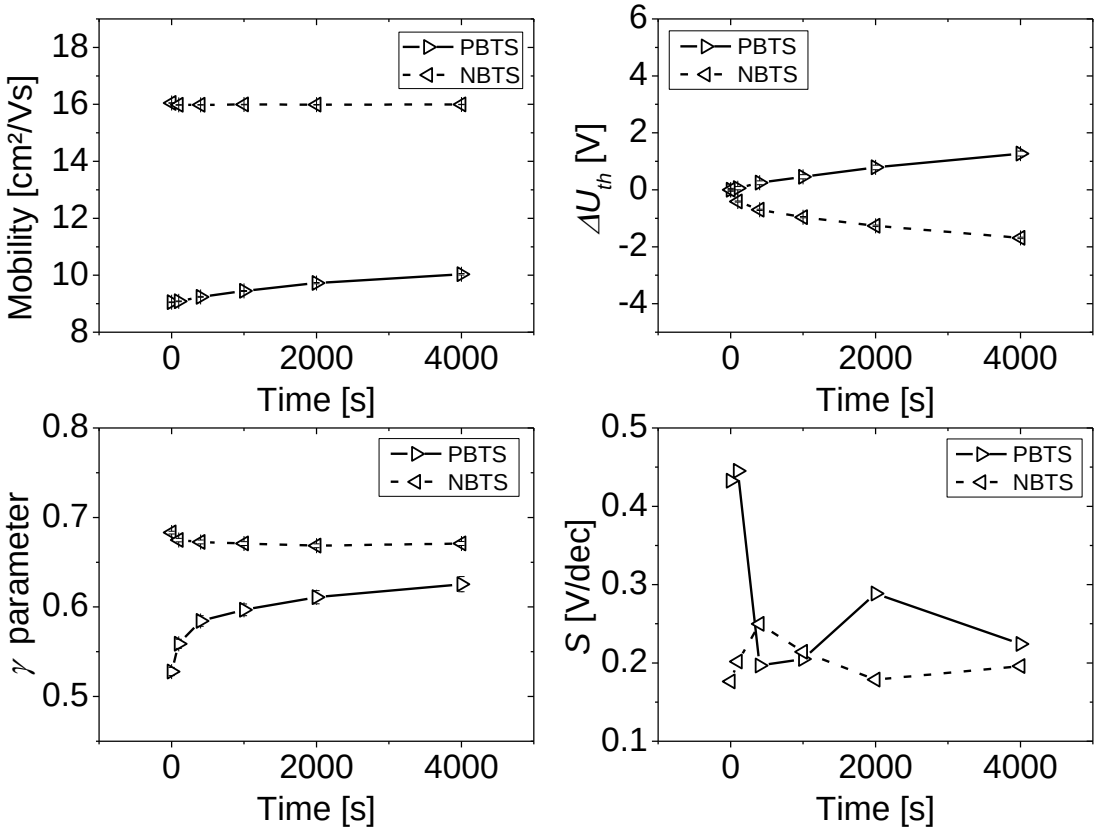

Figure 57. Figures of merit extracted from the transfer characteristics of the TFTs subjected to PBTS and NBTS conditions (oxoalkoxide in THFA as semiconductor formulation).

5.3.5. Charge transport mechanism

The temperature dependence of the figures of merit of the oxoalkoxide systems was measured with the same method applied to the TFTs based on the $In(NO_3)_3 \cdot H_2O$ in MIPA formulation. Firstly the samples were measured in the cryostat, in the temperature range from -133°C to 107°C in 15 degrees steps, in a nitrogen atmosphere. The recorded transfer curves were fitted with the gate-voltage-dependent mobility model and the extracted parameters were summarized in Figure 58 (the MIPA formulation based TFT) and Figure 59 (the THFA formulation based TFT). Next TFTs fabricated with both oxoalkoxide solutions were measured in ambient atmosphere in the temperature range from 21°C to 223°C in 7 degrees steps. The extracted data from the measured transfer characteristics were summarized in Figure 61 (the MIPA formulation based TFT) and in Figure 62 (the THFA formulation based TFT).

5.3.5.1. Inert atmosphere measurements

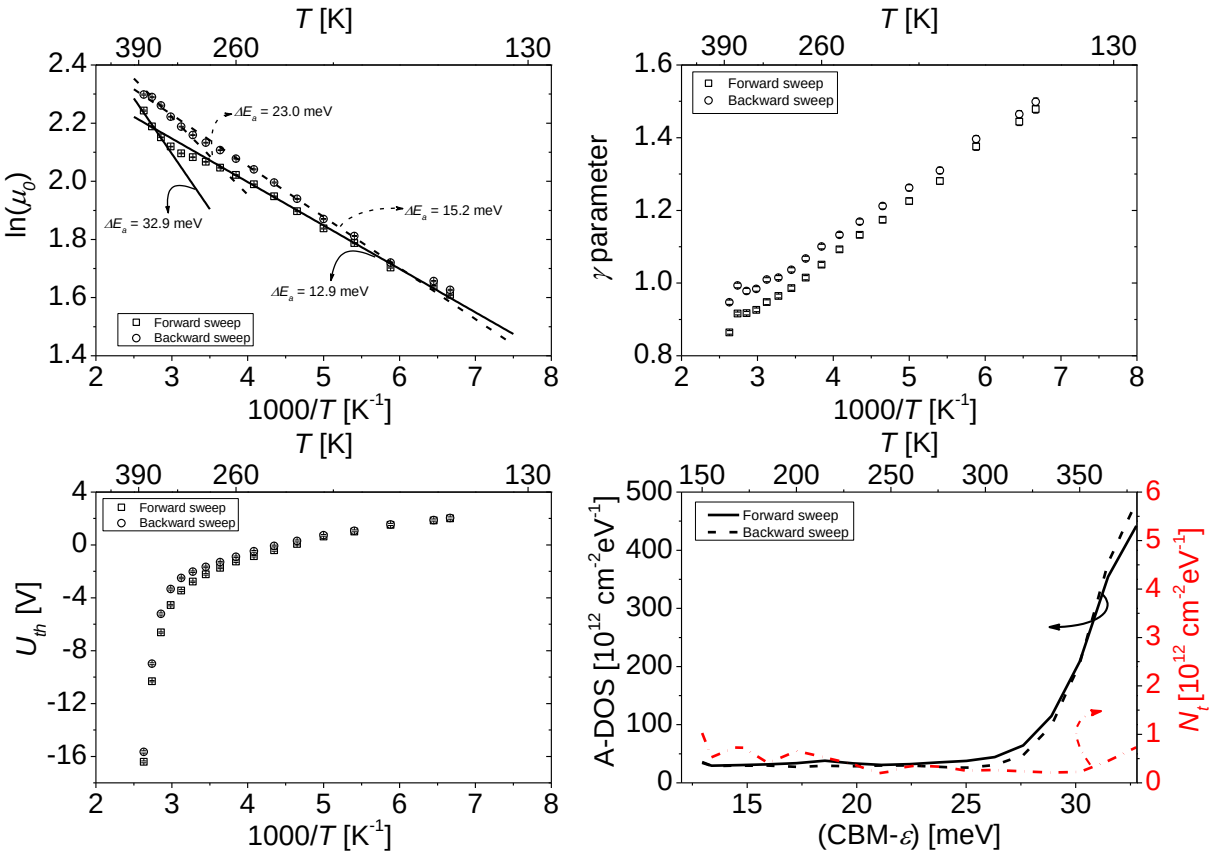

Figure 58. Temperature dependence of the figures of merit of a TFT fabricated with the indium oxoalkoxide in MIPA solution as semiconductor. Measurements performed in nitrogen.

The Arrhenius plots of the mobilities revealed a strong similarity between the oxoalkoxide samples and the $In(NO_3)_3 \cdot H_2O$ based TFT. All three systems appeared to have an inherent shallow energy level located between 12 meV and 15 meV, which influenced the charge carrier transport at temperatures around room temperature. This was reflected in the similar slope of the straight lines of dependence between $\ln(\mu_0)$ and $1/T$ up to about 60°C in all three cases. Above 60°C all three samples appeared to be affected by the same problem, there was a massive increase in charge carrier concentration with temperature, assumed to be caused by loss of oxygen atoms at the surface of the indium oxide exposed to the nitrogen atmosphere. This created an ultrathin metallic film on the surface of the semiconductor. It seemed that the used passivation could not prevent the formation of this metallic film. Since the conductive channel was as thick as the semiconductor film, the excess charge built up at the surface influenced the conduction, resulting in a fast increase in mobility, decrease in the γ parameter and strong negative shift of the U_{th} at temperatures above 60°C.

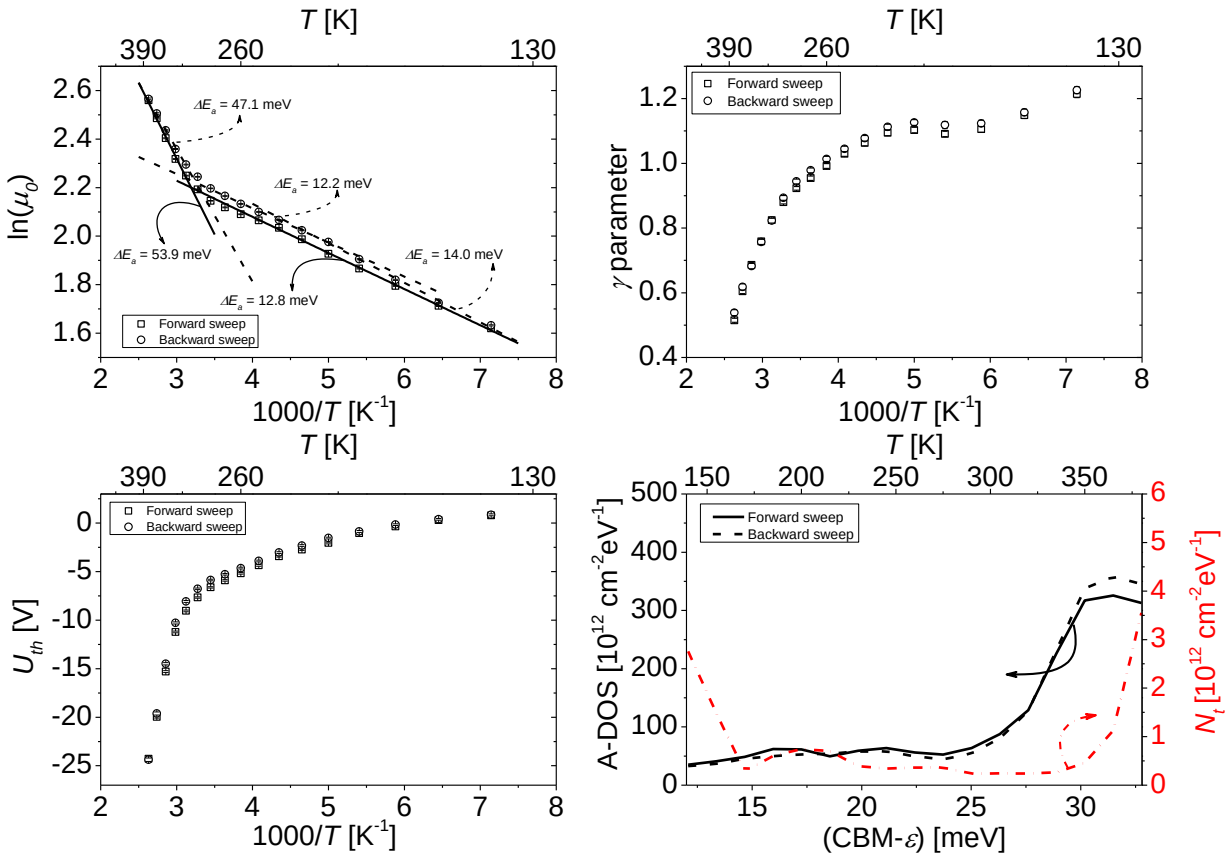

Figure 59. Temperature dependence of the figures of merit of a TFT fabricated with the indium oxoalkoxide in THFA solution as semiconductor. Measurements performed in nitrogen.

If one inspects the maximum U_{th} shift at the highest measurement temperature, then one notices that there is a correlation between film thickness and magnitude of the shift. More specifically, the further away from the semiconductor-insulator interface the metallic indium layer (the thicker the film), the smaller the magnitude of U_{th} shift. This was true for the entire temperature range, e.g. the thicker films appeared to be less susceptible to the influence of the surface of the conductive channel exposed to the surrounding atmosphere (Figure 60). This could be an important implication for sensor applications, meaning that in order to increase the sensitivity of the sensor one should decrease its conductive channel thickness.

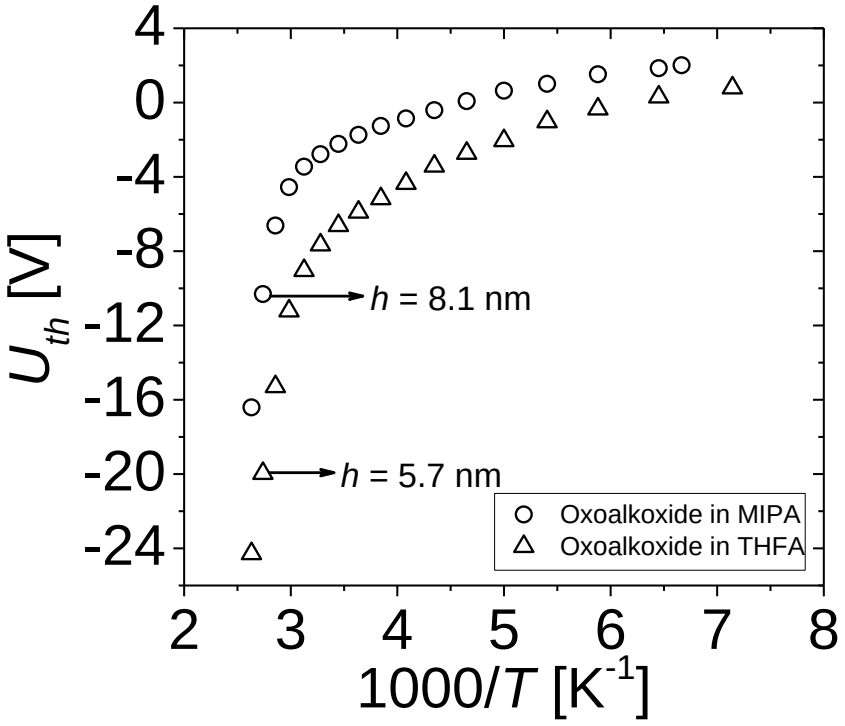

Figure 60. Negative shift of U_{th} with increasing temperature in a nitrogen atmosphere.

The rate of formation of surface oxygen vacancies was higher for the rough samples, such as the films deposited from the oxoalkoxide in MIPA formulation, which manifested itself in a more abrupt drop in U_{th} at higher temperatures. Surface defects favored the escape of oxygen from the film surface. As in the case of the $In(NO_3)_3 \cdot H_2O$ based films, the electrons remaining behind participated in conduction but the charged vacancies had a more pronounced trap character due to the defectuous film morphology, explaining why the rough samples also had a higher γ parameter compared to the other two systems.

Interestingly, the energy level of the surface oxygen vacancies became lower from $In(NO_3)_3 \cdot H_2O$ in MIPA (19.5 meV), to indium oxoalkoxide in MIPA (23 – 33 meV), to indium oxoalkoxide in THFA (47 – 54 meV), meaning that the formation of the vacancies became less favored in this order. The nitrate based films were considered to have fewer impurities in comparison to the other two systems, which might still contain carbon residues from their alkoxide groups. The C-O bond is stronger than the In-O bond [143]; therefore the oxoalkoxide based films retained more oxygen than the impurity-poor nitrate based films, while among the oxoalkoxides, the rougher film lost oxygen more readily compared to the smoother film.

The interfacial trap density calculated from the subthreshold slope was low and comparable in all three cases, indicating a good quality interface between the SiO_2 dielectric and the indium oxide film. Above 350 K (~80°C) the interfacial DOS of the oxoalkoxide in THFA based TFT appeared to increase several times, suggesting that new defects were being formed at increased temperatures, but the reason for this is unclear and might be the result of substrate surface contamination during sample preparation.

5.3.5.2. Ambient atmosphere measurements

The results of the temperature measurements conducted in air on the TFTs fabricated with the oxoalkoxide formulations also showed similarities with the $In(NO_3)_3 \cdot H_2O$ system. The discrepancy between the mobilities extracted from the forward and the backward swept transfer curves, especially the split of the mobility Arrhenius plots which started around 100°C appeared to indicate different charge transport mechanisms.

As in the case of $In(NO_3)_3 \cdot H_2O$ based TFTs, it was assumed that increasing the substrate temperature caused the generation of neutral oxygen vacancies. The generation process was promoted by temperature and intensified with its increase. The decreasing γ parameter in the forward sweep is evidence of a quickly increasing density of free charge in the conductive channel. This charge was swept away with the applied drain-source voltage, leaving the unshielded positively charged oxygen vacancies to act as traps. Due to the large amount of free charge, the conduction in the forward sweep appeared to be of the delocalized band transport type, since $dln(\mu_0)/dT^{-1} < 0$ [144]. The logarithm of the mobility extracted from the backward swept transfer curves increased with *T*, indicating a MTR type transport, with charges being trapped and released from the positively charged

traps. An additional argument to support this assumption was the increasing clockwise hysteresis with increasing temperature, corresponding to lower current levels in the backward sweep direction.

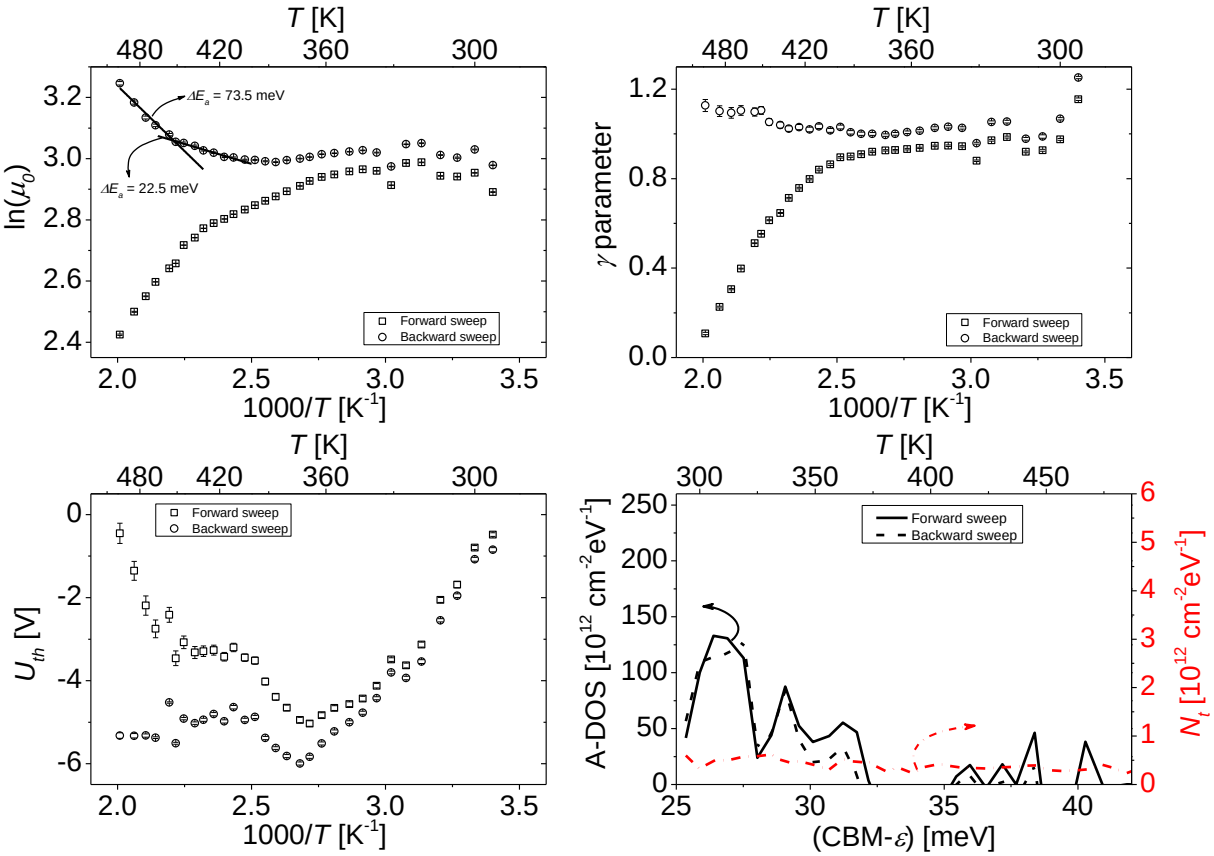

Figure 61. Temperature dependence of the figures of merit of a TFT fabricated with the indium oxoalkoxide in MIPA solution as semiconductor. Measurements performed in air.

As with other TFTs already characterized, the variation of the subthreshold slope in both systems was negligible, suggesting a temperature independent interfacial trap density; the low overall magnitude of the interfacial trap density indicated good quality semiconductor-insulator interface.

The areal density of states calculated with the adjusted optical method [52] again did not provide any conclusive data. In the case of the oxoalkoxide in MIPA based TFT this method elucidated the presence of a density of trap states at low temperatures, below 100°C, where the behavior of the γ parameter and mobility was relatively constant with respect to temperature. However, the peak at 300 K seemed to coincide with a sudden drop in the γ parameter, meaning a sudden increase in free charge density, which had no significant effect

on the charge carrier mobility, but was large enough to cause a continuous shift of U_{th} into the negative direction (Figure 61).

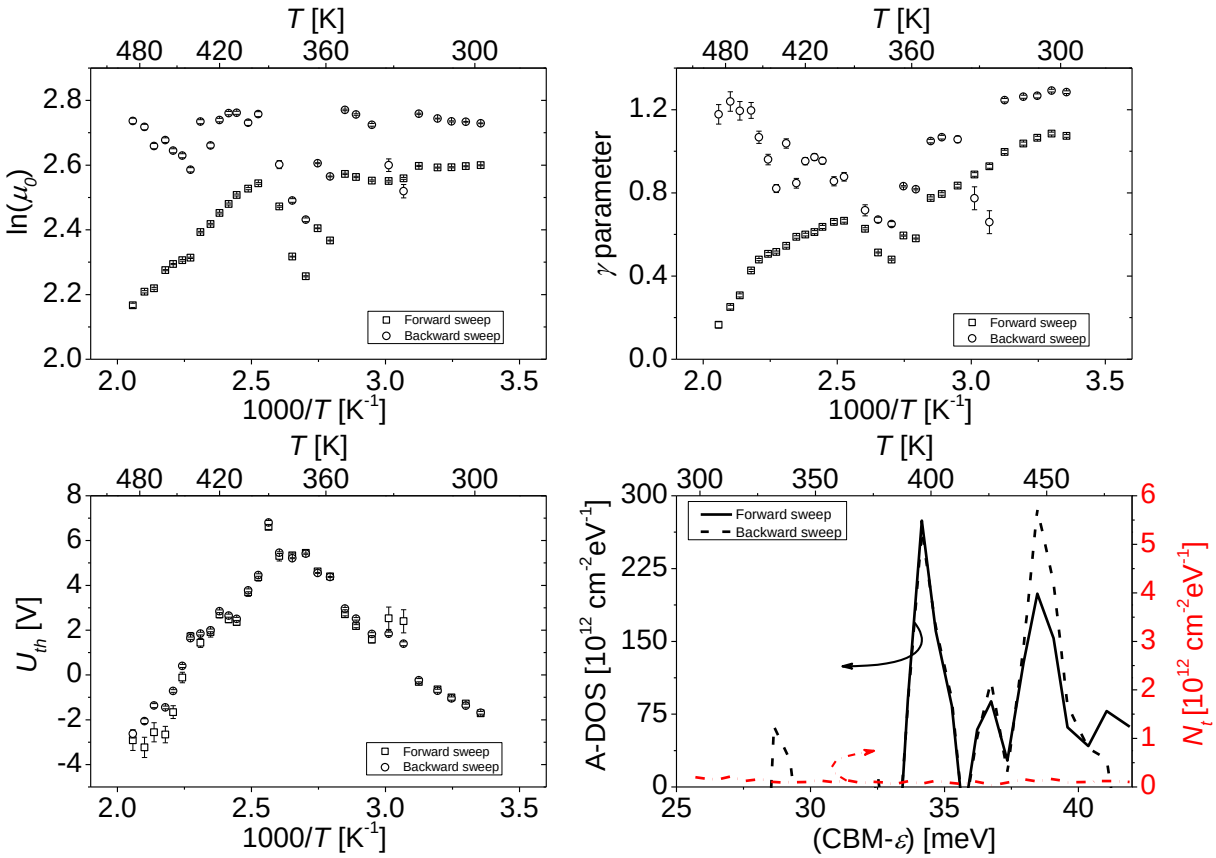

Figure 62. Temperature dependence of the figures of merit of a TFT fabricated with the indium oxoalkoxide in THFA solution as semiconductor. Measurements performed in air.

The areal density of trap states calculated with the same method for the oxoalkoxide in THFA based TFT showed an increased DOS at higher temperatures, mirroring again the negative slope of the dependence of U_{th} on temperature. Even though the γ parameter decreased over the entire temperature range, U_{th} shifted into the positive direction up to a temperature of 100°C after which it reversed its direction. A positive shift of U_{th} would mean a decrease in charge concentration, which contradicts the observed dependence of the γ parameter on temperature. Therefore the phenomena occurring below 100°C remain to this time without a plausible explanation.

5.3.6. Potential for a low temperature process

To complete the comparison of the indium oxoalkoxide with indium nitrate hydrate based formulations, some TFTs were fabricated at a maximum annealing temperature of 250°C.

Unlike the nitrate system, the oxoalkoxide solutions did not show a different performance on thickness dependence at a lower temperature. Also unlike the nitrate system, the oxoalkoxide films required a longer annealing time to increase the performance of the TFTs. After 1 h of annealing at 250°C the mobility of the TFT was slightly above 1 cm²/Vs, while a hysteresis larger than 10 V indicated an incomplete conversion of the precursor into the oxide film. As the annealing time increased, so did the performance of the TFTs. In Figure 63 one can see the recorded transfer curves of 4 TFTs annealed for 1, 2, 3 and 4 hours at 250°C respectively.

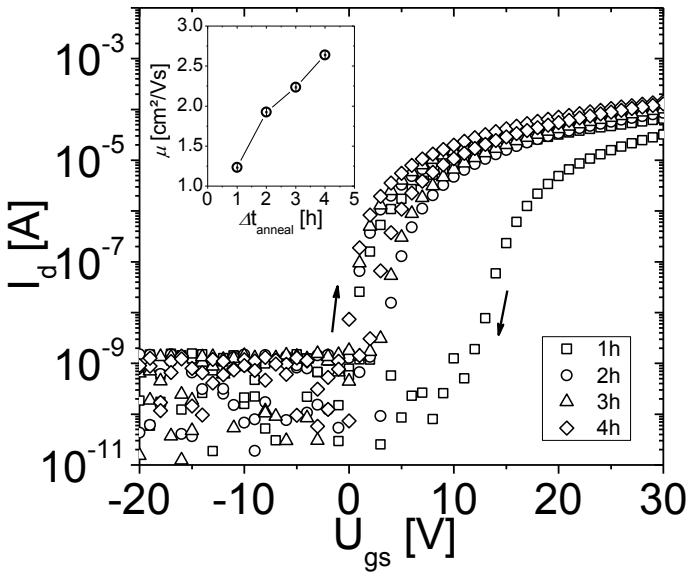

Figure 63. Transfer characteristics of TFTs with an indium oxoalkoxide based semiconductor thin film annealed at 250°C for different time spans. The measurements were made at U_{ds}= 2 V. The TFTs had the following structural parameters: W/L = 2000/20 µm, d_{ox}= 230 nm, ε_{ox}= 3.9.

The inset of Figure 63 illustrates the dependence of charge carrier mobility on annealing time at 250°C. After 4 hours of annealing it reached a value of 2.64 cm²/Vs, the hysteresis of the transfer curves decreased significantly, while U_{th} = 2.27 V, γ = 0.56 and S = 0.39 V/dec. These values are not as high as those obtained with an $In(NO_3)_3 \cdot H_2O$ based TFT, but the excellent stability of the oxoalkoxide material already enabled its application in device fabrication. For instance Rockelé *et al.* reported the fabrication of complementary circuits based on this material as n-type and pentacene for the p-type semiconductors [145].

6

Discussion

The aim of this work was to investigate the influence of the morphology of the semiconductor layer deposited from solution on the performance of the metal oxide TFTs. Initially a model system had to be chosen and after some consideration it was decided to focus on indium oxide as the material of interest, despite it being criticized in literature for the difficulty to control its charge carrier concentration and its poor stability. This decision was made based on the following reasons: the advantage of investigating a single cation system presents itself in the form of drastically reduced degrees of freedom of the material ensemble. The formulation of a stable multi-cation solution with a reasonable performance would be virtually impossible within the allotted time. The reason for that is the sheer multitude of available solvents and precursors with different solubility, reactivity and compatibility with one another. Even though in the last several years the research conducted on solution processable transparent oxide TFTs has surged, the reported data are as varied as the investigated systems.

Whenever scientific publications compare mixed solution based oxides among them or to indium oxide as reference material, the results show that combinations containing indium almost always perform better than those that do not; combinations with higher indium content most of the time perform better than those with less indium; and lastly the indium oxide reference samples most of the time perform better than any other mixed oxides processed under similar conditions (See Table 4 in Chapter 3.2).

It was shown here how important the chemistry of the precursor formulation is on the processability of the devices, starting with spin coating and up to the electrical characteristics. It is not only the solvent that has a direct impact on the film properties directly after deposition. It was seen that dissolving various precursors in the same solvent

can strongly change the properties of the formulation, such as viscosity or surface tension, which affect the wettability of the substrate and integrity of the spin coated film.

The choice of the material was made by testing the performance of various indium sources in a fixed solvent – methoxyisopropanol (MIPA) – and then screening a few other solvents with the same indium precursor. The best performance was obtained for 2 rather different indium precursors dissolved in MIPA: indium nitrate hydrate on the one hand, and an indium oxoalkoxide precursor synthesized at Evonik Industries AG on the other.

A strong dependence of the performance of the TFTs fabricated with $In(NO_3)_3 \cdot H_2O$ in MIPA on film thickness (*h*) was observed, which was varied via adjusting the concentration of the precursor in the semiconductor formulation. The mobility of the TFTs increased as *h* decreased and the reason was found when the surface was imaged with an atomic force microscope (AFM). The thick films had a particulate structure and large islands protruding through the surface of the films and surrounding craters which pierced the bulk of the semiconductor. As *h* decreased, so did the size of these islands until they eventually disappeared. As soon as the semiconductor layers became less than 10 nm thick, the islands disappeared and the films became smooth. The performance of the TFTs reached maximum values for a given fabrication process, showing how important a uniform and defect free semiconductor film is for good switching characteristics.

The optimal performance of the oxoalkoxide in MIPA was similar to that of the $In(NO_3)_3 \cdot H_2O$ based TFTs, but the film morphology was completely different, and the dependence of the figures of merit on it was also different. Unlike $In(NO_3)_3 \cdot H_2O$ films, the oxoalkoxide formulation resulted in rough films, with a grainy structure. The grains decreased in size as the films got thinner, but never actually disappeared. The films with the best performance still had a roughness two times larger than that of the $In(NO_3)_3 \cdot H_2O$ based films. And yet the performance was similar.

The dependence of the mobility on *h* was well described by a lognormal distribution. This meant that for this system, the mobility depended exponentially on a quantity normally distributed over the film thickness. Usually the mobility's temperature dependence is described as an exponential of negative activation energy of the charge carriers confined in trap states of various origins [31]. These trap states could be either energy wells [29] or barriers [30]. Given the grainy morphology of the semiconductor films obtained from the

oxoalkoxide in MIPA formulation, it is sensible to assume that the nature of the activation energy in this particular system stems from formation of grain boundaries.

Assuming that the activation energy, on which the mobility depends exponentially, is the sum of the contributions of all grain boundaries, this energy would be large for a few badly packed grains due to the high barrier of the individual boundaries (thick film scenario), as well as for a large number of small but well packed grains due to their quantity (thin film scenario). For a film of an intermediate thickness the number of the grains and the barrier height of their boundaries would both be small enough to result in a minimum activation energy value. Therefore, the negative activation energy would be normally distributed over *h*, validating the lognormal distribution of the mobility values over the range of film thickness.

In spite of the mediocre surface quality of the semiconductor film, the TFTs fabricated with the indium oxoalkoxide from Evonik Industries AG formulation showed a mobility of 9.65 cm^2/Vs, similar to the $In(NO_3)_3 \cdot H_2O$ in MIPA performance with a μ_0 = 9.78 cm^2/Vs. Both devices were processed in ambient atmosphere and annealed for 1 hour at 350°C. In comparison to these results, Kim *et al.* managed to fabricate In_2O_3 based devices via a combustion process at 325°C with a mobility of 9.4 cm^2/Vs, while at 400°C the same system and no combustion annealing reached a μ_0 of only 5.92 cm^2/Vs [112].

Banger *et al.* reported mobilities of 7-12 cm^2/Vs for TFTs fabricated at temperatures of only 230-275°C, with a mixture of indium isopropoxide in MIPA and zinc-*bis*-methoxyethoxide in 2-methoxyethanol in a “sol-gel on chip” process [21]. Hwang *et al.* used post-humid annealing to fabricate TFTs with AlInO as semiconductor which showed a mobility of 13.4 cm^2/Vs at 350°C annealing temperature [111].

The results reported in this work, however, were obtained from TFTs with a coplanar bottom gate architecture, which is known to deliver inferior performance compared to the staggered top contact configuration employed by most of the authors. Using a thinner high-k insulator instead of the 230 nm thermally grown SiO_2 and a smaller *W/L* ratio than 100[2] could improve the performance of the TFTs based on the currently researched systems further.

[2] The numbers indicate the values of the respective device parameters used in the current work

Nevertheless, the performance of the indium oxoalkoxide still had the potential to be increased by improving its film quality, if the thesis presented here is true. Indeed, after changing the solvent of the semiconductor formulation from MIPA to tetrahydrofurfuryl alcohol (THFA), the surface of the spin coated films became very smooth and independent on the thickness of the films. The solubility of the oxoalkoxide in THFA is lower than in MIPA and the stock solution was not concentrated enough to allow film thickness variation via dilution series as in the case of the other formulations, therefore the thickness of the semiconductor films was varied by means of the spin coating speed and the resulting thickness range was smaller.

With the improvement of the semiconductor layer morphology, the mobility of the TFTs improved by 50%, reaching 15.12 cm^2/Vs under the same fabrication conditions as the other investigated devices for a film of 5.7 nm thin. The dependence of the mobility on film thickness could also be fitted with a lognormal distribution, but the difficulty of resolving films thinner than 5 nm led to the lack of data in that region. Without that data, several other equations describe the μ_0 vs. h dependence fairly well, such as an exponential or a power law. The similarity of the material system (with the oxoalkoxide in MIPA) speaks in favor of the lognormal dependence, but the similarity of the film morphology with the nitrate based system, which does not show the lognormal dependence of μ_0 vs. h, speaks against it. At any rate, finding a plausible explanation for the observed behavior proved difficult.

Both material types, indium nitrate hydrate and indium oxoalkoxide have shown a formidable performance when processed at 250°C. After one hour of annealing on the hot plate, in ambient atmosphere, the TFTs with the semiconductor layer deposited from the $In(NO_3)_3 \cdot H_2O$ formulation displayed a mobility of 4.61 cm^2/Vs, while the threshold voltage was at 0.18 V and subthreshold slope was 0.26 V/dec. Surprisingly though, the peak performance of the TFTs shifted to thicker semiconductor layers, and despite the smooth films, the thinner layers performed worse than the thicker ones. Nevertheless, the mobility value reported here is among the highest reported so far in scientific literature considering the sample architecture and simplicity of the fabrication process.

The indium oxoalkoxide based TFTs retained their film thickness dependence of the performance but scored lower than their nitrate counterparts. One hour at 250°C did not

conclude the conversion of the precursor into indium oxide, which could be seen in the large hysteresis of the transfer curves. As the duration of the annealing step increased, so did the quality of the semiconductor. The hysteresis decreased substantially and after 4 hours on the hot plate the TFTs showed the following performance: μ_0 = 2.64 cm²/Vs, U_{th} = 2.27 V, and S = 0.39 V/dec. The fact that the oxoalkoxide based semiconductor layer performed much better than the nitrate system at 350°C, but showed a lower performance at 250°C, underlines the importance of tailoring the semiconductor formulation to a given process. The side groups of the oxoalkoxide material that can be easily removed out of the film at 350°C to result in a high quality semiconductor present a challenge at 250°C. They probably remain in the film in relatively large amounts, disrupting its uniformity and acting as impurities or scattering centers. At lower temperatures the facile decomposition of the nitrate cations [127] is a definite advantage.

The morphology of the semiconductor films however has implications far more diverse than just being an indicator of the quality of the active layer. It is true that a dense, defect free semiconductor is necessary for a good TFT performance, but the quality of the interfaces it forms with the insulator and contacts is of equal importance. The surface roughness of the semiconductor mirrors the density of the bulk of the film [125], [146], responsible for the resistance of the conductive channel (R_{ch}), as well as the profile of the surfaces adherent to the gate insulator and contacts, the latter being responsible for the contact resistance (R_c). R_c affects the injection and extraction of charge into and out of the conductive channel, and is therefore crucial for a qualitative operation of the TFTs. It eventually influences the decision of what material to use as source and drain contacts in order to optimize the TFT's performance.

In spite of the importance of the channel and contact resistances in the operation of TFTs, data on the behavior of these parameters among solution processed metal oxide TFTs are scarce. Reports on sputtered a-IGZO films place the width normalized contact resistance in the interval from several tens to several hundreds of Ω·cm [134], [147], while the channel resistance is in the order of MΩ [135].

Resistance values very close to the ones reported in literature were extracted by applying the transfer line method (TLM) [47] to the TFTs fabricated with each of the 3 material systems discussed here. The values of the extracted contact and sheet resistance from the

TFTs with the best performance fabricated with each formulation are summarized in Table 13. The data were calculated at U_{gs}= 25 V.

Even though the TFTs were fabricated in a bottom gate – bottom contact configuration, the deposition of the semiconductor via spin coating lead to the formation of high quality contact interfaces between the semiconductor and source-drain electrodes, which resulted in contact resistance values lower than those reported for IGZO devices with top contacts [134], [147]. This demonstrates that ITO is a compatible electrode material for the semiconductor resulting from the investigated formulations.

Table 13. Contact and sheet resistance of the TFTs fabricated with the indium nitrate and oxoalkoxide formulations as a function of film thickness and roughness.

Semiconductor formulation	R_c [Ω·cm]	R_{sheet} [MΩ]	h [nm]	S_{rms} [nm]
$In(NO_3)_3 \cdot H_2O$ in MIPA	20 ± 20	0.50 ± 0.04	6.4 ± 0.2	0.44
Indium oxoalkoxide in MIPA	20 ± 20	0.83 ± 0.03	8.1 ± 0.4	1.56
Indium oxoalkoxide in THFA	130 ± 70	0.40 ± 0.06	5.7 ± 0.5	0.47

The higher contact resistance apparent for the oxoalkoxide in THFA precursor might be due to the high spin coating speed which could have pressed the film against one electrode, while creating a gap between the film and the other electrode, opposite to the centripetal force. This gap would then be responsible for a deteriorated injection and thus a higher contact resistance.

The large uncertainties of the calculated contact resistance were caused by the fact that the TFTs with various channel lengths were not identical morphologically and in addition the small channel length TFTs might have been (and usually are) affected by short channel effects. The uncertainties become particularly large if the contact resistance has a small value, as in this case, because of the low resolution of the TLM for such values.

The sheet resistance however is higher for the oxoalkoxide in MIPA based active layer, in perfect agreement with the postulated dependence on the overall morphology of the films. The smooth films have a higher quality of the bulk of the film as well, which lowers the sheet resistance of the material. The rough film resulting from the oxoalkoxide in MIPA formulation has a higher concentration of defects within itself, in the form of grain

boundaries or even empty spaces between the grains, making the film more resistive to charge transport.

The rough semiconductor film also proved to be less stable to an applied gate bias stress. According to Conley J. F., electrical stressing of a TFT is responsible for the following instability inducing phenomena: defect creation within the conductive channel and charge trapping at the semiconductor-insulator interface [9]. The less optimal morphology of the oxoalkoxide in MIPA based film is likely to be more susceptible to these phenomena than the other two semiconductor formulations. The effect is even direr because it is considered that all 3 films have a conductive channel as thick as the film itself, meaning that the surfaces of the films are part of the channels and exerts a strong influence on the conduction.

It is not easy to compare stability data with published literature, mainly because of the variety of parameters that are varied during the stress measurements. These range from structural information of TFTs, to atmosphere properties in which the stressing took place, to whether the TFTs were passivated or not and whether the measurements were conducted under illumination or in the dark and most importantly, the magnitudes and duration of the applied biases [9], [101].

In this work the passivated TFTs were stressed in the dark, in ambient atmosphere at a temperature of 60°C, for 4000 s. The drain-source voltage in all cases was equal to 5 V and the gate voltage was -20 V for the NBTS conditions and +20 V for the PBTS conditions. Table 14 summarizes the magnitudes of the threshold voltage shifts for each TFT under each stress condition.

Table 14. Threshold voltage shifts of the TFTs fabricated with various indium precursors under positive and negative temperature bias stress conditions. The TFTs were stressed for 4000s at 60°C with Uds= 5 V and Ugs = ±20 V, depending on the stress conditions.

Semiconductor formulation	ΔU_{th} PBTS	ΔU_{th} NBTS	h [nm]	S_{rms} [nm]
$In(NO_3)_3 \cdot H_2O$ in MIPA	+2 V	-3 V	6.4 ± 0.2	0.44
Indium oxoalkoxide in MIPA	+5.5 V	-4.5 V	8.1 ± 0.4	1.56
Indium oxoalkoxide in THFA	+1.5 V	-1.5 V	5.7 ± 0.5	0.47

The less smooth semiconductor film fabricated from the indium oxoalkoxide in MIPA formulation showed larger shifts of U_{th} under both stress conditions, while the other two formulations resulted in TFTs with very good bias stress stability.

For a long time the instability of the metal oxide TFTs has been attributed to the generation of oxygen vacancies within the semiconductor films, which increased the charge carrier concentration or acted as traps and by that caused the shift of the threshold voltage during bias stressing [101]. Medvedeva and Hettiarachchi calculated the energetic positions of oxygen vacancies in bulk metal oxide semiconductors, including indium oxide, and showed that normally the formed oxygen vacancies are neutral from an electrical point of view, and are located so deep within the band gap, that they cannot influence the conduction mechanisms of the semiconductors [141]. In order for an oxygen vacancy to interfere with charge transport, it has to become ionized, process which requires an amount of energy which cannot be supplied thermally or by the bias voltages commonly applied during stressing. Once again, these calculations describe oxygen vacancies in the bulk of the metal oxide, where they are stabilized by their environment.

In this work the temperature dependence of the charge carrier mobility was used to evaluate the position of shallow trap states, if any, within the band gap of the semiconductors under investigation. The measurements were conducted in the temperature range from -133°C to 203°C, but due to limitations of the measurement setups, the full temperature range had to be split in two and the measurements conducted with two different setups.

The low temperature region spanned the interval from -133°C to 107°C. The measurements were conducted inside a cryostat cooled with liquid nitrogen. The TFTs themselves were kept in a nitrogen atmosphere over the duration of the experiment. All three semiconductors revealed an almost perfect linear Arrhenius plot of the mobility's natural logarithm against reciprocal temperature, out of which a shallow trap level located between 12 and 15 meV was found. This level was present in all TFTs fabricated with each of the three formulations. Above 60°C however, each TFT presented an abrupt and strong increase in carrier concentration. It was assumed that this increase was caused by a sudden activation of oxygen vacancy generation due to the non-equilibrium created at the interface of the metal oxide and the oxygen deficient nitrogen atmosphere. Because of the inability of

the metal oxide to stabilize these surface vacancies like in the bulk of the semiconductor, their energy could be much higher than that of the bulk vacancies, and their ionization energy much lower. In this way the phenomena observed above 60°C in a nitrogen atmosphere could have a plausible explanation.

In addition, the energy level of the newly formed oxygen vacancies varied among the three samples, being the lowest for the $In(NO_3)_3 \cdot H_2O$ sample, ΔE_a= 19.5 meV, and highest for the indium oxoalkoxide in THFA based TFT, 47 meV < ΔE_a < 54 meV. The variation of this energy level could be attributed to the readiness of each film to lose oxygen atoms from the surface and generate the oxygen vacancies.

Presumably, the nitrate based film does not have any leftover residues of the anions (assuming for the sake of the discussion that the solvent evaporates entirely). The strength of the indium-oxygen bonds at the surface of the semiconductor determines how easily the oxygen atoms will escape. Take the next formulation, indium oxoalkoxide in MIPA. It is very likely that the film is contaminated by carbon impurities from the alkoxide groups of the precursor which bind random oxygen atoms as well. Carbon-oxygen bonds are stronger than the indium-oxygen bonds [143], therefore the oxygen vacancy activation will be lower compared to the nitrate based film, but not much lower. The rough surface of the semiconductor introduces structural defects at the peaks of or valleys between the grains, which could favor the escape of oxygen atoms from the surface. The smooth surface of the third type of film in combination with the assumed carbon impurities stabilize somewhat the surface of the semiconductor, lowering the activation energy of the oxygen vacancies more in comparison with the other two systems.

Table 15. Activation energy of the oxygen vacancies formed at the surface of the semiconductor in a nitrogen atmosphere at elevated temperatures and the magnitude of the induced charge concentration depending on the precursor formulation.

Semiconductor formulation	ΔE_a of V_o [meV]	Induced charge [10^{14} $cm^{-2}eV^{-1}$]	*h* [nm]	S_{rms} [nm]
$In(NO_3)_3 \cdot H_2O$ in MIPA	19.5	2.8	6.4 ± 0.2	0.44
Indium oxoalkoxide in MIPA	23 - 33	4.5	8.1 ± 0.4	1.56
Indium oxoalkoxide in THFA	47 - 54	3.3	5.7 ± 0.5	0.47

The calculated induced charge density resulting from the threshold voltage shift rate at the maximum measurement temperature (107°C) also supports the argument that the smoother films are less likely to lose the oxygen from the surface than the rough film (Table 15).

Because of the limitations of the measurement setup and additionally due to the large shift of the threshold voltage into the negative direction in an oxygen deficient atmosphere above 60°C, higher temperature measurements had to be conducted in ambient atmosphere on a hot plate. The measurements in air were conducted in the temperature range from 21°C to 203°C, having a large overlap with the measurements conducted in nitrogen, for comparison.

Because of the change of the atmosphere, the behavior of the TFTs with increasing temperature change considerably. The generation of oxygen vacancies above 60°C was not completely suppressed, but shifted beyond 100°C. The energy level between 12 and 15 meV registered in all three samples in the nitrogen atmosphere measurements was not seen anymore. Instead, the extracted activation energies were much deeper, suggesting that the presence of oxygen in the surrounding atmosphere had a stabilizing effect on the TFT.

Remarkably, there was a difference in charge carrier mobility behavior with increasing temperature depending on the direction of the gate voltage sweep. When the gate voltage was swept forward, from -20 to +30 V, the mobility extracted from the transfer curves appeared to indicate a delocalized band transport mechanism, in which the mobility is known to decrease with increasing temperature, being limited by phonon scattering [148].

On the other hand, mobilities extracted from backwards swept transfer curves indicated a thermally activated or multiple trap and release type of charge transport, except for the indium nitrate system, whose mobility kept decreasing with temperature even in the backward sweep. The split in the Arrhenius plots appeared in all 3 cases around 100°C. This could probably mean that while the oxygen vacancies that were formed at the surface of the films in the nitrogen atmosphere above 60°C were already ionized, or could be ionized quickly during electrical measurements due to their shallow lying energy level, the oxygen vacancies formed in air were deeper and much slower to be ionized.

These results suggest that the formation of oxygen vacancies that would affect the charge transport of the TFTs fabricated with the formulations under investigation is not a concern for real device applications. Their formation appears to be activated above 100°C, temperatures out of reach of most of potential devices. In addition to these findings, the demonstrated electrical stability of TFTs measured in this work, their high charge carrier mobility and the simplicity of the TFT fabrication process, make these materials very attractive for real devices, despite the negative critique that indium oxide as a semiconductor receives in literature.

7

Summary & Outlook

A better understanding of the influence of the semiconductor layer morphology on the performance of solution processable indium oxide thin-film transistors was the focus of the research presented in this thesis. With that purpose, several suitable semiconductor solutions were formulated by dissolving various indium sources in methoxyisopropanol. When suitable precursor candidates were found, an attempt to improve film deposition and resulting morphology was made by varying the solvent of the formulations. These trials resulted in three formulations of interest: indium nitrate hydrate in methoxyisopropanol (MIPA), an indium oxoalkoxide from Evonik Industries AG in MIPA and the same indium oxoalkoxide in tetrahydrofurfuryl alcohol (THFA).

The TFTs were fabricated by spin coating the semiconductor formulations on bottom gate bottom contacts templates consisting of a highly doped Si wafer with 230 nm of thermally grown SiO_2 layer as gate insulator and source-drain electrodes consisting of 10 nm of ITO and 30 nm of gold on top of the ITO. Before semiconductor deposition the TFT templates were cleaned in a hot acetone and isopropanol (1:1) bath, rinsed with deionized water (di-water), blown dry with a nitrogen gun and exposed to an oxidizing environment in a UVO cleaner for 10 minutes. After spin coating the semiconductor the TFTs were annealed for 1 hour at 350°C, or for a specified amount of time at 250°C.

The electrical characterization of unencapsulated TFTs was performed in a glove box. The figures of merit were extracted from the measured transfer characteristics using a gate-voltage-dependent mobility model.

In order to investigate the influence of the active layer morphology on the TFT's performance, the thickness of the semiconductor layers was modified by varying the concentration of the indium precursor in the formulation. In the event that the stock formulation was not concentrated enough and further dilution led to extremely thin films

which didn't respond to a gate signal, the thickness of the films was modified by means of the spin coating speed.

The film thickness was measured either mechanically, with an atomic force microscope (AFM) or optically, with an ellipsometer. The surface of the films was imaged with the AFM. There was a strong correlation between film thickness and surface roughness observed. Generally the thicker films deposited from indium salts had a higher roughness, although above a certain threshold the films became smoother again. Oxoalkoxide in MIPA based films had a particulate surface, the semiconductor formed islands which decreased in diameter as the films became thinner, but never actually disappeared, as did the nitrate based films below a certain thickness.

The behavior of the charge carrier mobility with semiconductor layer thickness was found to be different for each material. The performance of the indium nitrate based TFTs increased as the film thickness decreased and oscillated around a maximum value which was reached as soon as the films became smooth. For films under 10 nm thick the charge carrier mobility reached almost 10 cm^2/Vs (9.78 cm^2/Vs for a 7.4 nm film) with a subthreshold slope of 0.46V/dec. The oxoalkoxide in MIPA system displayed an interesting dependence of mobility on film thickness, which appeared to look like a lognormal distribution. It rose to a maximum value of 9.65 cm^2/Vs with an S = 0.89 V/dec for a film of 8.1 nm thick, after which it decreased with film thickness. Considering that the transport mechanism of the metal oxide TFTs investigated in this work was a thermally activated one, which will later be supported by experimental evidence, one could conclude that the activation energy of the charge carriers was normally distributed over the range of film thickness. This assumption makes sense as long as the activation energy is viewed as the sum of the energy barrier heights which develop at the boundaries between the individual semiconductor islands.

It was seen that the size of the islands decreased with film thickness, which meant that their number increased and their packing improved. Thicker films had fewer but larger, worse packed islands with large total barrier energy. The total barrier energy of the thinner layers should also be large due to the sheer number of grain boundaries, in spite of their lower individual barrier height. Somewhere at intermediate film thickness the number and barrier height of the grain boundaries should both be small enough to result in a minimum

total energy. Thus the negative activation energy on which the mobility depends exponentially would have a normal distribution over the film thickness range.

The mobility of the TFTs fabricated with the oxoalkoxide in THFA formulation increased all the way to the thinnest semiconductor layer, reaching a performance of μ_0 = 15.12 cm²/Vs with S = 0.72 V/dec for a film of 5.7 nm. The experimental data was well fitted with a lognormal distribution as well. The absence of visible grains on the film surface however made it questionable whether the description of the dependence made sense for this material system, especially because the data could be just as well fitted with an exponential, a power law or a polynomial function. So far, a different plausible explanation for the observed mobility behavior has not been found.

The influence of the semiconductor film morphology on the contact and sheet resistance was also investigated. The data was collected via a two-point measurement method and evaluated with the *Transfer Line Method* (TLM). The transfer characteristics of transistors with different channel lengths were measured in the linear regime and then the total resistance was calculated by dividing the applied drain-source voltage (U_{ds}) by the measured drain current (I_d). Plotting the width normalized total resistance ($R_t \cdot W$) against channel length L, the data points could be fitted with first degree polynomials. Extrapolating the fit lines to L = 0, where the contribution of the channel resistance vanishes, the total width normalized contact resistance was obtained, with the units of Ω·cm. The slope of the lines yielded another parameter known as the sheet resistance, with units of Ω, which when multiplied by the geometry of the channel (L/W) results in the channel resistance.

The obtained values for sheet resistance were below 1 MΩ, which were below values reported in literature for other metal oxide systems [135]. The smooth films obtained with the indium nitrate in MIPA and indium oxoalkoxide in THFA solutions had a sheet resistance almost 2 times smaller than the rougher film resulting from the indium oxoalkoxide in MIPA formulation. This result demonstrated that the surface of a solution processed semiconductor mirrors the quality of the bulk of the film. Smooth films have less bulk defects and thus a lower resistivity.

On the other hand, the contact resistance of the two MIPA formulations were comparably small (20 ± 20 Ω·cm), also lower than reported values for metal oxides with metal contacts

[134], [147]. The contact resistance of the oxoalkoxide in THFA based TFT was somewhat larger (130 ± 70 Ω·cm), assumed to have been caused by the tension induced at the semiconductor-electrode interface opposite to the centripetal force direction arising in the spin coating process due to the large spin coating speed.

The viability of the tested semiconductor formulations for real applications was tested by applying a positive or negative bias temperature stress measurement for 4000 s at a substrate temperature of 60°C. During the measurement the gate bias was set to -20 V or +20 V, depending on the stress type, and the drain-source voltage was U_{ds} = 5 V. Since the measurements had to be performed in air, the samples had been encapsulated with a commercially available Solar Grade passivation.

An important finding was the effect of the passivation on samples with different surface roughness of the semiconductor. The mobility of the rougher sample almost doubled after applying the Solar Grade treatment, while the passivation had almost no effect on the performance of the smooth films. This again indicates how important the morphology of the semiconductor layer is.

The results of the stress measurements were quantified via the shift of the threshold voltage. The most stable system was the oxoalkoxide in THFA, whose U_{th} shifted by only 1.5 V in either positive or negative direction depending on the sign of the applied gate bias. The least stable TFT, as expected, was the one with the highest surface roughness, fabricated with the oxoalkoxide in MIPA formulation. It experienced U_{th} shifts above 4.5 V in either direction.

The potential of each material to be applicable in low temperature processes was investigated by changing the annealing temperature of the TFTs from 350°C to 250°C. The nitrate system showed excellent performance after only 1 hour on the hot plate in ambient atmosphere. The TFT fabricated with this semiconductor reached a mobility of 4.61 cm^2/Vs, while U_{th} = 0.18 V and S = 0.26 V/dec. However, the peak performance was reached at films thicker than in the case of the 350°C process, which also had a higher roughness. The reason why the lower temperature process resulted in maximum performance at thicker layers, ignoring their rough topography is counterintuitive. It proves that the semiconductor morphology dependence of TFT performance is not so straightforward after all. The TFTs

fabricated with the oxoalkoxide system peaked at the same layer thickness as in the case of a 350°C process. However 1 h of annealing in air at 250°C was not enough to fully convert the film into indium oxide and the performance remained low (μ_0 ~ 1 cm²/Vs) and the transfer curves were dominated by a very large hysteresis, a sign of high defect density inside the film. The performance increased though with annealing time and reached a mobility of 2.64 cm²/Vs after 4 hours on the hot plate. This experiment illustrated the advantage of the residue-free decomposition of the indium nitrate precursor at low temperatures to form a high quality indium oxide semiconductor.

The microscopic nature of the charge transport mechanism within the indium oxide semiconductor was investigated via a thermal method, by exploiting the temperature dependence of the charge carrier mobility. The temperature of the substrate of the TFTs was varied from -133°C to 203°C and at fixed intervals transfer curves were measured. The temperature dependence of the figures of merit was investigated.

The measurements were conducted inside a cryostat with a nitrogen atmosphere in the measurement chamber. Because of the limitations of the sample holder, the temperature could be raised only up to 107°C. The remaining temperature range was covered by placing the TFTs on a hot plate and increasing the temperature from RT to 203°C, which provided a large overlap region (RT – 107°C) for comparison of the effects of the two atmospheres as well.

The behavior of the three samples inside the cryostat was almost identical up to 60°C. The linear increase in the natural logarithm of μ_0 with reciprocal temperature seen in an Arrhenius plot revealed the existence of a shallow activation energy level located between 12 meV and 15 meV in all three TFTs. The distribution of states at this level was somewhat broader for the oxoalkoxide in MIPA based TFT, followed by the oxoalkoxide in THFA system and then a rather sharp peak at 13.8 meV shown by the nitrate system, as revealed by the forward and backward sweeps of the gate voltage.

As the temperature increased above 60°C, the measurements were affected by a sudden shift of the threshold voltage into the negative direction. It was assumed to be a result of a massive amount of oxygen vacancies formed at the surface of the semiconductor because of the strong non-equilibrium created by the oxygen deficient atmosphere. The effect was

more pronounced for the semiconductor with a rougher surface, resulting in a higher induced charge concentration calculated from the rate of change of the threshold voltage. This is another reason why the higher temperature measurements had to be conducted in air.

The measurements conducted in air revealed a different behavior of the TFTs. Within the overlapping region up to 100°C the oxoalkoxide based TFTs displayed a weak dependence of mobility on temperature, while in the case of the nitrate based TFT an activation energy level was found located at 50.5 meV from the *Conduction Band Minimum* (CBM). Above 100°C all three materials appeared to be affected by oxygen vacancy formation, although in air the process seemed to be slower than in a nitrogen atmosphere. In fact it was so slow, that the behavior of the mobility extracted from the forward sweep of the transfer curves indicated a delocalized band transport, as the mobility was decreasing with rising temperature due to phonon scattering. The mobility extracted from the backward swept transfer curves described a multiple trap and release transport (thermally activated transport) as the mobility rose with temperature.

The split in the forward and backward swept mobilities was assumed to be caused by a retarded ionization of the oxygen vacancies, which acted as trap states during the backward sweep of the gate bias. The location of the oxygen vacancies' activation energy was also much deeper for the TFTs measured in air than for the TFTs measured in nitrogen, supporting the apparent retarded ionization assumption.

With this work it has been shown that the morphology of the semiconductor layer is very important for a good performance of a thin-film transistor. It tends to be an indicator of the overall quality of the active layer, of its resistance, of its predisposition to form various defects under the influence of various process or environmental factors and thus of the electrical and thermal stability of the TFT. The TFTs fabricated in a bottom gate – bottom contacts architecture here via a solution process and only at 350°C displayed remarkable performance. Mobility values of 15 cm^2/Vs were reached with the indium oxoalkoxide from Evonik Industries AG, which are more than enough to drive high resolution and high frequency displays [79].

There are also numerous ways to still improve these results by switching to a high-k dielectric material for gate insulation, changing the architecture of the TFTs to top contact,

changing the *W/L* ratio, adjusting the source-drain electrodes' material to one with a more suitable work function.

The electrical stability of the material is as important as the value of the charge carrier mobility for application in actual devices, and if those devices are to be displays, the semiconductor should also be stable with respect to constant illumination as well as applied bias. Should this not be the case, it would probably be necessary to modify the chemistry of the semiconductor formulation to make it result in a layer able to suppress photo-charge generation, or formulate a suitable passivation to absorb the high energy wavelength responsible for photo-instability.

The work described here shows that indium oxide is a formidable candidate for the semiconductor layer in a thin-film transistor due to its high mobility and good electrical stability. A careful selection of the precursor and a matching solvent can result in high quality films with a high performance deposited from solution and annealed at temperatures as low as 250°C, which opens new application horizons. A deeper understanding of the conversion process of the precursor system into indium oxide and the associated transport mechanism will enable tailoring the semiconductor formulations to specific applications and revolutionize consumer electronics as we know it.

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