A Low Power, Variable Gain Common-Gate LNA

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***Abstract*— In this paper a novel variable gain common-gate LNA is presented, which features adaptive gain dependent bias current. The CG-LNA is designed in a 0.25 μm CMOS technology and consumes only 831 μA in maximum gain mode. The current consumption can be reduced further by factor 7 in the minimum gain mode.**

I. Introduction

There are different requirements upon low noise amplifiers (LNAs), e.g. low noise, high linearity, high gain and the lowest possible current consumption. Based on the system simulation [1] it can be shown that the linearity and noise figure requirements are much more relaxed for wireless sensor network receivers (IEEE 802.15.4 - ZigBee [2]) than for other communication systems, e.g. UMTS, GSM or GPS. Hence, battery lifetime of up to two years becomes feasible for a IEEE 802.15.4 receiver, whereas for GSM or UMTS it is difficult to achieve larger battery lifetime than one week.

As known from literature, there are two basic topologies for LNAs: common-source (CS) and common-gate (CG) configurations [3], [4]. The noise figure (NF) of the CS-LNA is bias-dependent, since it is a function of the bias-dependent f_T. The noise figure of the CG-LNA is bias independent in a first order approximation. Thus, the noise factor (F) of CS-LNA is a linear function of the ratio carrier frequency f_0 to transit frequency, while it is constant with respect to it for the CG-LNA [5]. For large values of this ratio, the CG-LNA outperforms the CS-LNA in terms of noise figure. However, for small bias currents, the f_T becomes low and, hence, the ratio $\frac{f_0}{f_T}$ becomes large. Therefore, the CG-LNA is more suitable for relaxed noise figure requirements but tough demands for low current consumption as shown in [6].

The basic CG-LNA architecture is depicted in Fig. 1. The operating point is adjusted using the bias current source at the source terminal and the supply voltage at the gate terminal of the MOSFET. The inductor at the drain terminal resonates with the parasitic capacitors of the MOSFET and the inductor itself and the input capacitor of the following circuit (mixer) at the desired carrier frequency. The resulting equivalent resistor $R_{P,Load}$ of the resonance circuit can be determined for this frequency.

In a first order approximation , the voltage gain becomes

$$G_V = \left| \frac{v_{out}}{v_{in}} \right| \approx g_{ms} \cdot R_{P,Load} \tag{1}$$

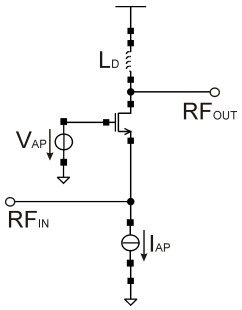

Fig. 1. Principle CG-LNA architecture.

and the input impedance is approximately equal to

$$Z_{in} \approx \frac{1}{g_{ms}} , \tag{2}$$

where g_{ms} denotes the drain-source transconductance of the MOSFET as proposed in [7]. To suppress reflection at the input, the input impedance of the LNA must match the output impedance of the preceding stage, e.g. $50\ \Omega$ [3], [4].

The input signal of a LNA covers typically a large dynamic range. For the IEEE 802.15.4 receiver the sensitivity is specified as $P_{IN}|_{min} = -92\ dBm$ and the maximum input signal as $P_{IN}|_{max} = -20\ dBm$ [2]. To avoid saturation effects of subsequent stages, the gain of the LNA should be reduced for large input signals. A new concept of gain adjustment is presented in the paper.

This paper is structured as follows: Section II discusses the feasibility of adjusting the gain. The adaptive gain adjustment for the CG-LNA is explained in Section III and simulation results are presented in Section IV. Finally, conclusions are drawn in Section V.

II. Gain Adjustment of LNAs

A. Basic Concepts

There are two options to reduce the gain for large input signals. According to (1) the first option is to reduce the resistor $R_{P,Load}$ by shunting the inductor at the drain of the MOSFET by a additional resistor R_x as shown in Fig. 2. This is the typical way to reduce the gain. The input impedance (2) does not vary, if the impedance at the drain changes. The current remains constant, since the MOSFET is biased from a constant current source. Thereby, the energy is wasted,

just if a large input signal is received. The input signal of a receiver is not continuously at the receiver sensitivity in practice. Therefore, this gain adjustment option is not a adequate solution for receivers operating in low power wireless sensor networks.

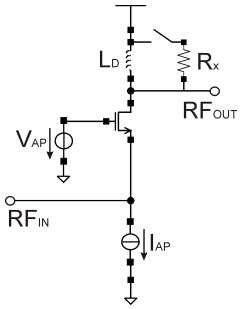

Fig. 2. Gain adjusting by shunting the drain inductor.

The second way to reduce the gain according to (1) is a reduction of the source transconductance g_{ms}. This is done by reducing the bias current of the MOSFET as shown in Fig. 3, but unfortunately the input impedance of the MOSFET (2) also changes. To ensure a constant $50\ \Omega$ input impedance, a shunt resistor is added at the input. The input impedance of the LNA is then

$$Z_{in} \approx \frac{1}{g_{ms} + \frac{1}{R_x}}\ , \tag{3}$$

where $\frac{1}{g_{ms}}$ is the input impedance of the MOSFET and R_x is the shunt resistor.

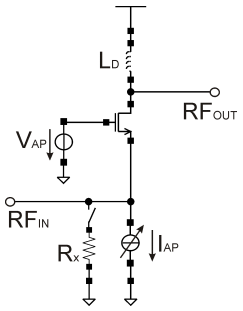

Fig. 3. Gain adjusting by adequate bias current and resistive input shunting.

Resistive termination at the input of a LNA is discussed as very unfavorable option for LNA design in [4]. On the other hand, the resistor is only added, if the input signal is very large and hence above the noise floor.

B. SNR Performance

According to the previous subsection, the LNA varies the as function of the gain. Therefore, it is necessary to show that the signal to noise ratio (SNR) performance does not deteriorate in the low gain mode. For this purpose the ratio of SNR at the output must be calculated for the different gain modes. Starting with the most common definition of noise factor (F)

$$F = \frac{SNR|_{IN}}{SNR|_{OUT}} \tag{4}$$

in agreement with [3], [4], [8]. Then, the SNR output ratio Δ is

$$\Delta = \left.\frac{SNR_2}{SNR_1}\right|_{OUT} = \left.\frac{SNR_2}{SNR_1}\right|_{IN} \cdot \frac{F_1}{F_2} = \left.\frac{P_2}{P_1}\right|_{IN} \cdot \frac{F_1}{F_2}\ , \tag{5}$$

where the index 1 denote the high gain mode, 2 the low gain mode, and P the input signal power, respectively. It can be also expressed in dB as

$$\Delta_{dB} \quad = \quad \Delta_{P_{IN,dB}} - \Delta_{NF} \tag{6}$$

and it is a measure of performance improvement in spite of the higher noise of the LNA in low gain mode.

III. Realization of the Adaptive Gain for CG-LNA

The adaptive gain CG-LNA was designed in a 0.25 μm CMOS technology for a use in an IEEE 802.15.4 receiver, suitable for a carrier frequency of 868.3 MHz (ISM band). The schematic is depicted in Fig. 4. External components such as off-chip inductors or external matching networks are dispensable.

The CG-LNA core comprises the MOSFETs M1 - M3 as presented in [6] and is biased in moderate inversion exploiting the higher current efficiency in this operation region. This is a good compromise for low power RF-systems [9].

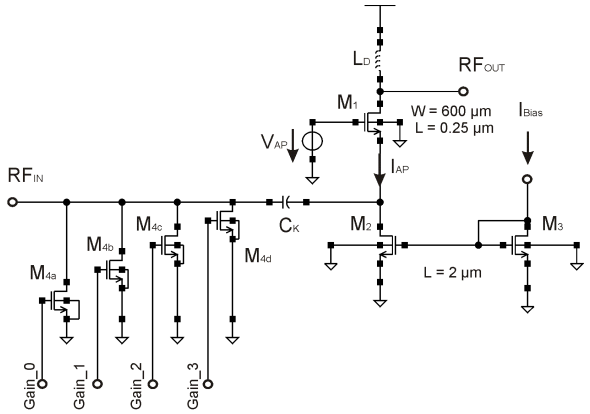

Fig. 4. Realization variable gain CG-LNA.

The resistor at the input can be realized using a MOSFET in triode region, which works as an imperfect switch with a relatively high ON-resistance. The maximum equivalent input voltage at input matching is very low ($u_{in}|_{max} = 31.6\ mV$), even for large input signals of $P_{IN}|_{max} = -20\ dBm$. Thus, the MOSFET resistor does not change its resistance and, hence, does not degrade the linearity performance.

An adjustable resistor was implemented using four MOSFETs (M4a - M4d), which are controlled by the logic using a gain control word. Thereby, it becomes possible to select various gain settings digitally. Since four MOSFETs provide sixteen gain stages, the gain step size is approximately 1 dB. The appropriate bias currents are supplied via the current mirror M2 and M3.

The LNA is designed as follows: First, the CG-LNA is designed for maximum gain in accordance with the specification. Then, the gain in linear or logarithmic scale is computed. After that, the bias current for each gain step is determined. From simulation the input impedance is determined and the shunt resistor calculated. From that, the corresponding shunt MOSFET is inserted. In an empirical way, the finger length and width are determined.

The parasitic capacitance was minimized by taking appropriate measures in the layout of M4. M4a to M4d use a different number of fingers equal length an width ($L = 0.25\ \mu m$, $W = 1\ \mu m$). The multipliers are 1,3,7 and 12.

IV. Simulation Results

A. Gain, Noise Figure, and IIP3

The circuit simulation is performed using Cadence and are based on the BSIM 3.3 MOSFET model. The pad parasitics are modeled as well as the bondwire inductors and accounted for in the simulation.

The inductor was modeled by its π-equivalent circuit with ten elements as described in [10]. The parameter of the inductor model can be determined either by separate EM-simulation of the coil or by measurement of the inductor, followed by a parameter fitting.

The simulated voltage gain at the different stages is depicted in Fig. 5. The maximum voltage gain (gain word 0000) is marked by squares and it amounts to is 4.41 which is equivalent to 12.89 dB on logarithmic scale. It steps 1-dB-wise down to -2.61 dB at minimum gain (gain word 1111). The frequency of maximum gain varies only slightly towards lower frequencies at low gain stages, but is still close to the carrier frequency $f_0 = 868.3$ MHz.

The current consumption is already very low in maximum gain mode ($831\ \mu A$), but it can be reduced further if a lower gain stage is chosen. In the minimum gain mode is the current consumption only $118\ \mu A$, which means a reduction by factor 7.

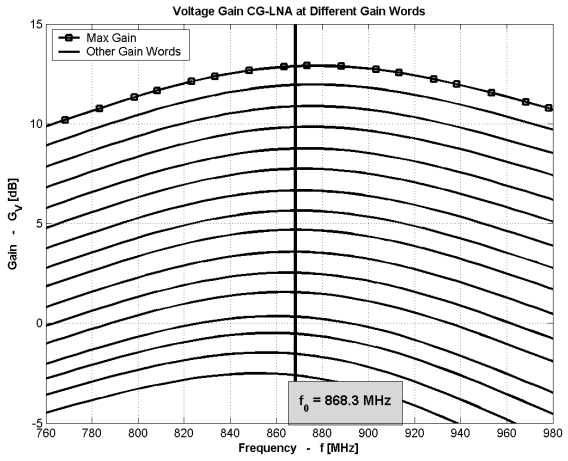

Fig. 5. Simulation result: voltage gain CG-LNA.

Fig. 6 shows simulated noise figure. The circuit simulation shows a noise figure of 4.5 dB which is equivalent to a noise factor of 2.8 at maximum gain (marked by squares). The maximum noise figure of 18.3 dB is achieved at minimum gain (gain word 1111).

It is very important to note that these simulations results include the noise contributed from the load of the LNA. A common way in the literature e.g. [3], [4] is to neglect this part, but it is valid theoretically only, if the load and thus the gain approaches infinity. Since the LNA needs a finite load impedance to achieve a voltage gain, NF calculations must consider it [6].

The BSIM 3.3 model used in these simulations does not allow for several parasitic effects raising the noise. Considering this, a worst case NF of about 5 dB is expected [6]. According to the system simulation [1], this is sufficient to meet the IEEE 802.15.4 requirements. Therefore, the here presented curves must be corrected only a little bit.

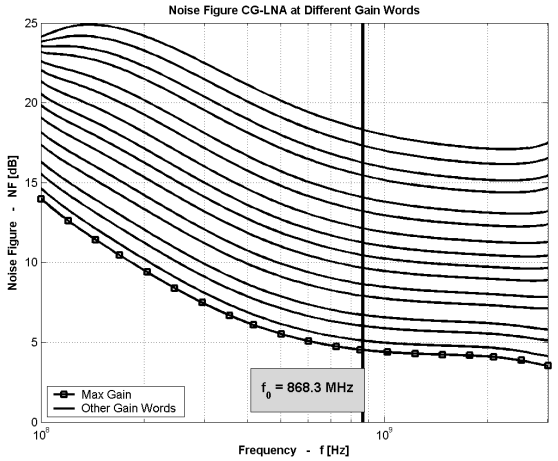

Fig. 6. Simulation result: noise figure (NF) CG-LNA.

The simulated input reflection coefficient S_{11} is depicted in Fig. 7. In the maximum gain mode (marked by squares) is $S_{11} = -15.51$ dB and in minimum gain mode $S_{11} = -18.08$ dB. The maximum reflection coefficient is -14.94 dB (gain word 0001) and the minimum reflection is -22.9 dB (gain word 1011). The remaining reflection coefficient is due to the parasitic effects of the gate source capacitance, the bondwire and pads. Consequently, the input impedance is close to 50 Ω at all gain stages.

Fig. 8 depicts the simulation result of the linearity. The solid lines represent the fundamental and the dotted lines the 3rd order intermodulation product (IM3). For sake of legibility, only the curves for maximum gain (gain word 0000), minimum gain (gain word 1111) and as an arbitrary example the gain word 1000 are shown. The first data point of the IM3 curve for the gain word 1111 can be considered as a numerical error.

The IIP3 is the abscissa at the intersection of the extrapolated fundamental and IM3 curve. The IIP3 is -6.37 dBm, -7.41 dBm and -7.24 dBm for the gain word 0000, 1111 and

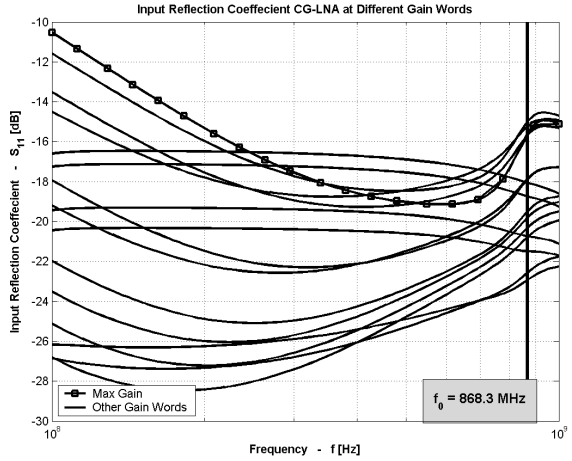

Fig. 7. Simulation result: input refection coefficient S_{11} CG-LNA.

1000 respectively.

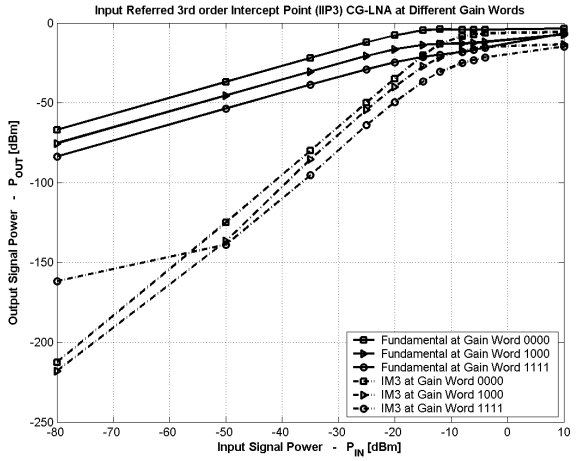

Fig. 8. Simulation result: Linearity (IIP3) CG-LNA.

B. SNR Performance

To show that the SNR performance does not deteriorate in the low gain mode, the SNR output ratio Δ is calculated as described in section II. The minimum input signal power is taken as the reference $P_1|_{IN} = -92\ dBm$. For the gain word 1000, the minimum input signal is $P_2|_{IN} = -56\ dBm$. The noise figure changes from $NF_1 = 4.51\ dB$ to $NF_2 = 11.23\ dB$. From this follows $\Delta_{dB} = 36\ dB - 6.72\ dB = 29.28\ dB$. An equivalent calculation can be done for the other gain stages. From these results it can be seen clearly, that SNR performance does not deteriorate in the low gain mode, even though the noise of the LNA in this mode is higher. The simulation results for three different gain words are summarized in Table I.

TABLE I
SIMULATION RESULTS.

G-Word	I_{AP} **[μA]**	**G [dB]**	S_{11} **[dB]**	**NF [dB]**	Δ **[dB]**
0000	830.95	12.89	-15.51	4.51	NaN
1000	281.76	4.69	-20.27	11.23	+29.28
1111	117.58	-2.61	-18.08	18.30	+53.71

V. CONCLUSION

In this paper a new adaptive gain CG-LNA is presented as well as the corresponding design strategy. It was shown that it is possible to reduce the bias current for the low gain stages and shunting a resistor to the input to ensure impedance matching. Thereby, it becomes possible to save energy if large signals are received. Furthermore it was shown, that SNR performance does not deteriorate in the low gain mode, even in spite of the higher noise of the LNA in this mode.

The designed CG-LNA is used in our IEEE 802.15.4 (ZigBee) receiver, which is at the moment in production at our $0.25\ \mu m$ CMOS technology. Measurement results will be presented after the fab-out.

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