Concept and Development of a New MOBILE-Gate with All Optical Input

Artur Poloczek, Wei Wang, Jörn Driesen, Ingo Regolin, Werner Prost, F.-J. Tegude

University of Duisburg-Essen, Center for Semiconductor and Optoelectronics, D-47048 Duisburg, Germany
Phone: +49 (0)203 379 3878, E-Mail: poloczek@hlt.uni-duisburg.de

***Short Abstract*—We demonstrate a concept and first results of an all optical driven MOBILE-Gate. We propose the transmission of the clock at a different wavelength than the data signal, but via a single optical fiber. Therefore, a staggered wavelength selective pin-diode is developed enabling the detection of both signals within a single spot. PSpice simulations based on experimental single device data are presented, indicating a circuit performance >10 Gbit/s.**

Keywords - MOBILE; RTD; HBT; RTBT; OEIC; pin-diode, wavelength selective detection

I. INTRODUCTION

The Monostable Bistable Transition Logic Element (MOBILE) [1] is an attractive approach for both robust and high speed logic circuits with a very low device count. A MOBILE is formed by two series connected Resonant Tunneling Diodes (RTD). The gate enables the execution of logic operations with an intrinsic latch function [1] provided by clocked operation. Therefore, the drive of the gate with a return-to-zero clock input is essential.

The combination of the MOBILE-Gate with optoelectronic devices such as photo-diodes forms an Opto Electronic Integrated Circuit (OEIC) with high functionality suitable for high speed fiber communication applications. On Indium Phosphide Substrate (InP) an 80 Gbit/s intrinsic operation of a MOBILE with a photo-diode as data terminal was presented in [2]. But, the monitoring of the output signal was performed by an electro-optic sampling system, only. An OEIC MOBILE with an optical data input, and electrical output has been demonstrated successfully by the authors in [3]. There, the clock signal has been supplied electrically and the optical data stream has been detected by a pin photo-diode. This concept is not practical for front end fiber communication systems, because the MOBILE gate needs a phase locked clocking and data stream.

In this paper an extended concept with an additional optical clock input terminal is presented. A heterostructure bipolar transistor (HBT) is used to switch between the high and low clock level. To offer high functionality, the intended optical receiver detects the optical clock control and data signal modulated on two different wavelengths selectively, but using a single spot of illumination. Thus, the phase locked clock control and data stream can be transmitted through a single fiber.

II. CONCEPT

The MOBILE requires a phase locked transmission of the data signal, detected by PD_1, and the clock signal, which will be detected by PD_2. The two RTDs are in series connected and form the classical MOBILE-Gate. The base-emitter-diode of transistor T_2 works as level shifter for the subsequent stage. The switching of the MOBILE occurs if the photo current of PD_1 exceeds the peak-current difference of RTD_1 and RTD_2.

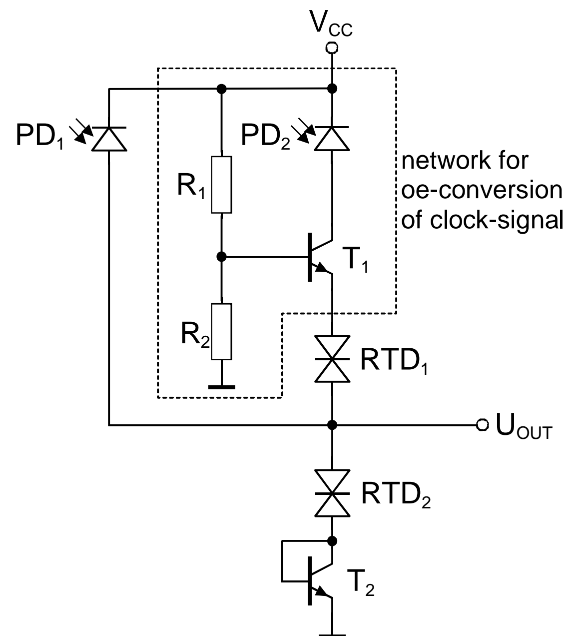

Figure 1. Circuit design for optical MOBILE-Gate clocking

The replacement of the electrical clock signal with an optical equivalent is beneficial, because the clock signal may be transported through the same fiber. It is necessary to convert the response of a photo detector into a voltage drop across the RTDs. Here, this is solved by the transistor T_1 (HBT), the resistors R_1 and R_2 and the pin-diode PD_2, bordered by the dashed line in Fig. 1. The resistors work as a biasing network

for T_1. The photo detector PD_2 is placed in the collector branch of T_1.

Without illumination on PD_2, a current flow in the collector of T_1 is prevented. Thus, the current is flowing mainly through R_1, the base-emitter-diode of T_1, the RTDs and the base-emitter-diode of T_2. The main voltage drop occurs on R_1. In this case the voltage across the RTDs corresponds to a low level clock signal.

If PD_2 is illuminated, the collector branch is opened because of the generated photocurrent. Due to the current gain of T_1, the base current decreases to approximately zero. Now, the voltage drop on R_1 is negligible. In this case, the voltage drop on the RTDs corresponds to a high level clock signal.

Due to the mentioned working behavior of T_1, the variation of voltage drop across PD_2 during the clock conversion does not change drastically. Thus, the transshipping of charge at the capacitance of PD_2 is minimized and the high speed performance of the circuit is optimized.

III. SIMULATION

A. Device Models

The presented concept was simulated by PSpice V 14.2. The used HBTs are modeled by a fitted Gummel-Poon based model. Fig. 2 shows the equivalent device models for RTD and pin-diode simulation.

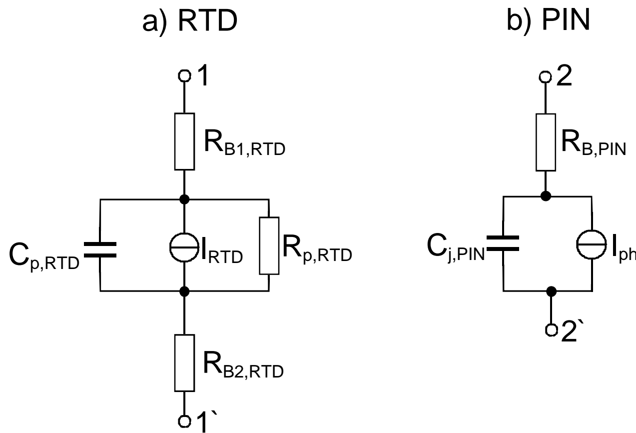

Figure 2. Device models for a) RTD and b) pin-diode

The resistors R_{Bx} represent the lead resistances of both devices. The capacitance of the RTD and the junction capacitance of the pin-diode are represented by $C_{p,RTD}$ and $C_{j,PIN}$. For improved convergence of the simulation, a high value ohmic resistor $R_{p,RTD}$ is included in parallel to $C_{p,RTD}$. I_{RTD} is a voltage controlled current source and describes the typical IV-characteristics of a RTD by a stage function. The first positive differential range (PDR1) and the negative differential range (NDR) are described separately in both directions by hyperbolic functions in the form

$$I_{range} = 1 \pm \tanh\left(f\left(\pm V_{11`} \pm V_{px}\right)\right), \tag{1}$$

where "f" is a fitting factor and V_{px} is the peak voltage of each direction. The second positive differential range (PDR2) is described by a conventional diode equation. The model was fitted to measured data of RTD devices fabricated in our laboratory [3].

The model used for the pin-diode describes the behavior of the device in reverse direction only, where it works as a photo detector. This is sufficient, because the pin-diodes used are biased negatively at any time. The generated photo current is modulated by the voltage controlled current source $I_{ph,sim}$. Within the simulation, the optical input power of the pin-diodes corresponds to the applied voltage to I_{ph}. This ratio is equal to the measured responsivities on λ=1.55 µm (PD_1) and λ=1.3 µm (PD_2) of InGaAs single pin-diodes with 600 nm absorption layer thickness, investigated in our department [3].

$$R = \frac{I_{photo}}{P_{opt}} = \frac{I_{ph,sim}}{V_{ph,sim}} \tag{2}$$

B. Simulation Results

The function of the oe-conversion network for the clock signal branch, is shown in Fig. 3, which gives the timing diagram of the base potential and base current of T_1.

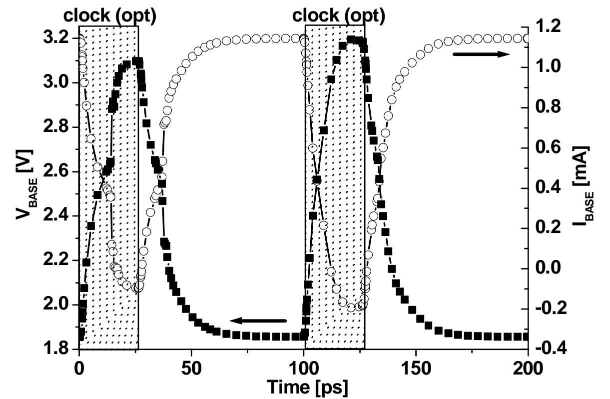

Figure 3. Simulated base potential and base current of T_1

The illumination of PD_2 provides a collector current to the transistor T1 and enables its normal open operation in combination with the base network R_1 and R_2. The MOBILE is connected with low losses to the electrical bias V_{CC}: the electrical clock is high. The resulting electrical clock potential over the RTDs is

$$V_{clk,high} = V_{BASE,on} - V_{BE,T1} - V_{BE,T2} \approx 1.7\text{ V} \tag{3}$$

Without illumination, the collector from T1 is disconnected from V_{CC}. The remaining current is the base-emitter current provided by the base network which is much higher than the previous base current during the open operation of T_1 and leads

to a voltage drop across R_1. The resulting voltage drop over both RTDs is

$$V_{clk,low} = V_{BASE,off} - V_{BE,T1} - V_{BE,T2} \approx 0.3 \text{ V} \quad (4)$$

Fig. 4 shows the simulated output timing diagram at 10 GHz. If the data pin-diode PD_1 is illuminated, the output of the MOBILE-gate reaches the high state. If PD_1 stays dark, the MOBILE-gate remains in low state.

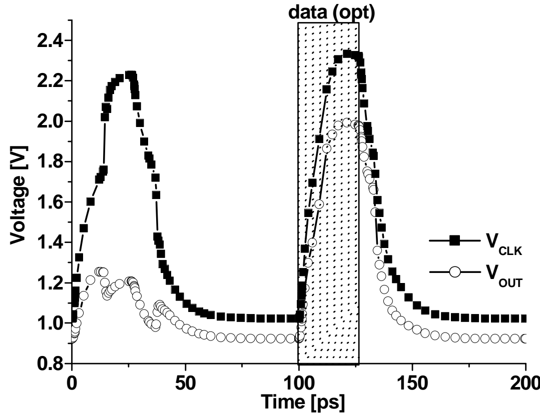

Figure 4. Simulated output timing diagram of the MOBILE-gate with all optical input

IV. DETECTOR

A. Detector Concept

The idea of driving the all optical input MOBILE-gate with a single fiber requires a phase locked transmission of the clock signal and the data signal simultaneously. This may cause further speed limitations which are not considered, here. The separation of both signals can be realized using two different wavelengths or by polarized light. Here, a wavelength selective detector optimized for the two favored wavelengths λ_1=1300 nm and λ_2=1550 nm for fiber communication is chosen.

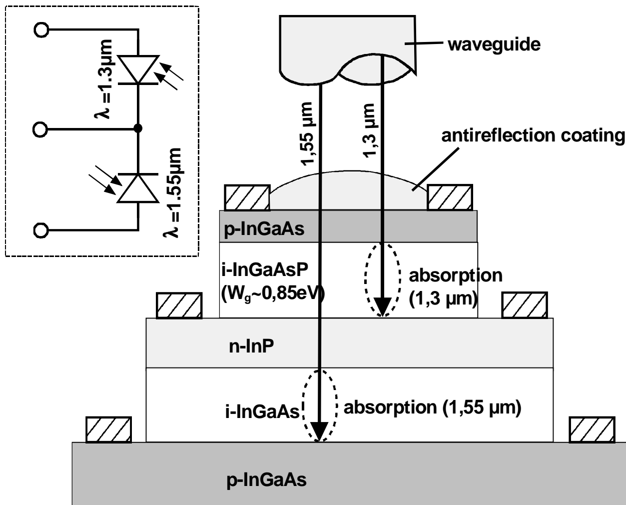

Figure 5. Cross section of the wavelength selective detector and its equivalent circuit (insert)

The idea is to stack two absorption layers with different band gaps, so that the upper layer absorbs only the low wavelength signal (λ_1) and is transparent for the other one. The high wavelength signal (λ_2) is absorbed in the lower layer [4]. Thus, both optical signals are detected and demultiplexed in parallel. The configuration shown in Fig. 5 requires an equal cathode potential for both pin-diodes. This restriction is considered by the presented circuit design.

B. Epitaxy

The layer stack of the investigated detector was grown in a low-pressure metal-organic vapour phase epitaxy (LP-MOVPE) system AIX200 with horizontal RF-heated reactor heating. The growth was carried out using nitrogen carrier gas at constant 50 mbar reactor pressure and with a V/III ratio between 5 and 40 using tertiarybuthylarsin (TBAs) and tertiarybutyl-phosphine (TBP) as group-V precursor. As group-III precursor trimethylindium (TMIn) and trimethyl-gallium (TEGa) were used. The p-type doping of the InGaAs contact layers was realized using diethylzinc (DEZn), while the maximum value was limited to 8E18 cm^{-3} to prevent the zinc diffusion into the following layers. N-type doping of the InP layer was adjusted up to 1.5E19 cm^{-3} by ditertiary- butylsilicon (DitBuSi).

C. Process Technology

The devices were processed by optical contact lithography and conventional wet chemical etching using a triple mesa design with ring metallisation on each contact layer. The critical etching of 600 nm nid-InGaAsP was performed by H_2SO_4:H_2O_2:H_2O (1:1:10) with an etch rate of ~ 2 nm/s highly selective on InP. The underetching slope and mesa surface is acceptable but may be further optimized with a dry etching process in future. To manage the contact bridges between the measurement pads and the intrinsic device with a total height up to 1.6 µm, a spin on glass (BCB) is used to support the contact line.

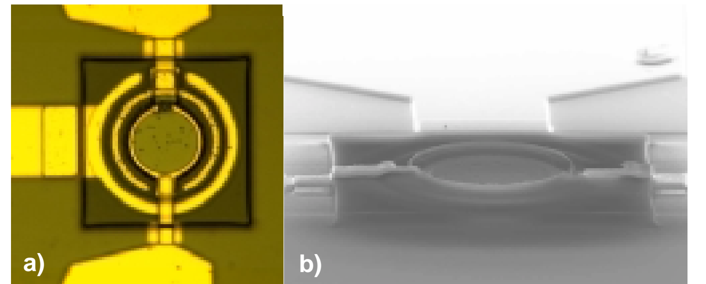

Figure 6. a) Optical - and b) SEM-micrograph of a fabricated pinip-single device with 21 µm diameter active area

D. Device Results

The processed pinip-devices are characterized concerning their DC I/V-characteristics and responsivity (see Fig. 7 and 8). The dark current of the InGaAs-diode moves in a typical range of ~20 nA. Looking at the upper InGaAsP-diode the dark current reaches values, which are higher by about one order of magnitude. This may be caused by poorer crystal quality of the

quaternary material and the mesa surface of the upper absorption layer.

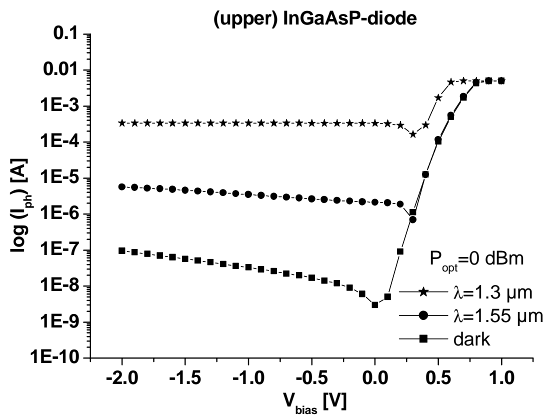

Figure 7. DC-Measurements and responsivity results of the upper InGaAsP pin-diode

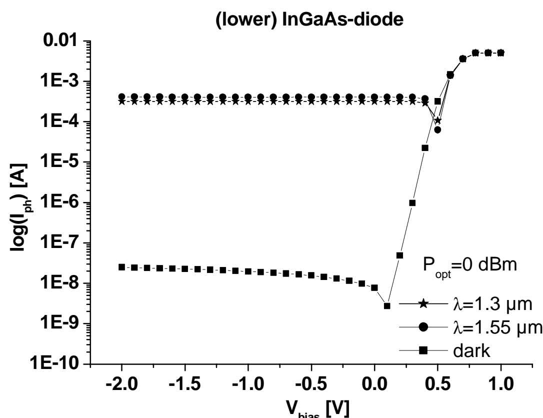

Figure 8. DC-Measurements and responsivity results of the lower InGaAs pin-diode

The responsivity measurements were accomplished with a cw-semiconductor laser providing λ=1,3 µm and λ=1,55 µm through a cleaved fiber. With regard to the InGaAsP-diode, the generated photocurrents differ by approximately two orders of magnitude. The lower InGaAs-diode is sensitive to both wavelengths and provides almost no selectivity. The measured resposivities are close to each other. Thus, the resulting crosstalks are $C_{1,55\mu m}$ = -20,6 dB and $C_{1,3\mu m}$ = -0,19 dB. The optimization of crosstalk on λ=1,3 µm is in progress. Here, we analyze the composition of the quaternary absorption material due to its absorption coefficient α and band gap W_g on the one hand, and we check the device design for possible diffused light sources on the other hand. The work on wavelength selective devices continues with investigation of the RF-performance.

V. INTEGRATION CONCEPT

For ease of fabrication of the OEIC, the layer stack height should be as low as possible. This is necessary to minimize the epitaxy costs and to ensure the stability of process. One possible solution is shown in Fig. 9. The thickness of the absorption layers depend on the required responsivity and on the RF-performance of the device. They make up the main part of the layer stack thickness. The HBT is integrated with the

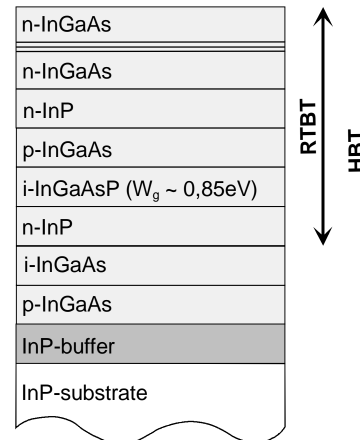

Figure 9. Layer stack for integration of the all optical input MOBILE-Gate

upper pin-diode. The p-contact, the absorption and the n-contact layers are suited for the base, collector and subcollector layers of a DHBT. The RTD quantum well is positioned in the emitter cap of the HBT. Thus, the use of a resonant tunneling bipolar transistor (RTBT) is possible. By removing the quantum well from the top, a conventional HBT is provided. With this integration concept, the total height of the layer stack is kept lower then 3 µm and is suited for processing with optical lithography.

VI. CONCLUSION

A concept for a MOBILE-gate with all optical input is presented and verified by simulation. Epitaxy parameters, technology details and first measurement results of photo detectors with improved functionality are presented in this paper. Furthermore, a technology concept for integration of the complete circuit is given. The proposed concept makes the MOBILE suitable for high speed fiber communication systems, because the optical clock control and the data stream can be transmitted phase locked through one fiber.

[1] K. Meazawa, T. Mizutani, "A New Resonant Tunneling Logic gate Employing Monostable-Bistable Transition," Jpn. J. Appl. Phys., Vol. 32, pp. L 42-L 44, 15 January 1993

[2] K. Sano, K. Murata, T. Otsuji, T. Akeyoshi, N. Shimitzu, E. Sano, "80 Gbit/s optoelectronic delayed flip-flop circuit using resonant tunneling diodes and uni-traveling-carrier photodiode," Electronics Letters, Vol. 35, No. 16, 5 August 1999

[3] W. Prost, P. Kelly, A. Guttzeit, V. Khorenko, A. Matiss, J. Driesen, A.-C. Mofor, A. Bakin, A. Poloczek, S. Neumann, A. Stöhr, D. Jäger, M. McGinnity, A. Schlachetzki, F.-J. Tegude, "Design and Modelling of a III/V Mobile-Gate with Optical Input on a Silicon Substrate," 17th Indium Phosphide and Related Materials Conference, Glasgow, UK, 8-12 May 2005

[4] J.C. Campbell, A.G. Dental, T.P. Lee, C.A. Burrus, *"Improved Two-Wavelength Demultiplexing InGaAsP Photodetector,"* IEEE Journal of Quantum Electronics, Vol. QE-16, No.6, June 1980