Modelling Methods for Testability Analysis of Analog Integrated Circuits Based on Pole-Zero Analysis

Der Fakultät für Ingenieurwissenschaften der
Universität Duisburg-Essen
zur Erlangung des akademischen Grades eines

Doktor-Ingenieur
(Dr.-Ing.)

vorgelegte Dissertation

von

Hasan Albustani
aus
Hama/Syrien

Referent: Prof. Dr.-Ing. Axel Hunger
Korreferent: Prof. Dr-.Ing. Bernd Straube

Tag der mündlichen Prüfung: 06 August 2004

Abstract

Analog and mixed-signal circuits are gaining popularity in various applications such as telecommunication, multimedia, biomedical applications and others. Testing of these circuits has a major impact on product cost and time-to-market. Furthermore, the trend of integrating complete analog/digital systems on a single chip has resulted in new testing challenges for such systems.

Testability analysis for analog circuits provides valuable information for designers and test engineers. Such information includes a number of testable and nontestable elements of a circuit, ambiguity groups, and nodes to be tested. This information is useful for solving the fault diagnosis problem.

In order to verify the functionality of analog circuits, a large number of specifications have to be checked. However, checking all circuit specifications can result in prohibitive testing times on expensive automated test equipment. Therefore, the test engineer has to select a finite subset of specifications to be measured. This subset of specifications must result in reducing the test time and guaranteeing that no faulty chips are shipped.

This research develops a novel methodology for testability analysis of linear analog circuits based on pole-zero analysis and on pole-zero sensitivity analysis. Based on this methodology, a new interpretation of ambiguity groups is provided relying on the circuit theory. The testability analysis methodology can be employed as a guideline for constructing fault diagnosis equations and for selecting the test nodes.

We have also proposed an algorithm for selecting specifications that need to be measured. The element testability concept will be introduced. This concept provides the degree of difficulty in testing circuit elements. The value of the element testability can easily be obtained using the pole sensitivities. Then, specifications which need to be measured can be selected based on this concept. Consequently, the selected measurements can be utilized for reducing the test time without sacrificing the fault coverage and maximizing the information for fault diagnosis.

Acknowledgments

I would like to take this opportunity to thank Prof. Dr.-Ing. B. Straube from Fraunhofer Institute Branch Lab Design Automation in Dresden for his support and patience. I would like also to thank all members of the Test and Verification group, especially, Dr.-Ing W. Vermeirn for his guidance and valuable advice throughout this research.

I would like to express my gratitude to Prof. Dr.-Ing. A. Hunger for his supervision.

Finally, I would like to thank my wife Maram and my son Adir for their encouragement and support.

Table of Contents

Chapter 1

Introduction

1.1. Analog Test Philosophy

Testing of analog and mixed signal circuits has become a challenge and gained more interest in the last decade for many reasons including increasing the applications of the analog circuits, integrating the whole system on one chip, and the high cost of analog testing compared with digital testing counterpart.

The reason for increasing the analog circuit applications is due to signals in real world are analog in nature with a continuous amplitude and time scale. Thus, any electronic system which interacts with the outer world has to contain some analog interface circuitry. Many domains such as telecommunications, multimedia, and biomedical applications require such analog interface circuitry. Analog and mixed-signal circuits such as amplifiers, filters, switches, analog-to-digital, and digital-to-analog converters are required in many end-equipment applications such as cellular telephones, hard-disk drives, modems, motor controllers, and multimedia audio and video products. Moreover, the analog circuits provide a good overall performance for high-performance applications (high frequency and low power applications), low-noise data-acquisition systems (e.g. in biomedical sensor applications), and parallel analog signal processing (such as in neural networks with a huge number of neurons). The strategy for testing these analog and mixed signal circuits (interface circuitry) is still needed.

In the past, a chip was just a component of a system; today, a chip is a system in itself. This integration of a system including analog and digital circuits in a chip (system-on-a-chip SoC)

has posed non-trivial problems in design and test areas. There are many factors that cause the complexity in testing the system-on-a-chip (SoC). Such factors are [Claa03]: the lack of adequate fault models, incapable tools for coping with the complexity of the SoC, lack of accessibility (lack of controllability and observability), lack of an industrial standard analog design for testability (DfT) methodology, and raising the importance of the timing-related faults.
The test cost of analog and mixed-signal circuits has now increased in comparison with digital test cost as shown in Figure 1-1 [Robe01]. The high analog test cost results from many factors such as expensive test equipment, long test development time, and long test production time. The development and production test time costs constitute a part of the development and production costs of the integrated circuits (ICs), respectively. Both the development and production test time are related to the time-to-market (TTM) which plays an important role for competitive semiconductor companies.

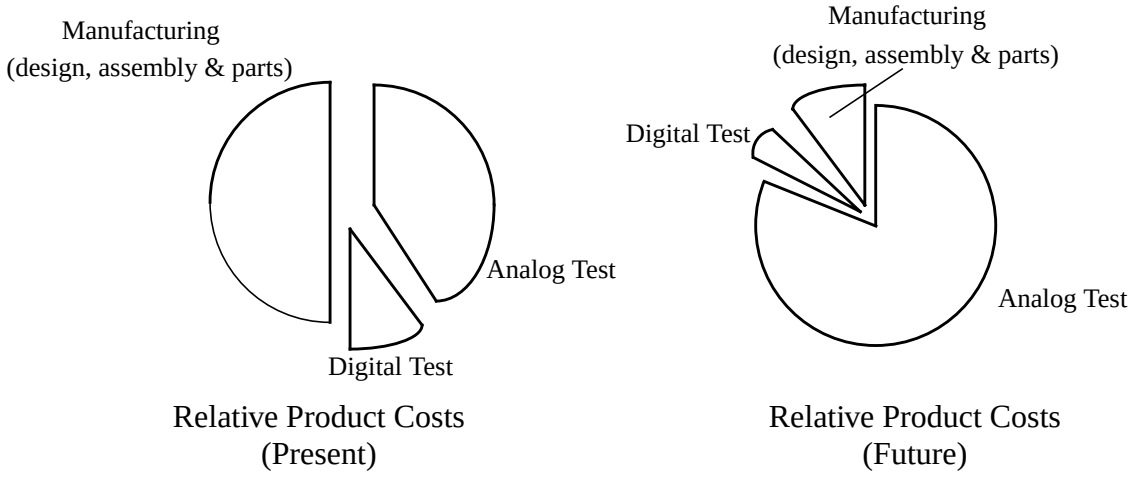


Figure 1-1: Electronic Manufacturing/ Test Cost [Robe01]

The challenge which test engineers are faced with is to develop a test methodology in order to reduce the test cost and to accelerate the time-to-market without sacrificing IC quality.
Consequently, the generation and evaluation of an effective test methodology is a very important issue in the production of an IC that having direct consequences on the price and the quality of the final product.

1.2. Motivation and Problem Definition

Testing can be defined as the process of verifying that an IC meets the specifications for what was designed [Huer93a]. Thus, the primary need for testing is to perform the following two sequential tasks:
(1) Checking the design characterizations: this task is called *prototype testing*.
(2) Checking manufacturing defects: this task is called *production testing*.

The objective of prototype testing is to verify the circuit under test (CUT) characterizations. If the circuit under test is identified as faulty during design characterization before it is sent to mass-production, it is desirable to diagnose the cause of the failure. Once faults are identified and located, a circuit can then be redesigned to enhance the yield of the ICs.
Prior information is required before fault diagnosis can be attempted. Such information includes optimal test points, optimal measurements, ambiguity groups, testable elements (which can be isolated), and untestable elements (which are assumed to be nominal). This information can be obtained by *testability analysis* of the circuit under test (CUT). The concept of testability analysis is strictly tied to the concept of the element-value solvability problem, which gives information about the solvability of the test problem for linear analog circuits. The degree of solvability of the circuit under test can be quantified using *testability measure* concept. As a result, the testability measure allows us to know beforehand how many faulty elements can be identified and how many elements have to be assumed fault-free. The testability measure is quantitatively given by the rank of the sensitivity matrix (testability matrix) constructed from the derivation of output parameters with respect to circuit elements.
In low testability circuits, where the testability measure is less than the number of the circuit elements, the testability analysis is strictly tied to the *ambiguity group* concept. Ambiguity groups consist of circuit elements that produce the same values of measurements. Therefore, the ambiguity groups have to be identified before constructing the fault diagnosis equations. The ambiguity groups can be determined by finding the null space of the testability matrix, in other words by finding the linearly dependent columns of the testability matrix. The zero-value rows of null space matrix correspond to the definitely testable elements and the nonzero-value rows and not orthogonal correspond to the elements that belong to the same ambiguity group. The null space of the testability matrix can be computed by *QR* factorization or by singular value decomposition (*SVD*) of the testability matrix.

The target of production testing is to detect defects resulting from the imperfections of the manufacturing process. Production testing is performed to distinguish good circuits from faulty ones. Testing cost (reflected as test time, throughput, and the cost of automatic test equipment) is a major concern for production testing. In order to make the decision whether a circuit is faulty or fault-free, a large number of specifications have to be checked. Thus, it is not possible to perform an exhaustive test, since it will require an infinite number of measurements and may result in prohibitive testing times on expensive automated test equipment. Therefore, the test engineer has to select a finite subset of specifications to be measured. This subset of specifications must result in reducing the test time and guarantee that no faulty chips are shipped.

Selecting an optimal set of measurements is related to the objective of a test. For example, if the goal of a test is only to detect faults, the selected measurements have to guarantee high fault coverage and reduce the test time. On the other hand, if the goal of a test is to locate faults, the selected measurements have to distinguish faulty elements from good ones taking into account ambiguity groups.

In this thesis, we will address two problems. The first one is to determine a testability measure (the number of testable elements) and ambiguity groups. The second one is to select the minimum number of measurements which lead to the reduction of the time cost without sacrificing fault coverage. Our measurement selection algorithm can also be employed in breaking up ambiguity groups should the fault diagnosis be the goal of the test.

In the first part of the thesis, we will present a novel methodology for determining the testability measure and ambiguity groups based on the poles and zeros of the transfer function which represents the linear analog circuit. Unlike other methods, which require numerical methods such as QR or SVD decompositions, our methodology requires only the knowledge based on the circuit theory. Thus, a new interpretation for the testability measure and ambiguity groups is presented which depends on the poles and zeros of the linear analog circuit. The proposed methodology can be employed as a guideline for fault diagnosis and test node selection.

Furthermore, the relationship between the testability measure based on the pole and zero analysis and controllability/observability concepts from control theory will be discussed. The controllable (or non-controllable) and observable (or non-observable) states in linear analog circuits can be determined based on pole and zero sensitivity.

In the second part of the thesis, the problem of minimizing the cost of production testing is considered. We will introduce the *element testability* concept which can be defined as the relative degree of difficulty in testing circuit elements with respect to circuit specifications under the parametric faults conditions. The element testability is computed based on the sensitivities of the poles and zeros of the linear or linearized analog circuit. Thus, our method depends on the sensitivity analysis which provides the relationship between the circuit elements and performance specifications. This kind of analysis ensures the structural and the functional test; in other words the circuit elements are tested by verifying circuit functionality. The selected measurements can be utilized for

- obtaining the high fault coverage or evaluating the test vectors in a fault simulator,
- reducing the test cost by reducing the number of tests without affecting the fault coverage, and
- for breaking up the ambiguity groups if the fault diagnosis is the goal of a test.

1.3. Organization

This thesis is organized as follows:
In Chapter 2, modeling and simulation of analog circuits will be discussed. Circuit modeling is presented using the levels of abstraction and hierarchy concepts. Furthermore, we will address simulation techniques used for simulating digital, analog, and mixed-signal circuits. Finally, a general overview of circuit simulation will be discussed.

In Chapter 3, a general introduction to testing analog and mixed-signal circuits will be addressed. The complexity of analog circuit testing and design-test flow will be discussed. Then, the analog testing techniques, namely the specification-driven test and fault-driven test, will be given. The classification of faults which can occur in analog circuits is discussed. Finally, we will present the state of the art for analog and mixed-signal circuit testing.

In Chapter 4, a new methodology for testability measure and ambiguity group determination will be presented. This methodology is based on the well-known pole and zero analysis and on pole-zero sensitivity. The testability measure at a certain node of a circuit can be computed from the number of the poles and zero in addition to the *DC* gain of the transfer function. Also, the testability measure can be computed from the circuit matrix constituted using the modified nodal analysis. The ambiguity groups can be determined using the pole and zero sensitivity.

Thus, a new interpretation of the ambiguity groups will be given based on the knowledge of the circuit theory. In this chapter, various simulation examples will be presented in order to validate our method.

In Chapter 5, we will present an algorithm for measurement selection for linear second-order circuits. The aim of this algorithm is to maximize the fault coverage and to reduce test cost by reducing the number of specifications that need to be measured. Also, this algorithm can provide maximum information about fault identification for fault diagnosis by breaking up the ambiguity groups. This algorithm is based on the element testability concept which can be determined based on the sensitivity of the circuit poles. The element testability will provide the information about the difficulty in testing circuit elements as well as the effect of element changes on circuit specifications. Parametric faults which are caused by manufacturing process variations and do not affect the circuit topology will be considered in this chapter.

In Chapter 6, the element testability and measurement selection algorithm proposed in Chapter 5 is developed to cover higher-order circuits. Higher-order circuits will be approximated by second ones using moment matching methods such as asymptotic waveform evaluation (AWE) by which the two complex-conjugate dominant poles of a circuit can be extracted. The element testability concept can be utilized to select specifications that need to be measured.

Chapter 7 presents the testability analysis of nonlinear analog circuits. A nonlinear analog circuit is linearized around an operation point and represented by its transfer function in the Laplace domain. The ambiguity groups can be determined based on the sensitivities of the poles and zeros of the linearized circuit. The parameter testability concept which gives an insight into the difficulty of testing the circuit parameters is introduced. Specifications that need to be measured can be selected relying on this concept. The parameter testability of circuit parameters with respect to circuit specifications can be obtained based on the pole sensitivities.
The measurement selection algorithm for nonlinear circuits can also be utilized to reduce test time without sacrificing the fault coverage and to provide maximum information for fault identification.

Chapter 8 concludes the thesis with a summary and comments concerning future researches.

Chapter 2

Circuit Modeling and Simulation

2.1. Introduction

Modeling and simulation are the most important parts of system analysis [Law00]. Modeling is defined as a process by which the physical system can be transformed into an abstract form called model. Simulation is defined as the process by which a computer is used (numerical analysis) to evaluate a model and to estimate its important characteristics. From an electronic circuit point of view, modeling can be employed to transform electrical circuits into a mathematical description called model. The model is described by the internal states and the input/output relationships such as logic equations for digital circuits or differential and algebraic equations (DAEs) for analog circuits [Sale94]. Then, an analog simulator such as SPICE is used to solve the mathematical equations that describe a circuit.

2.2. Circuit Modeling

The levels of abstraction modeling the digital circuits are mature and strictly defined [Ash03]. In contrast, the case of analog circuits is not similar, the levels of abstraction of analog design are not strictly defined, and there is no general agreement in the analog design community about the actual abstraction levels to be used in analog design automation [Giel91, Rose98].
The analog circuits may be modeled in different domains, each domain focusing on different aspects. These domains can be categorized into three perspectives: structure, behavior and

geometry, as shown in Figure 2-1 [Ashe03]. Each of these domains can also be divided into different levels of abstraction. At the upper level, a general overview of these domains is considered, and at the lowest level the greatest amount of details of the system is provided.

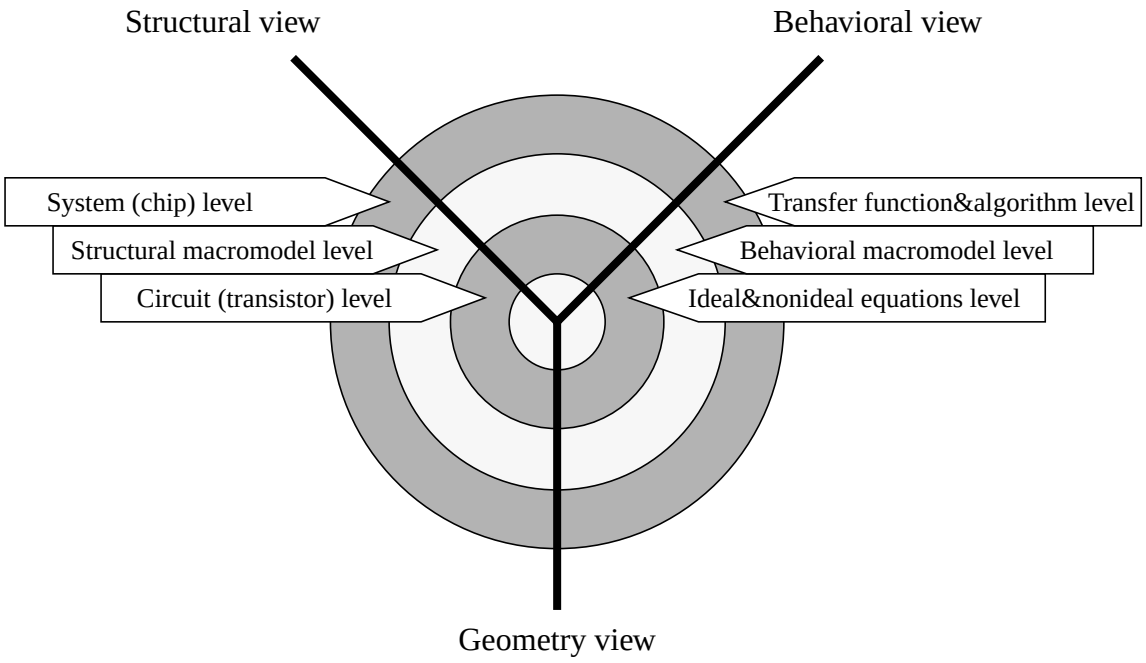


Figure 2-1: Analog domain and levels of abstraction [Ashe03]

The structure domain describes the analog circuits by a composition of interconnected elements or subsystems such as resistors, capacitors, transistors, op-amps, filters and others. The structure domain can be divided into different levels of abstraction: circuit level (also called element level or transistor level), structural macromodel level (also called functional level) and system or chip level.

The circuit level is the lowest level of abstraction and the elements at this level are primitives. At this level, the analog circuits are presented using semiconductor devices (such as BJT and MOSFET transistors) and passive elements (such as resistors and capacitors). There are several commercial circuit simulators such as SPICE and their derivatives which offer very accurate simulation, however, at this level the simulation is a very time-consuming task for large circuits. Therefore, a trade-off between accuracy and speed is accomplished using higher levels of abstraction.

The structural macro-model level or functional level consists of a collection of primitive elements such as operation amplifiers and comparators which are designed to achieve a specific functionality. Models at this level can be simplified to produce other models with the same

function, this technique being known as macromodeling [Mant95]. The model obtained consists of fewer elements than the original model of the circuit level description, an example being the Boyle op-amp macromodel [Boyl74]. This leads to short computational time and enables the simulation of larger circuits. The derivation of simplified models can be achieved by several methods such as circuit simplification, circuit build-up, symbolic macromodeling, and a combination of these methods [Mant95].

The system level consists of a connection of functional blocks or system transfer functions such as a modem chip. An example of the structural view is given in Figure 2-2 [Giel91].

The behavior domain describes the system by means of the linear or nonlinear mathematical equations. The detailed structure of the system is undefined. The behavior domain can also be divided into different levels of abstraction, nonideal equations, ideal equations, behavioral macromodel, transfer function, and algorithm [Ashe03].

For analog circuits, the description of the lowest level is provided by differential and algebraic equations (DAEs) with sets of unknowns that are a function of the time. At the highest level, the analog circuits can be modeled by using the transfer functions (for example using Laplace Transform). Hardware description languages such as VHDL-AMS [Ashe03] and MAST [Anal97] can be used to describe analog circuits using the behavioral description.

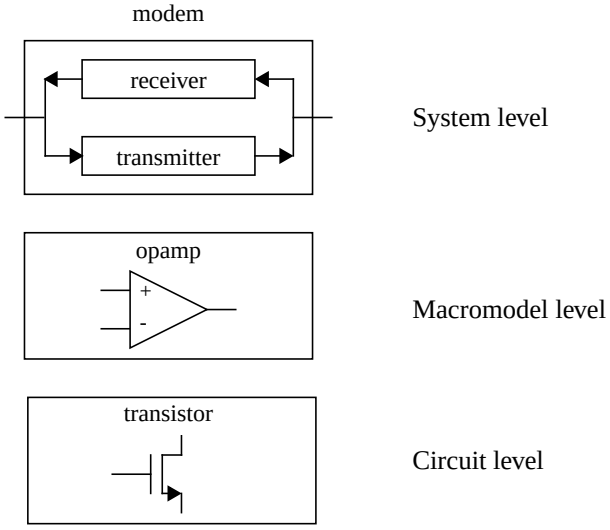


Figure 2-2: The levels of abstraction for a modem circuit [Giel91]

It is worthwhile to distinguish between the structural macromodel and the behavioral macromodel. The structural macromodel described by primitive elements can be simulated using a circuit simulator like SPICE, and provides more accuracy. In contrast, the behavioral macro-

model described by means of differential equations can be simulated using a behavioral simulator based on a behavioral modeling language such as VHDL-AMS. The behavioral macromodeling is still faster than the structural macromodel.
The combination of structural and behavioral modeling can be utilized using different levels of abstraction; this technique is known as multi-level hierarchical modeling. The circuit models can be described at different levels of abstraction. The model of interest is simulated at the lower level with more details (if detailed timing information is desired). The rest of the circuit models are simulated at the higher level to accelerate the simulation (where the accuracy is not the critical issue).

Finally, the geometry domain describes how the system is laid out in physical space (layout). This domain can be also divided into different levels of abstraction [Ashe03].

A progression from the upper level (the system level) to the lowest level (the electrical level) provides an increase in the accuracy of the simulation at the cost of more CPU-time. In contrast, a progression from the circuit level to the highest levels allows for larger and larger circuits to be simulated for a given amount of CPU-time or requires less and less CPU-time to simulate a given circuit. Multiple levels of abstraction are commonly used in top-down design or bottom-up verification. In both cases, the entire design at any given point in time may be represented at a number of different levels of abstraction [Sale94]. Therefore, mixing different domains and multiple levels would provide an effective balance between simulation speed and accuracy.

2.3. Simulation Techniques

System simulation methods can be classified as event-driven simulation, time-continuous and combined methods, depending on whether the system states are changed continuously or instantaneously [Law00]. In most simulation methods, the major independent variable is time.

2.3.1. Event-Driven Simulation

In event-driven simulation, the signals of interest consist of events which are changed instantaneously at separated points of time. The events contain the functional and the time information of a system. The event-driven simulation is widely employed in modeling digital hardware and communication systems.

In a digital system, the state variables take certain values called logic levels (e.g. high, low, and unknown). An *event* is a change in state variables of some circuit nodes that may affect other nodes in the circuit. The effect of an event is to cause all fan-out nodes to be processed and possible new events to be scheduled if changes in their output nodes occur.
Digital signals change their state values instantaneously (at discrete time points). Therefore, a digital simulator only needs to keep track of the timing of these changes (referred to as events) and the value held by a node between events. In order to accomplish this most efficiently, digital simulators employ what is known as an event queue. An event queue is an list ordered according to the occurrence time. “Digital time” progresses by taking each event in order, placing the changed state on a variable, and activating the models that are listed for such an event [Mant95].

2.3.2. Time-Continuous Simulation

In time-continuous simulation, the state variables, which represent the system models, are changed continuously with respect to time. The system can be modeled by ordinary differential equations (ODEs). Thus, a time-continuous simulator is a differential equations solver. Normally, an analytical solution for the models which are represented by means of the nonlinear differential equations is not possible in most cases, therefore, numerical integration methods are used. Continuous-time models can usually be used for analog circuits, physical processes, sensors and actuators.
In analog circuits, Kirchhoff’s Voltage Law (KVL), Kirchhoff’s Current Law (KCL) and branch constitutive equations are used to obtain the differential equations. Then, a time-continuous simulator such as SPICE can be used to solve these equations numerically via numerical integration methods. It is also possible in analog circuits to represent the state-variables as a function of frequency instead of time.
As a result, a simulator for continuous analog systems is a solver of simultaneous differential equations while an event-driven simulator is an event manager that activates selected parts of the system sequentially.

2.3.3. Mixed-Mode Simulation

In combined methods, the event-driven methods interact with time-continuous methods to simulate mixed-signal circuits. Such simulation methods that combine event-driven and time

continuous simulations are referred to as mixed-mode simulation. In practice, the implementation of the mixed-mode simulation can be classified as native mode, glued mode or fully integrated mode approaches [Sale94].

The native approach (or core modification approach) is implemented by extending an existing analog or digital simulator to comprehend the levels that are missing. Both, analog and digital algorithms are merged into a single simulator architecture and operate under a single event scheduler. Typically, an analog simulator is extended to incorporate the digital one, since the opposite extension is difficult without major modifications to the original digital simulator.

The glued approach actually is implemented using two existing simulators (analog and digital). Such approach must define an interface protocol so that both simulators can communicate with each other effectively. The communication protocol may tend to reduce the speed, and sometimes the accuracy, of the complete simulator. The glued simulator permits using both simulators without any modifications in contrast to the native mode which needs to achieve some modification of the original simulator.

The fully integrated approach is implemented using various simulation algorithms which are connected via well-defined data-transfer/synchronization mechanism called *backplane*. In this approach, single engine and unified data structure for both analog and digital components are used. The main drawback of this approach is the long development time.

2.4. Circuit Simulation

Circuit simulation is used in circuit design to verify circuit functionality and to obtain detailed timing information before the expensive and time-consuming fabrication process is performed [Bane94].

Circuit simulators provide very accurate electrical waveform information, however, it is impractical and extremely time-consuming for complex analog and mixed-signal VLSI circuits. In fact, a circuit simulator is the only tool which provides enough detail to ensure that a circuit will meet specifications over a wide range of circuit parameters and operation conditions [Sale94, Horn99].

2.4.1. Circuit Topology

An analog circuit can be described using the graph theory where the circuit elements are represented by the edges of a graph and circuits nodes are represented by the nodes of a graph. The

direction of current flowing through the branches can be assumed from the positive to the negative nodes. An example of the circuit and its associated graph is shown in Figure 2-3 [Vlac94]

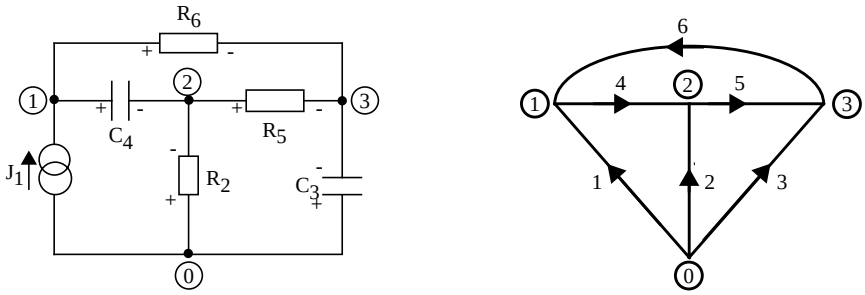


Figure 2-3: An example of analog circuit and its associated graph [Vlac94]

There are three matrices associated with a direct graph: incidence matrix *A*, cutset matrix *Q*, and loop matrix *B* as shown in Figure 2-4.

Incidence matrix *A* is a *n* x *b* matrix where *n* is the number of ungrounded nodes and *b* the number of edges in the graph. The rank of matrix *A* is equal to *n (Rank(A) = n)*. The KCL and KVL can be represented using the incidence matrix as $Ai = 0$ and $v_b = A^t v_n$ respectively, where *i* is the current of branches, v_n is node voltages and v_b is branch voltages.

A tree of a graph is defined as the edges containing all the nodes of the original network which do not form a closed path. The remaining edges form a cotree. A cut through an edge of the tree and many edges in the cotree form a cutset. Since there are *n* edges in a tree, there will be *n* basis cuts.

The cutset matrix *Q (n* x *b)* can be constructed using a set of cuts $Qi = 0$ and can be written as $Q = [Q_t\ Q_c]$ or $[1\ Q_c]$ where Q_c and Q_t corresponds to the cotree edges and tree edges respectively.

The loop matrix *B (n* x *b)* is formed using the fundamental loops in the graph that contain only one cotree edge and many tree edges where $Bv = 0$. The loop matrix can be partitioned into two matrices $B = [B_t\ B_c]$ or $[B_t\ 1]$ where B_c and B_t corresponds to the cotree edges and tree edges respectively. The cutset matrix and loop matrix are orthogonal $BQ^t = 0$ or $QB^t = 0$. Thus, the loop matrix can be obtained from the cutset matrix and vice versa.

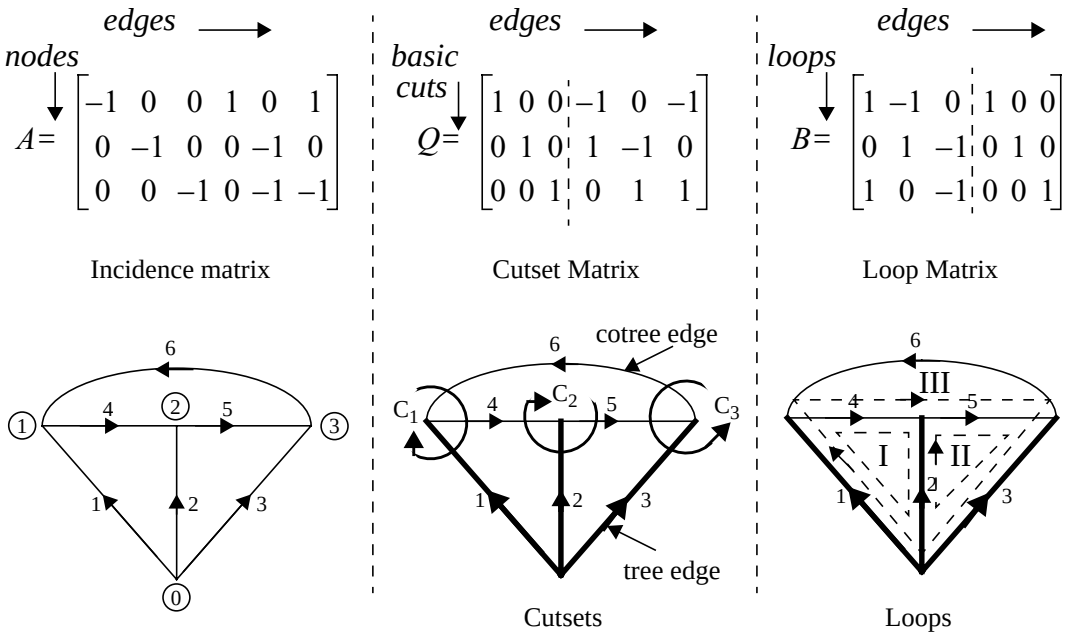


Figure 2-4: The fundamental matrices and their associated graphs

The graph representation of the analog circuits is employed in many applications such as formulation of circuit equations and formulation of state-variable equations [Vlac94].

2.4.2. Circuit Equations Formulation and Solution

There are mainly three formulation methods of circuit equations, namely nodal analysis, modified nodal analysis, and Sparse Tableau analysis [Vlac94].

Classical nodal analysis depends on the KCL for each node to formulate the circuit equations and is given in matrix form as follows:

$$\left[Y_n\right]\left[V\right] = \left[J\right] \tag{2-1}$$

where Y_n is the admittance matrix, V is the node voltages, and J is the independent current sources. However, nodal analysis cannot represent the dependent sources such as current controlled voltage source (CCVS), voltage controlled voltage source (VCVS), and current controlled current source (CCCS). Hence, the modified nodal analysis is used to add the ability to present such circuit elements. The modified nodal analysis is now the most common method used in circuit simulators. The underlying idea of modified nodal analysis is to add the current

of elements which do not have an admittance description. The matrix form of modified nodal analysis is given:

$$\begin{bmatrix} Y_n & B \\ C & D \end{bmatrix} \begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} J \\ E \end{bmatrix} \qquad \text{or} \qquad [Y][x] = [b] \tag{2-2}$$

where Y_n is the admittance matrix, *B, C,* and *D* are matrices which are resulted from the new equations that describe the non-conductive elements (contain only -1, 1, and 0), *V* is the node voltages and *I* is the branch currents of the non-conductive elements, *J* and *E* are the independent current and voltage sources respectively. Also, the system equations can be expressed as $Yx = b$, where *Y* is the system matrix created by modified nodal analysis, *x* is the solution vector which can be composed of currents and voltages and *b* is the source vector.

The third method of circuit equation formulation is Sparse Tableau in which all branch currents, all branch voltages, and all nodal voltages are retained as unknown variables of a circuit. The matrix form of Sparse Tableau is given by Eq. (2-3)

$$\begin{bmatrix} 1 & 0 & -A^t \\ Y_b & Z_b & 0 \\ 0 & A & 0 \end{bmatrix} \begin{bmatrix} V_b \\ I_b \\ V_n \end{bmatrix} = \begin{bmatrix} 0 \\ W_b \\ 0 \end{bmatrix} \qquad \text{or} \qquad [T][X] = [W] \tag{2-3}$$

where 1 is the identity matrix, *A* is the incidence matrix, Y_b and Z_b are the admittance and impedance matrices respectively, V_b is the branch voltages, I_b is the branch currents, V_n is the branch voltages, and W_b is the independent current and voltage sources. The size of the matrix *T* is $(n+b+b)$ x $(b+b+n)$ where *n* is the number of the circuit nodes and *b* is the number of the circuit branches.

The solution of the linear system described by the last equations (2-1), (2-2), and (2-3) is performed by either direct methods or iterative methods. Direct methods are used to solve the linear equations in a fixed and finite number of steps while iterative methods need to converge to the exact solution by presumed error. Many important factors are contributed to assess the desired method such as complexity of computation, accuracy, and the ease of implementation. The most direct methods used to solve linear system are the Gaussian elimination and the *LU* decomposition with pivoting strategy to avoid the ill-conditioning problem. These algorithms are employed to perform *DC, AC,* and transient analysis. Iterative methods such as Gauss-Jacobi, Gauss-Seidel, and relaxation methods are normally used to perform the transient analysis. These methods are faster than the direct methods and provide more information such as *latency* (certain circuit signal values do not change appreciably with time) and *multirate*

behavior (signal values in different portions of circuits change at different rates requiring different time steps). Furthermore, they are suited for parallel computing [Bane94].
A nonlinear system is described by nonlinear equations. These nonlinear equations are usually solved by means of the Newton-Raphson algorithm. The Newton-Raphson algorithm can be used to perform nonlinear the *DC* analysis and can be combined with other algorithms like the *LU* decomposition to perform the nonlinear transient analysis.

2.4.3. Analog Circuit Analyses

2.4.3.1. *DC* Analysis

The *DC* analysis of linear circuits is achieved with shortened inductors and opened capacitors. Also, all time-dependent sources and time-varying parameters and their derivatives are set to zero. The goal of the *DC* analysis is to determine the *DC* operating point of the circuit. The operating point defines the steady state of the circuit at time = 0. The *DC* analysis is automatically performed prior to a transient analysis to determine the initial values of the differential equations and prior to the *AC* small-signal analysis to evaluate the parameters of the linearized small-signal models for nonlinear semiconductor devices. Moreover, the *DC* analysis can be used to perform the *DC* transfer (sweep) analysis. The independent source is stepped over a user-specified range, and the *DC* operation point for a specific output is computed for each *DC* step.
For nonlinear circuits, the *DC* operating points are evaluated using iterative methods such as the Newton-Raphson algorithm. The nonlinear elements are linearized around a presumed operation point, and the nodal equations that characterize the linearized circuit are formulated. The linearization about the operating point can be achieved by replacing the nonlinear devices by linear models such as companion model for a diode [Pill95]. Then, the parameters of the linearized model are computed at each iteration. After an initial guess is assumed, the nodal equations are solved at the presumed operation point. Finally, the convergence criteria are checked. If these criteria are fulfilled, the iteration is terminated. Otherwise, the solution is assumed as a new operating point, and the algorithm is again repeated as shown in Figure 2-5 [Pill95]. All problems derived from the iterative algorithms such as iteration step and convergence problem (overflow) must be taken into consideration while solving of the nonlinear equations.

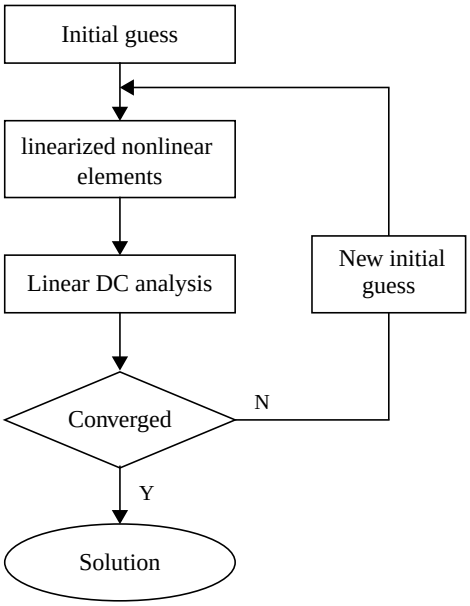


Figure 2-5: Newton-Raphson iteration for nonlinear *DC* analysis

2.4.3.2. *AC* Small Signal Analysis

In the *AC* small-signal analysis, the *DC* analysis is required to determine the parameters of the small-signal model for nonlinear elements. In other words, the nonlinear elements are linearized around their operating points and assumed to be operated at the linear region of the input/output characterization (for example the forward-active region in *BJT* transistors). Energy storage elements such as capacitors and inductors are modeled in the frequency domain (or Laplace domain) in terms of complex admittances *Y* (capacitor admittance = $j\omega C$ *or* sC, inductor admittance = $1/j\omega L$ *or* $1/sL$). The linear equations that describe the circuit are formulated. The *AC* output variables (voltages or currents) are computed by solving the linear equations over a user-specified range of frequencies. The problem which is created by performing the *AC* small-signal analysis at the extreme values of frequency such as $\omega = 0$ (in which the capacitors become open circuit and the inductors become short circuit), $\omega \rightarrow \infty$ (in which the capacitors become short circuit and the inductors become open circuit), or frequencies that cause the ill-conditioning problem must be avoided. In the *AC* small-signal analysis, the behavior of the circuit is evaluated as a function of frequency. The *AC* small-signal analysis can be used to determine the frequency response of the circuit using Bode plot in

which the amplitude and the phase of the output variable are evaluated over a range of frequencies as shown in Figure 2-6 [Pill95]. Furthermore, the *AC* small-signal analysis can be utilized to perform the pole-zero analysis, the *AC* sensitivity analysis, and the noise analysis.

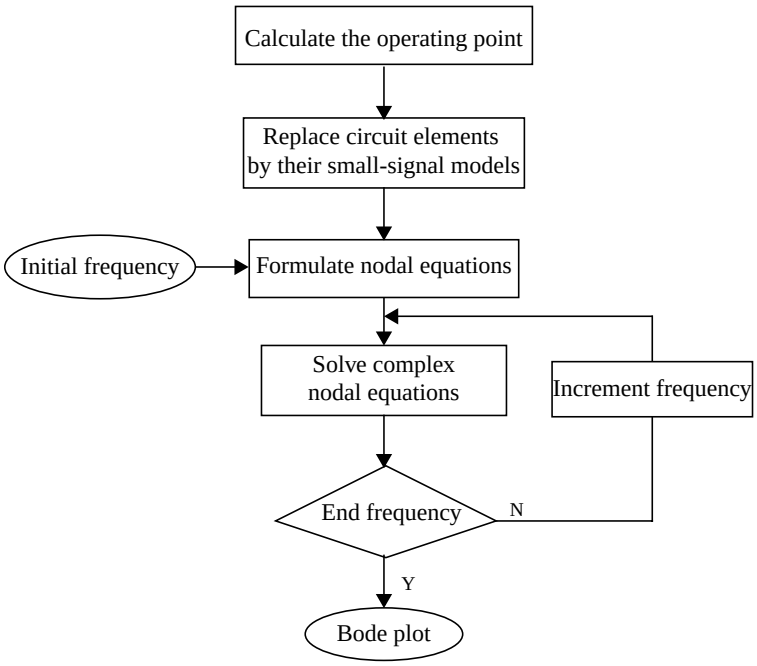


Figure 2-6: Small signal AC analysis

2.4.3.3. Transient Analysis

The transient analysis is used to describe the circuit behavior as a function of time. The electrical circuits are represented by differential equations which are formed by means of the Kirchhoff's Voltage Law (KVL) or Kirchhoff's Current Law (KCL) and the constitutive equations. The *DC* analysis is usually required to determine the initial conditions of the differential equations. There are two approaches to solve the circuit simulation problem: the direct methods and the relaxation-based methods.

In direct methods, the differential equations are converted into linear or nonlinear algebraic equations by means of integration methods such as forward Euler, backward Euler and Trapezoidal methods. In this step, the time is discretized by a prescribed time step Δt and the energy storage elements such as capacitors and inductors are replaced by their time-dependent companion models [Pill95]. The next step of direct methods depends on whether a circuit is linear or nonlinear. In linear circuits, the integration methods provide directly linear algebraic equa-

tions, whose solution is obtained by Gaussian elimination or LU decomposition at each time point. In nonlinear circuits, the Newton-Raphson algorithm is used for solving the nonlinear equations.
The accuracy plays an important role in transient analysis since the integration methods are an approximation that depends on the selection of time step Δt. Other problems such as convergence speed, initial conditions, stiffness and stability have to be considered.

The main disadvantages of the direct methods of the transient analysis are [Ban94]: (1) The excessive computational time needed to compute the response over a long time interval. Two time-consuming processes have to be executed, the Newton-Raphson iteration and solving linear equations (factorization of the Jacobian matrix) at each time point, as shown in Figure 2-7 [Pill95]. (2) The waveform properties such as latency (certain circuit signal values do not change appreciably with time) and multirate behavior (signal values in different portions of circuits change at different rates requiring different time steps) are difficult to exploit. Such properties are often encountered in *MOS* circuits. Hence, the relaxation-based methods are proposed for solving circuit simulation problems.
The relaxation-based approaches can be divided into three approaches, according to the kind of equations that describe the system [Newt84]. Then, it can be applied for solving linear equations (linear relaxation methods), nonlinear equations (nonlinear relaxation methods), and differential equations (waveform relaxation methods).
The linear relaxation methods are used for solving the linear circuit equations by means of iterative methods such as the Gauss-Jacobi or Gauss-Seidel methods. In these methods, the linear equations are solved for one unknown variable at a time and the other unknown variables are fixed. After iterative solving for unknowns, the final result is convergent to the exact solution. The nonlinear relaxation methods exploit the nonlinear Gauss-Jacobi or nonlinear Gauss-Seidel algorithms combined with the Newton-Raphson algorithm to solve a set of nonlinear equations. There are many forms of nonlinear relaxation methods such as timing analysis, iterated timing analysis, and one-step relaxation. Partitioning of the large circuit can be achieved and, by exploiting the parallelism, the nonlinear equations can be solved to accelerate the computation [Bane94]. The last kind of relaxation methods is the waveform relaxation method which exploit the Gauss-Seidel procedure for solving the ordinary differential equations.

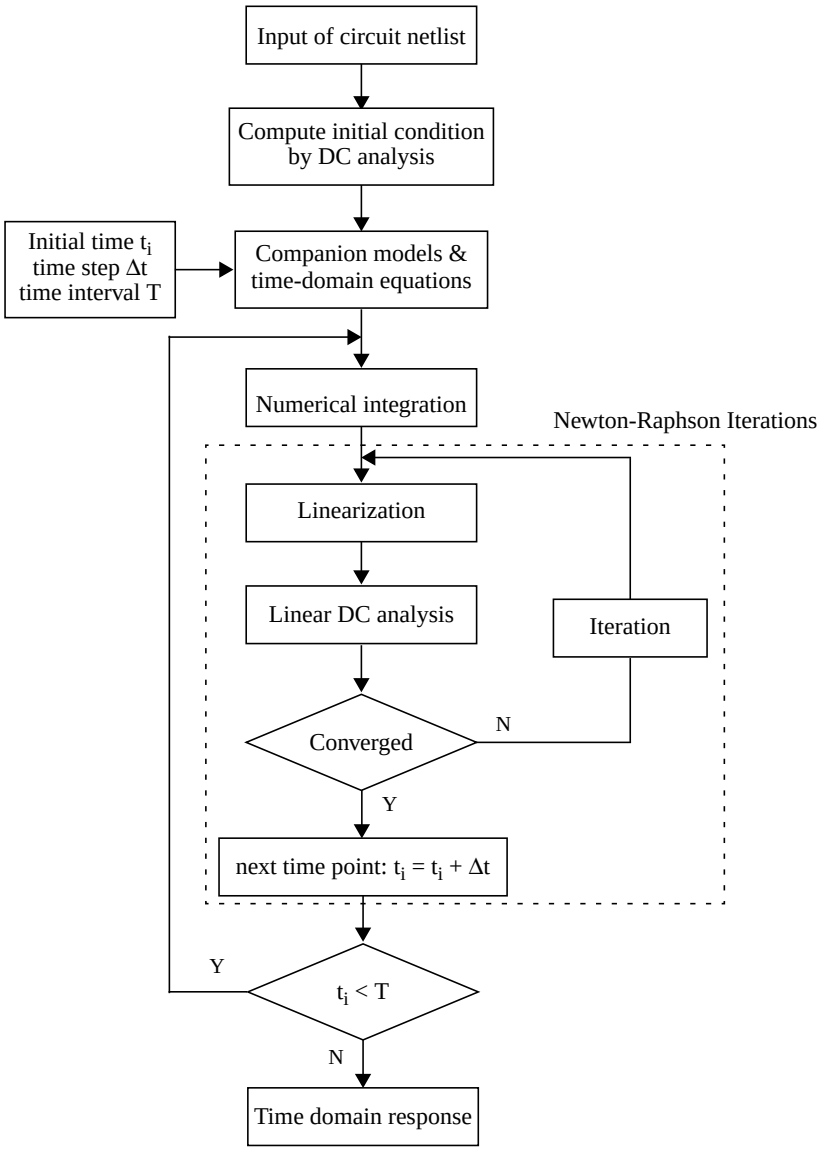


Figure 2-7: Transient analysis

The state-variable equations given in Eq (2-4) can be utilized to perform the transient analysis for linear analog systems. The system with *r* input sources and *m* outputs can be described by first-order differential equations as in following:

$$\begin{aligned} x'(t) &= A \cdot x(t) + B \cdot u(t) \\ y(t) &= C \cdot x(t) + D \cdot u(t) \end{aligned} \tag{2-4}$$

where, *x(t)* is the *n* x *1* state vector, *u(t)* is the *r* x *1* input vector, *y(t)* is the *m* x *1* output vector, and matrices *A*, *B*, *C*, *D* are *n* x *n*, *n* x *r*, *m* x *n*, and *m* x *r*, respectively. The state-variable equations can be formulated via network topology based on the direct graph (cutset and loop equa-

tions) associated to the circuit [Chao95a]. The total response of the circuit can be divided into two responses: zero-state and zero-input responses. The solution of the state-variable (total response) can be obtained via the state transition matrix approach or via the inverse Laplace transform approach.

2.4.3.4. Sensitivity Analysis

The sensitivity analysis is employed in most commercial circuit simulators such as PSpice and Saber. The effect of parameter changes on performance specifications caused by the deviation of the manufacturing process can be determined by using the sensitivity analysis. In other words, the sensitivity analysis based on a first-order approximation provides the variation of a circuit's response with respect to parameter variations. The performance sensitivity is mathematically defined as the derivation of the performance T_j ($j=1,2,...,n$, where n is the number of circuit performance specifications) with respect to the circuit element h_i ($i= 1,2,...,k$, where k in the number of the circuit elements). The derivatives are computed at the nominal values of the circuit elements. There are two forms of sensitivity, according to the amount of parameter variation. The normalized differential sensitivity (called also small-change sensitivity) is valid only for small deviations (infinitesimal changes) of the element h_i (Eq. (2-5)). The normalized incremental sensitivity (also called large-change sensitivity) is used for small and large deviations (Eq. (2-7)).

$$S_{h_i}^{T_j} = \frac{h_i}{T_j}\frac{\partial T_j}{\partial h_i} \tag{2-5}$$

In the case of variation of many output parameters caused by the variation of many elements, the Eq. (2-5) can be expressed in matrix form as follows:

$$\left[\frac{\Delta T}{T}\right] = \left[S_h^T\right]\left[\frac{\Delta h}{h}\right] \tag{2-6}$$

The incremental sensitivity can be expressed as follows:

$$\rho_{h_i}^{T_j} = \frac{h_i}{T_i}\cdot\frac{\Delta T_j}{\Delta h_i} \tag{2-7}$$

where ΔT_j is the change in performance T_j resulting from an incremental change Δh_i of the element h_i. If the circuit performance can be written in rational form as $T(s,x) = N(s,x) / D(s,x)$ (where s is the complex frequency), then the incremental sensitivity can be computed as a function of the differential sensitivity [Fidl84]:

$$\rho_{h_i}^{T_j} = \frac{S_{h_i}^{T_j}}{1 + S_{h_i}^{D} \frac{\Delta h_i}{h_i}} \tag{2-8}$$

where S_{hi}^{D} is the differential sensitivity of the denominator D of the performance T_j. The incremental sensitivity can be generalized for the deviation in many elements. In the case of the deviation of k elements $\{h_1, h_2,..., h_k\}$ and one output parameter T, the relative deviation of output parameter $\Delta T/T$ can be given by Eq (2-9)

$$\frac{\Delta T}{T} = \frac{\sum_{i=1}^{k} S_{h_i}^{T_j} \frac{\Delta h_i}{h_i}}{1 + \sum_{i=1}^{k} S_{h_i}^{D} \frac{\Delta h_i}{h_i}} \tag{2-9}$$

There are two methods for sensitivity computation, namely the direct method and the adjoint method [Dire69] (based on Tellegen's theorem [Penf70]). In the direct method, the sensitivity of all outputs with respect to one element is needed while in the adjoint method the sensitivity of one output with respect to many parameters is needed. Usually, the sensitivities of all outputs are not required, or only a single output is available; therefore, the adjoint method is preferred for computing the sensitivity of the output associated with all circuit elements (cf. Appendix A). For the system represented by the modified nodal analysis $Yx = b$. The adjoint system is represented by $Y^t x^a = - d$, where x^a is the solution of the adjoint system and d is the linear combination of the variables x. The output of interest $\phi(x)$ can be expressed as $\phi = d^t x$. The sensitivity of the output ϕ associated to the element h can be given:

$$\frac{\partial \phi}{\partial h} = (x^a)^t \frac{\partial Y}{\partial h} x - (x^a)^t \frac{\partial b}{\partial h} \tag{2-10}$$

The cost for the sensitivity adjoint method is equal to that of the two circuit simulations, once for the original circuit and once for the adjoint circuit. The computation of the sensitivities is a time-consuming task, because the sensitivity must be evaluated at each frequency point. Therefore, pole and zero sensitivity provide an alternative for determining the effect of the element variation on circuit performance, independent of the frequency.

The applications of the sensitivity analysis for analog testing such as fault diagnosis, test signal generation, and test measurement selection will be discussed in Chapter 3, and the applications of the pole and zero sensitivity for the testability analysis and the test measurement selection will be discussed in chapters 4, 5, 6, and 7.

2.4.4. Symbolic Modeling

Symbolic modeling of analog circuits is usually achieved at the circuit level of abstraction to generate a closed-form analytical expression for circuit characteristics as a function of independent variables (time or frequency) with a part or all of circuit's elements represented by a symbol [Giel94]. This allows for understanding the circuit behavior more effectively than the numerical analysis. The symbolic analysis can be employed for various applications for analog integrated circuits such as circuit analysis, circuit behavioral modeling, automatic circuit sizing, circuit optimization, and analog testing [Somm99].

Normally, the symbolic analysis is used to analyze linear circuits in the frequency domain. The transfer function (the ratio of the desired output to the input of a circuit) is generated in rational form as a function of the complex frequency s. The coefficients a_i and b_i of the numerator and denominator polynomials are a function of the circuit elements.

$$H(s) = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_m s^m}{b_0 + b_1 s + b_2 s^2 + \ldots + b_n s^n} = \frac{\sum_{i=0}^{m} a_i s^i}{\sum_{i=0}^{n} b_i s^i} = \frac{N(s)}{D(s)} \qquad (2\text{-}11)$$

where m and n is the degree of the numerator and denominator polynomials, respectively.

The small-signal models of the nonlinear elements such as diodes and transistors are generated (linearization about the *DC* operating point). The symbolic analysis is performed to extract the symbolic transfer function. There are three classes of symbolic analysis [Hass98]: (1) algebraic methods such as interpolation method and parameter extraction method, (2) graph-based methods such as tree enumeration and signal flow graph, and (3) matrix-based methods such as determinant-based solutions and parameter reduction solutions.

In algebraic methods, the circuit is represented by a set of equations; then, algebraic operations on this set of equations are achieved to obtain the symbolic network function. In graph-based methods, the circuit is represented in a graph with symbolic branch weights. The network function is computed by finding all paths and loop in this graph. Matrix-based methods generate the fully symbolic circuit equations directly from the circuit description and then putting them into a linear matrix form (the equations (2-1), (2-2),and (2-3) [Anal01].

Since the generated expression is large and difficult to interpret, approximation (simplification) is required to reduce the expression complexity by the sacrificing its accuracy. The sim-

plification methods can be divided into three groups according to whether the simplification of the network function is achieved after, during or before generation [Half03].

The simplification after generation (SAG) methods simplify the network function after obtaining their exact solution, hence called solution-based method. The simplification during generation methods (SDG) apply simplification during the process of the transfer function calculation. Simplification after generation methods (SAG) such as equation-base approximation or matrix approximation simplify the transfer function directly based on the numerical reference called design point. The symbolic analysis is usually completed by the extraction of the poles and zeros of the analog circuits and sensitivity analysis in symbolic form. The symbolic analysis can be summarized as shown in Figure 2-8.

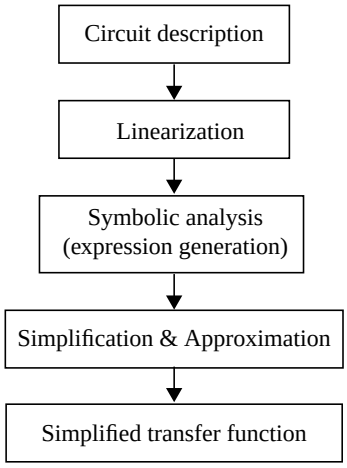


Figure 2-8: Symbolic analysis steps

The main disadvantage of the symbolic analysis is the limit for small analog circuits since the exponential grows of the number of terms with the circuit size. Therefore, many developments in symbolic analysis are proposed for the reduction of the complexity of the symbolic analysis for large circuits. Some of these developments are: hierarchical methods based on the sequence of expressions [Giel94], determinant decision diagram (DDD) [Shi00], and semi-symbolic analysis (combining symbolic and numerical analysis) [Somm99, Biol01, Somm03].

Chapter 3

An Introduction to Testing of Analog Circuits

Analog and mixed-signal circuits are gaining popularity in various applications such as telecommunications, multimedia, biomedical applications and others. The trend of integrating complete analog/digital systems on a single chip has resulted in new challenges in testing such systems. The analog test cost compared to its digital counterpart is very high. Furthermore, analog testing is still quite immature in both methodologies and tools. Therefore, the need for developing new test methodologies is still insisted upon.

In this Chapter, a general introduction to testing analog and mixed-signal circuits will be presented. In section 3.1, the difficulties result in a very complicated task for developing and automating methodologies for testing analog circuits are given. In section 3.2, the analog test flow and its relationship to analog design will be discussed. In section 3.3, the analog testing techniques -specification-driven test and fault-driven test- are addressed. The fault classification for analog circuits is given in Section 3.4. The current state of the art of testing analog and mixed-signal circuits is presented in Section 3.5.

3.1. Difficulties with Testing Analog Circuits

The natural properties of analog signals and analog test complexities can be summarized as follows [Huer93a, Sach95, Spaa96,Vinn98, Bush00]:

1) Analog signals are time and amplitude continuous in nature. Unlike digital signals, which are represented only by two values (low and high), analog signals are represented in principle by an infinite number of signal values which present signal information. Analog sig-

nals are very sensitive waveforms, even a small disturbance of signal magnitudes may cause a serious degradation in signal quality.

2) Analog circuits are inherently nonlinear systems. The user assumes that the nonlinear circuit operates as linear within a region of its input space. In addition, the nonlinear input-output characteristics of analog circuits need sophisticated techniques to solve the nonlinear equations that describe circuit behavior (e.g. iterative methods to solve the nonlinear equations of transient analysis in analog circuits).
3) The relationship between input and output in analog circuits is very complicated in comparison to digital circuits which can be described by the truth table or boolean equations and are thus precise and easy to model.
4) Analog circuits can be described in several domains such as frequency and time domains. Each of these domains has its own specifications and methodologies for describing analog circuits.
5) In digital circuits, only a few specifications have to be measured (rise time, fall time, delay time, logic threshold voltage, and so on). These specifications are usually the same for all digital circuits and independent of applications. In contrast, analog and mixed-signal circuits include several kinds of classes or models e.g. filters, operation amplifiers, A/D and D/A converters, phase-locked loops, and so on. Each circuit class has a separate set of specifications that is different from other classes. Furthermore, these specifications depend on a particular application even for the same circuit. Thus, checking the parameters related to these specifications can generally be costly and time-consuming.
6) Circuit element values vary widely which so caused by manufacturing process variations. Therefore, the circuit functionality depends on process variations, and the analog circuit is designed to depend on the range of element values rather than individual component values. The acceptable range of element values and circuit functionality (tolerance) depends on several factors such as intended applications, simulation inaccuracies and measurement errors.
7) The fault model complexity in analog and mixed-signal circuits is different from that in digital circuits. In digital circuits, the stuck-at fault model is widely used at gate level [Abra91]. In contrast, in analog circuits accurate analog fault models are not always available. Also, describing the good and faulty circuit for all types of faults at higher levels such as the behavior or the macro-model level is a very complicated task and still remains a challenge in analog circuit testing. Several fault models at different abstraction levels are

proposed. Furthermore, probability methods are often not efficient because the statistical distributions of analog faults, generally, are not known with enough precision to accurately predict the fault coverage of a test set.

8) As the technology is shrunk down and analog and digital circuits coexist on a single chip (System-on-a-chip), the accessibility to circuit nodes from IC pins is reduced. Therefore, the controllability and observability of circuit nodes are reduced. This growth of integration demands techniques for modifying the design such as design for testability (DfT) and built-in self-test (BIST) to ensure a higher testability of analog circuits.
9) Standard mixed-signal DfT and ATPG methodologies are not available. Each company has its own methods for test node access and test signal generation. The lack of standards leads to a long design cycle, long test development time, and increasing time to market.
10) There is no general agreement in the analog design community about the actual abstraction levels and hierarchy to be used in analog design automation.
11) In addition to the above-mentioned problems, there are further problems in testing of analog and mixed-signal circuits such as measurement errors, random noise effects, the effect of the load of the measurements probe, and environmental conditions like temperature.

The significance of these difficulties is not the same. The diversity of the specifications for characterizing an analog circuit and the lack of fault models are considered the most critical issues.

All of these difficulties make the automation of the analog test process to be a very complicated task. It also explains why nowadays analog testing is far behind its digital counterpart. Also, these difficulties lead to the need for producing very expensive analog test equipment to obtain precise signal measurements.

3.2. Test Flow

Test can be carried out during different phases of integrated circuit (IC) design. According to Figure 3-1 [Engi00, Huer93a], the first step in test flow is the IC specifications. At this step, specifications are usually given in terms of transient and steady-state performances. A circuit is designed so that its specifications fulfill the requirements specified by the user.
The second step is the design and its validation. The goal of this step is to ensure that the design obtained as an outcome of the design process is correct.

The third step of the test flow is *prototype manufacturing and testing*. Prototype testing is primarily aimed at verifying the circuit under test (CUT) characterizations and to certify that CUT can be sent to mass production, where an exhaustive test must be applied to identify any fault or any disparity with the required specifications. Therefore, prototype testing is focused on design mistakes rather than on manufacturing defects. Prototype testing consists of two stages: design debug and design evaluation. The design debug ensures that the circuit under test (CUT) performs its intended functions correctly using measurement instruments such as waveform generators and oscilloscopes. For example, in order to ensure that the filter behaves as designed, its frequency response and some transient characteristics such as settling time and rise time need to be tested. The design evaluation is performed by measuring specified performance specifications under many different conditions such as a range of temperatures and input voltages to evaluate worst-case conditions.
In prototype testing, the main specifications of a CUT are checked. If it does not operate as expected, a diagnostics technique is employed to detect and locate faults responsible for the malfunctioning and to decide whether a circuit requires modifications in circuit design in order to enhance the yield of the IC. As prototype testing is performed on only a small number of ICs, the test time is not a primary limitation. However, the most important factor is the accuracy of the measurements which requires very expensive automatic test equipment.

After a design is manufactured, the fourth step of test flow, which called *production testing*, is performed. The target of the production testing is to detect the defects resulting from the imperfections of the manufacturing process. Production testing is performed to make a fail/pass decision, or to distinguish good circuits from faulty ones. Testing cost (reflected as test time, throughput and the cost of automatic test equipment) is a major concern of production testing. Since packaging and final test are more expensive than all other manufacturing steps, an additional testing stage called *wafer test* is added before packaging. At the wafer test stage, simple parametric tests e.g. DC and low-frequency AC signals are carried out to detect faulty chips. Faulty naked dies are rejected and fault-free dies are packaged. Then, the final step of CUT testing called the *final test* is achieved on packaged dies. In the final test, high frequency tests can be applied and a subset of specifications is carefully chosen for measurement. This subset of specifications must guarantee that no faulty chips are shipped. The time spent on production testing can be very long, therefore, the number of applied test stimuli and measurements must to be minimized.

After achieving the final test step, the chips are ready for shipping to the end-equipment manufacturer.

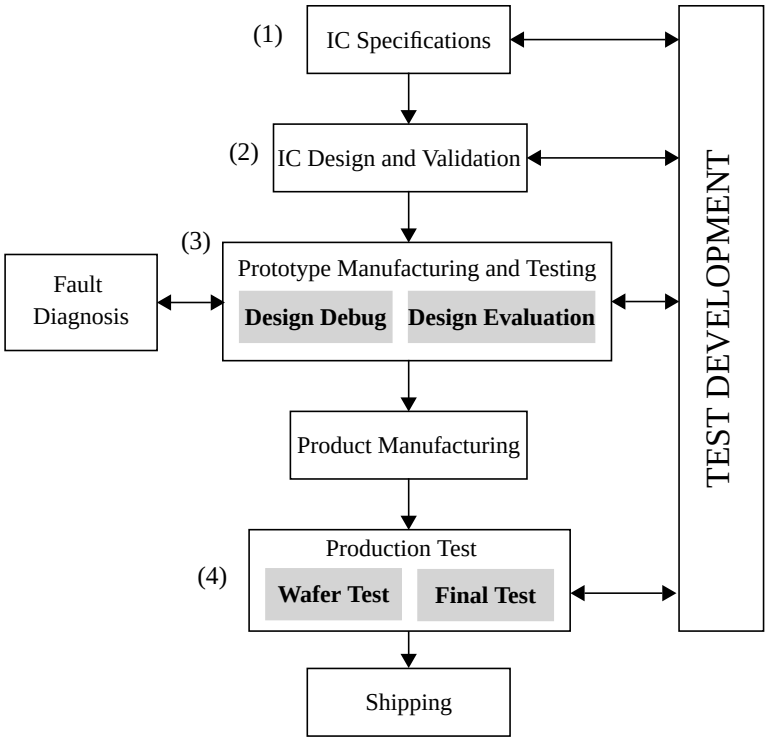


Figure 3-1: A general overview of the design and test flow for analog circuits

After shipping the chips, the board where the chip is embedded needs to be tested. Furthermore, the chip is tested during the operation in the field. Many faults may occur due to aging or environment conditions. In this case, a fault diagnosis is needed to segregate the faulty chips from the good ones.

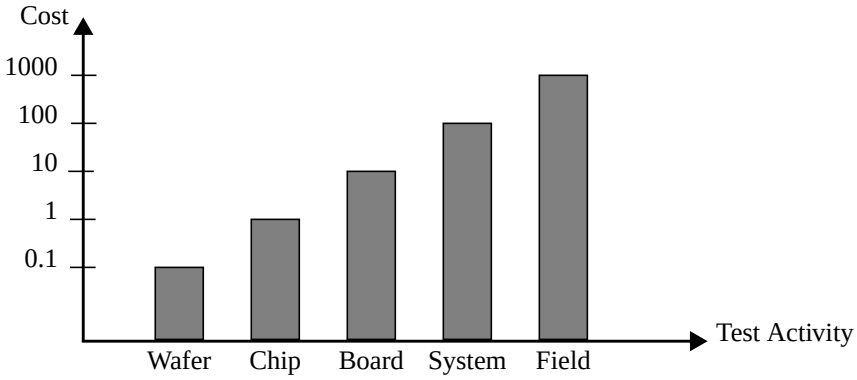


Figure 3-2: Test Economic

As a rule of thumb, the incremental cost of detecting, locating and repairing a fault through each successive phase of IC development is around ten times higher than the previous phase, as shown in Figure 3-2 [Robe01].

3.3. Fault Classification

Any deviation in the electrical or geometrical properties of the manufactured IC from the values given by the IC layout beyond the expected process variation is called a *defect* [Engi00].
The effect of a defect on the electrical characteristics of the IC deviating from the specified behavior is called a *fault* [Engi00].
In other words, a fault is the consequence of a defect, but it is also possible that a circuit with a defect electrically has no fault at all.

In this section, fault classification of analog circuit faults is given based on [Huer93a, Milo98, Engi00]. The sources of faults in analog circuits (process disturbance) are either global or local defects. Global defects include imperfect parametric control in IC manufacturing, instabilities in process conditions, material instabilities, substrate inhomogeneities and mask misalignments. Such defects affect all chips on a wafer in approximately the same way. On the other hand, local defects (such as spot defects, oxide pinholes, missing contact, etc.) are usually originated from particles in the fabrication process and affect individual devices or a very small region on a chip.

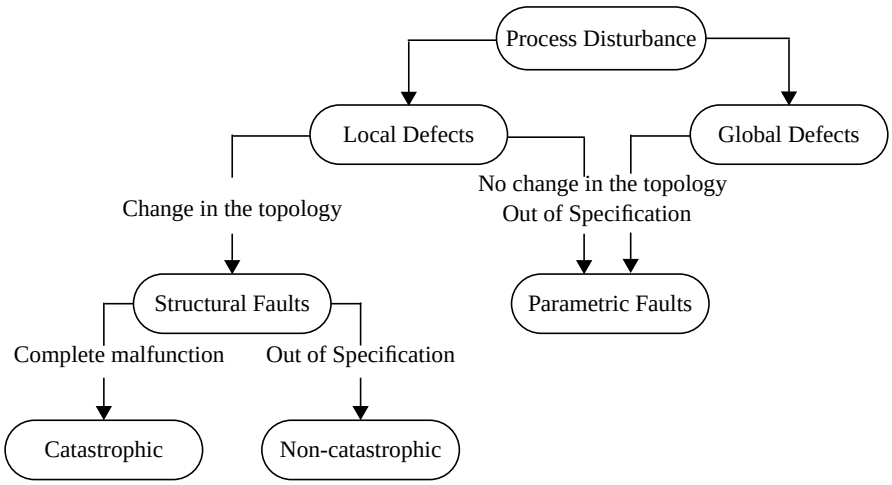


Figure 3-5: Classification of analog faults

Local and global process disturbances can result in *structural and parametric faults* (see Figure 3-5). The structural faults include open nodes, shorts between nodes, and other topological changes in a circuit. The structural faults can be categorized according to the effect of a fault on circuit specifications. A fault that causes circuit specifications to fail completely is called *catastrophic fault*. Typically, a simple *DC* test can detect this kind of fault. A fault that causes circuit specifications to operate out of their specified specification range (out of region of acceptability) is called *non-catastrophic faults*.

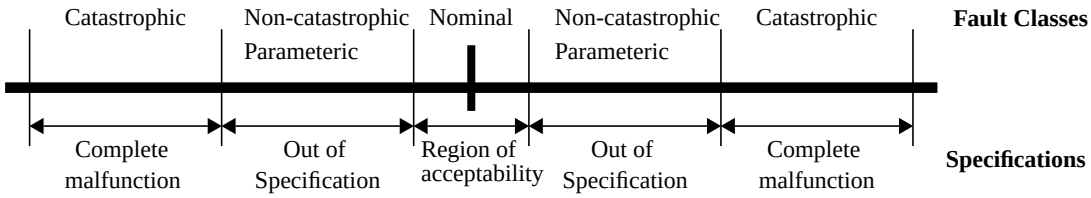


Figure 3-6: Specifications related to fault classes

Parametric faults indicate faults that do not change the circuit topology and only have an impact on parameter values (for example, cause a deviation in a resistance or capacitor value of 20%). Such faults result from local or global defects. Global parametric faults are due to imperfect process control in IC manufacturing. Such variations affect all transistors and capacitors on a die. Global parametric faults may or may not cause a circuit to fail specifications, depending on how this variation of a particular parameter changes the IC specifications. Local parametric faults are due to a local defect mechanism, like particles which enlarge a transistor's channel length [Milo98]. Parametric faults like the non-catastrophic faults cause the IC to operate outside of its expected specification range (see Figure 3-6).

3.4. Testing Techniques

Analog and mixed-signal testing techniques can be classified as either specification-driven or fault-driven test.

3.4.1. Specification-Driven Test

Specifications in analog circuits are often formulated as constraints on continuous functions of some independent variables [Huer93a]. The methodology which examines the performance of

the DUT and classify the DUT as fault-free (passed) or faulty (failed) according to the satisfaction/violation of their specifications is called *specification-driven tes*t. Such examinations can be carried out directly by applying a set of tests and measuring a set of output parameters and checking the measured parameters against an associated tolerance range.
The specification-driven test can be performed at different levels of the test flow. It could be applied at the prototype test stages (design debug and design evaluation) to ensure that the IC performs as specified, and at the chip level (production testing) to make a pass/fail decision. It is worth mentioning that today the specification-based testing methodologies dominate in analog testing because there is no general acceptance of analog fault models [Huer93a, Engi00].

Specifications can be defined in the multi-dimensional space called the *performance space* spanned by the *parameter space*. The parameter space is a *n*-dimensional space defined by circuit parameters, where *n* is the number of the circuit parameters. Every point in the parameter space represents a circuit. All these circuits have the same structure but different parameter values. In this space, a *tolerance region* R_T can be defined as shown in Figure 3-3(a). On the other hand, the customer's specifications are expressed in the performance space. If the bounds of the desired specifications are given, the *region of acceptability* R_A can be determined. The term *region of acceptability* R_A is used in order to indicate that all circuits within the performance tolerances given above are acceptable from the customer's point of view [Lito97].

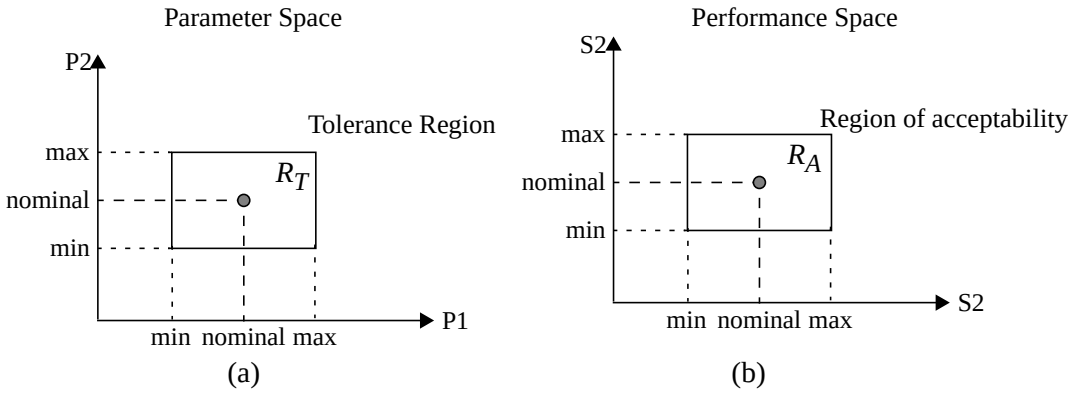


Figure 3-3: (a) The parameter space, (b) The performance space

An example for the two dimensions of the parameter space and the performance space is given in Figure 3-3 [Huer93a].

The relation between specifications and the region of acceptability is better understood in the parameter space, hence it is desirable to present both the tolerance region and the region of acceptability in the parameter space as shown in figure 3-4. In this case, the specification-based test would simply be the verification of whether the measured specifications are lying within the R_A in the performance space or not.

As a result of mapping the region of acceptability from the performance space into the parameter space, both regions will overlap. In this case, the *yield,* which is defined as the number of the of IC's that pass the test divided by the total number of IC's tested, can be determined by the number of fabricated circuits lying within R_A. Furthermore, *design centering* is the process which can be utilized to maximize the overlapping between R_T and R_A to enhance the IC yield [Spen88].

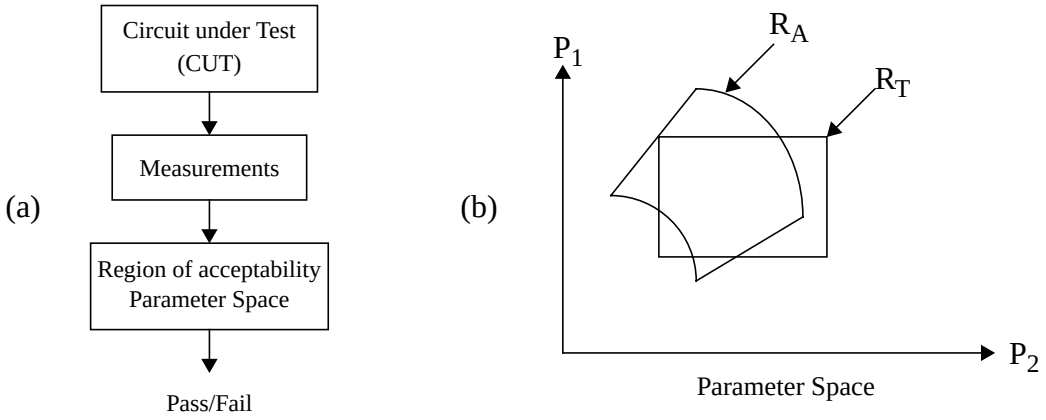


Figure 3-4: (a) The specification-driven test. (b) Overlapped the R_A and R_T in the parameter space

The specification-based test offers several advantages [Vinn98]. A circuit which passes the test process will meet a user's needs. Test generation is straightforward since tests can be generated directly from the specifications. Such an approach can adapt easily to the different types of circuits.

Unfortunately, evaluating all detailed specifications in analog circuits is not possible because it takes a considerable amount of time. For this reason, only a subset of specifications is chosen.

3.4.2. Fault-Driven Test

The *fault-driven technique* is used to detect a specific fault in an analog circuit, thus, a fault model must be available. In this sense, the fault-driven test is very similar to the digital testing techniques. A fault list is first constructed based on fault models. For each fault, a test signal is

generated, and the expected output is then measured. A judicious comparison is carried out between the actual circuit output according to a set of test signals and a pre-simulated output in order to estimate whether a probable fault exists or not. Fault-driven testing is concerned with the detection of a modeled physical defect (i.e. a fault), regardless of the satisfaction/violation of the specifications of the DUT.
The fault-driven test allows for the quantification of the effectiveness of any set of test signals in terms of *fault coverage*. Fault coverage is defined as the percentage of faults that can be detected divided by the total number of faults that are taken into consideration.
The main drawback of the usage of fault coverage as a degree of test effectiveness is the large amount of CPU time using standard analog circuit simulators such as SPICE. Furthermore, the fault-driven techniques for parametric faults are very limited in their ability.

3.5. Analog Test Issues

In this section, a general introduction of analog test issues will be presented based on the current state of the art of testing analog and mixed-signal circuits.

3.5.1. Analog Fault modeling

An effective fault model must be considered at each level of abstraction. Then the desired level is selected to simulate a faulty circuit based on the trade-off between the accuracy and the simulation speed.
The stuck-at fault model has been successfully used in digital circuits at the logical level (the gate level) [Abra90]. This fault model has led to effective digital testing issues such as fault simulation, test pattern generation, BIST and DfT. On the contrary, analog fault models are still a challenge in the analog test area.
As mentioned in Section 2.2, analog circuits can be modeled in three domains: structure, behavior, and geometry. Based on these domains, the techniques for analog fault modeling can be classified into three categories: structure-based, behavior-based, and geometry-based or layout-based.

- **Geometry-based approach**

The geometry-based approach depends on the technique of the inductive fault analysis (IFA) in which faults are derived from mapping defects (such as spot defects and variation in param-

eters) onto the circuit layout. This technique is known as *defect-oriented testing* [Meix91, Harv94, Sach95, Sebe95, Kuij95, Ohle96a, Ohle96b, Olbr96, Sach98, Vinn98, Prie98, Xing98, Engi00].

The defect analysis of a layout is carried out using defect simulators such as VLASIC [Walk86] and FABRICS II [Nass84]. The input of the defect simulator is the defect in the semicoductor process, information about process disturbance characteristics, a circuit layout, a nominal device models. The defect simulator employs this information to insert a defect into the circuit layout and to describe whether a defect causes a change in the circuit behavior. The output of the defect simulator is a list of circuit level faults caused by manufacturing defects. Faults in the fault list are ordered according to their probability of occurrence. The probabilities of occurrence of a fault are calculated using stochastic simulation methods such as the Monte Carlo simulation. The most likely faults to occur (high probability) are extracted from the fault list, this step is called *fault extraction*. Furthermore, many defects can be collapsed into a unique fault class. The fault list may contain structural faults (open nodes and short between nodes) and parametric faults (parameter variation) in active and passive elements, and may contain multiple faults as well.

- **Structure-based approach**

The structure-based faults can be modeled at different levels of abstraction of the structural domain. At the circuit level, the fault list is constructed directly relying on the schematic of the circuit without any knowledge about the physical layout and process information [Caun96]. Mostly, the fault list includes open and short faults modeled by high-value and low-value resistors, respectively. The fault list can be constructed either manually or automatically.

The main disadvantage of this approach is the high cost of simulation due to redundant, unrealistic and unlikely faults. Due to the long simulation time, it is therefore impractical to simulate a large circuit at the circuit level.

In order to alleviate the computational complexity at the circuit level, it is feasible to model the faults at higher levels of abstraction. However, this improvement in simulation speed will sacrifice accuracy. A macro-based fault model was proposed to model a fault at the structural marcomodel level of abstraction [Nagi92, Pan94, Naig96, Pan96, Pan97a, Pan97c]. The first step of the this approach is to construct the fault list containing structural and parametric faults at the circuit level. Circuit simulation is performed for each fault in the fault list. The faulty behavior of a circuit is modeled at the structural macromodel level based on the functional error characterization of the constituent primitive elements.

- **Behavior-based approach**

Although, the structural fault macromodel reduces the simulation complexity using less elements than the original circuit, the behavioral fault models reduce the complexity one step further [Soma96a]. The reduction of complexity stems from the possibility of using behavioral simulators based on hardware description languages such as VHDL-AMS, and the circuit under test is considered a black box. There are various techniques to model analog faults at the behavioral level such as regression analysis, radial basis function, and asymptotic waveform evaluation (AWE) [Nagi92, Nagi96, Perk98]. Once behavioral fault models are developed, they can be used to inject behavior-based faults on the behavioral macromodel level.

3.5.2. Analog Fault Simulation

Once the fault list is constructed, fault simulation is executed to evaluate fault coverage. A fault from the fault list is injected into a circuit under test. Test stimuli are applied at controlled nodes (mostly the input nodes) of the circuit. The simulation is running in order to determine the detectability of faults and to obtain the fault coverage. The fault coverage is defined as the number of detected faults divided by the number of total faults in a fault list. The detectability of faults is determined by a comparison of the good and the faulty responses of a circuit.

Analog fault simulation is traditionally carried out at the circuit level of abstraction. Many tools have been implemented at this level based on SPICE-like circuit simulators such as aFSIM [Stra00b] and AnaFAULT [Sebe96]. However, analog fault simulation for medium and large analog circuits is a very expensive task in terms of CPU time.
Several techniques are proposed to alleviate the complexity of analog fault simulation and to reduce the computational time. These techniques can be summarized as following:

a) Defect-oriented test techniques for fault modeling [Harv94, Sach95, Sebe95, Kuij95, Olbr96, Sebe96, Nagi96, Ohle96a, Ohle96b] are used to reduce the computational time by reducing the number of faults in a fault list. The reduction is achieved by:
   (1) modeling only realistic faults in contrast to constructing the fault list at the transistor level relying on the circuit schematic which contains unrealistic and unlikely faults,
   (2) truncating the fault list by considering the most likely faults to occur by weighing the faults. It is also possible to collapse the equivalent faults.
b) Several levels of abstraction in the behavioral view are used to accelerate the analog fault simulation [Nagi93, Bali96a, Vari97, Perk98, Stra01]]. Analog fault simulators such as

DRAFT [Nagi93a] and FLYER [Vari97] have been implemented at the equations level based on state-variable equations. The behavioral macromodel level is also used to accelerate the fault simulation one step further over the structural macromodel [Nagi96]. Traditional analog fault simulators such as aFSIM can be combined with a hardware description language such as VHDL-AMS to simulate the circuit under test in multi-level hierarchical manner [Stra01]. However, some problems may be encountered through hierarchical analog fault simulation [Stra97, Perk98].

c) The fault simulation can be accelerated by employing specific features of the fault analog simulator itself [Vinn98]. For examples:
   1. Complementary pivot method is used for *DC* fault simulation of nonlinear circuits [Vinn98, Bush00].
   2. One-step relaxation and fault ordering methods are used for nonlinear *DC* fault simulation [Tian98], and for nonlinear transient fault simulation [Engi00, Engi03].
   3. The concurrent analog fault simulation method is used for nonlinear *DC* and transient fault simulation [Zwol97, Yang99]. The reduction in *CPU* time is reported in [Yang99] to be 56% for *DC* analysis and 61% for transient analysis over traditional analog fault simulators at the transistor level.

d) Distributed platforms are used in [Holu96] to speed up the analog fault simulation based on the concept of fault groups. Several different networks connected in parallel are simulated with the same input stimuli. The fault list is divided into several fault groups related to the number of available workstations.

Specifications selected to be measured play a great role in maximizing fault coverage in fault simulation. In this thesis, we will propose a measurement selection algorithm that reduces the test cost without sacrificing fault coverage.

3.5.3. Test Signal Generation

Test signal generation is required for deriving input signals which maximize the difference between the good response and the faulty response of a circuit. The shape of the input signals can be beforehand assumed such as *DC*, sinusiodal waveform, step, ramp, etc. Thus, the goal of the test generation algorithm is to find some properties of the input signal such as the frequency of the sinusiodal waveform.

Fault models can be either parametric faults or structural faults. Hence, test signal generation approaches can be divided into two classes, the first class of test signals is used to detect parametric faults and the second class to detect structural faults.

- **Test signals for detecting parametric faults**

Many test signal generation approaches for parametric faults are suggested in the test literature [Soma96b]. The test signal generation approach for linear analog circuits based on signal flow graphs (SFG) and reverse simulation is proposed in [Rama99]. A circuit is represented by its transfer function and corresponding signal flow graph. Reverse simulation is used to invert the signal flow graph. Analog backtrace technique (backward from the primary output to the primary input) is used to generate the input signal and to compute the tolerance of the circuit elements.

The test signal generation task can be formulated as an optimization problem such as a quadratic programming problem [Tias91] and minmax optimization problem [Abde96].

The sensitivity analysis is employed for generating test vectors [Saab96, Hami96, Vari00]. In this approach, the differential sensitivity is computed using the adjoint network method. Then, the faulty element's relative deviation is computed using the output performance and the fault-free elements. A set of test vectors is generated which maximizes the observability of the faulty element on the output performance. The differential sensitivity is accurate for modeling small deviation faults, but it becomes inaccurate for modeling large-deviation faults. Hence, the incremental sensitivity has to be used to generate test vectors for large deviation faults [Slam95].

The sensitivity analysis can be used with nonlinear programming [Burd01] or with statistical methods [Saab00, Chan02] to generate test vectors for testing parametric faults.

A test signal generation algorithm based on search-based heuristic is proposed in [Bali96b, Bali96c] for testing parametric faults in linear analog circuits. The good and the faulty circuits are represented by their transfer function in the pole residue form. The golden-search and the false-position technique are employed to search for a frequency that maximizes the steady-state response's amplitude or phase error.

Test signal generation based on pseudorandom testing which is similar to the digital linear feedback shift register (LFSR) is proposed in [Pan97b, Pan99]. The linear analog circuit is embedded between a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC). Pseudorandom test patterns are applied to DAC which converts the digital signal into the analog one applied to the circuit under test. The circuit is simulated for each pattern, and

the signature of the circuit is labeled as passed/failed. The cross-correlation is chosen as a signature in [Pan97b] which can be calculated using digital signal processing (DSP).
The test generation task can be formulated as a linear discrimination problem [Pan99]. The region of acceptability of circuit specifications is defined by a set of hyperplanes in a multidimensional space formed by a set of parameters of the circuit under test. The pattern classification algorithm employs test patterns to classify the hyperplanes and to determine whether the CUT is with the region of acceptability or not.

- **Test signals for detecting structural faults**

If the structural faults result in the complete absence of the desired function, *DC* testing, in the most cases, is effective in detecting such faults. In [Deva94], The *DC* test generation problem is formulated as a minmax optimization problem. This algorithm is developed in [Deva95] for the dynamic case. In [Stra02, Stra03], the *DC* test generation technique based on nullators and nurators for linear and nonlinear circuits is proposed.
The test signal generation based on the testability analysis is proposed in [Huyn99, Soma01, Stan02]. The testability for the good and the faulty circuit is determined, then the difference between the testability of the good and the faulty one is evaluated in the frequency domain. The Inverse Fourier Transform is employed to obtain the test signals in the time domain.

3.5.4. DSP-Based Testing

The functional DSP-based testing technique is the method which is often used in production environments for testing analog and mixed-signal circuits. DSP-based testing enables the test engineer to manipulate the test of analog and mixed-signal circuits using applications of high-speed D/A and A/D converters and a very fast DSP-processor.
In DSP-based testing, the function of analog hardware instruments is replaced by computer software, this process is referred to as "*emulation*". In the DSP-based system, the currents or voltages are represented by numerical vectors that can easily be analyzed, transferred and saved by DSP instruments [Maho87, Bush00].
The structure of the DSP-based system is shown in Figure 3-7. The test engineer creates the test stimuli described as a vector (block of patterns). The *synthesizer* feeds the patterns to the D/A converter through the RAM memory. For periodic waveforms, the patterns are usually fed in a continuous loop. If a transient waveform is desired, the vector is converted only once, and the loop is terminated. The D/A output is de-glitched to remove hazards and passed through a

reconstruction filter to obtain the continuous, band-limited waveforms. The resulting analog signal is then applied to the circuit under test (CUT) which generates the output response in analog form. The *digitizer* digitizes the analog response using a high-speed A/D converter and passes it on to the DSP instruments for further processing. The RAM in digitizer waveform collects the samples until the desired measurement is terminated.

When the output of the CUT produces digital waveform (mixed-signal circuits case), the output patterns are collected by a temporary RAM called the "*received memory*" and is then sent as vector to the processor. Similarly, when the input of the CUT is in digital waveform instead of analog, the test stimulus vector is transmitted by a RAM called "*send memory*". The vectors are transmitted in the DSP-based system in a burst mode. The burst mode allows the transmission of a large number of vectors accompanied by the start address and information about the vector length. Synchronization is required to keep clocking everything together and gives the DSP system a coherence property in which all frequency and time functions are programmable related in exact whole-number ratios.

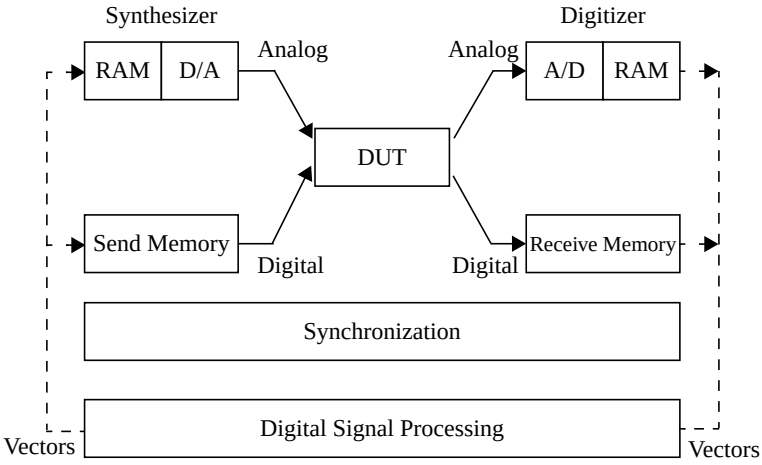


Figure 3-7: DSP-based testing structure [Mah87]

DSP-based testing is a powerful methodology that offers several advantages in comparison to traditional analog test and measurement techniques [Maho87, Bush00].

DSP-based ATE is more accurate than a pure analog test instrument, since the measurement and noise effects are reduced by digitizing the analog waveform at the earliest opportunity. The DSP-based testing is more time-efficient than analog instruments since many measurements can be parallel carried out. Furthermore, in DSP-based testing very fast analysis techniques are used to perform the measurements such as Discrete Fourier Transform (DFT) and

Fast Fourier Transform (FFT). DSP-based testing can speed up the production test and increase the test throughput. Moreover, DSP-based ATE are flexible and repeatable instruments since the instruments are digital, rather than analog.
In contrast, DSP-based testing has also several liabilities such as being expensive, flexibility can be lost by unskilled engineers, and the test engineer needs to understand the theory of the instruments and to know the physical and mathematical principles of the measurements.

3.5.5. Design for Testability (DfT)

Test nodes play a great role for testing analog and mixed-signal circuits. Test nodes may be required for several purposes:
1) to excite the test signals (stimuli) at controllable nodes into embedded modules,
2) to perform measurements at observable nodes to obtain the circuit responses, and
3) to isolate the faults in fault diagnosis approaches.

Due to accessibility limitations resulting from increasing the integrity of the ICs, DfT methodologies are required to improve the circuit testability in terms of improving controllability and observability of internal nodes. As a result, DfT techniques are aimed at accessing the internal nodes for testing purposes by adding an additional hardware in order to support high fault detectability and reduce the total test costs of ICs by reducing testing time.
DfT techniques can be divided into two categories: reconfiguration-based DfT and accessibility-based DfT [Chat97].

3.5.5.1. Reconfiguration-Based DfT

Reconfiguration-based DfT techniques rely on a reconfiguration of the circuit under test to improve their testability. These techniques were developed to improve the controllability and observability of internal nodes for specific classes of circuits such as active filter with cascaded stages [Soma90], switched-capacitor filters [Soma94, Huer93b], operation amplifier [Brat95, Reno98].

3.5.5.2. Accessibility-Based DfT

Accessibility-based DfT techniques are used to improve controllability and observability for analog and mixed-signal circuits by extending the digital DfT techniques such as scan chain, boundary scan, and test bus to test analog and mixed-signal circuits.

- **Scan Chain Technique**

In scan chain techniques (see Figure 3-8) [Kerk94], there are two modes, one for tests and the other for normal operations. The nodes of interest are connected to an analog shift register through switches and buffers. The switches are used to isolate the analog shift register from the circuit during normal operation. The buffers are used to minimize the influence of the test hardware on the measured nodes.

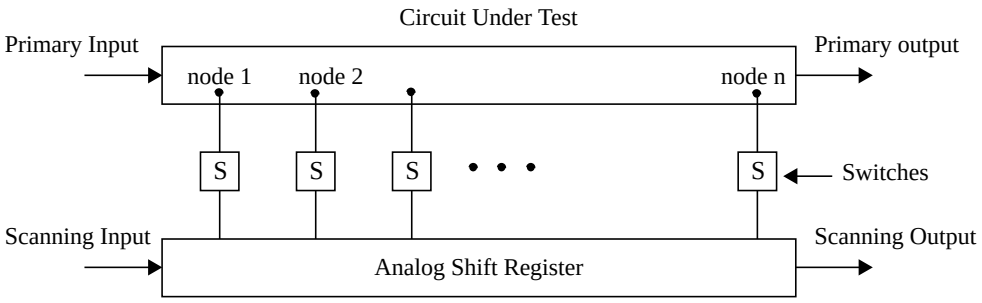


Figure 3-8: Scanning Techniques [Kerk94]

In the first step of the test mode, the test data are sampled at measured nodes and stored in capacitors by closing the switches to the circuit under test and opening the switches of the analog shift register. In the second step of the test mode, the connecting switches are open and switches of analog shift register are closed. In this way the stored information in the capacitors can be shifted by a simple digital shift register to a scanning output. This technique is referred to as Bucket-Brigade-Like Devices.

An improvement to this technique can be carried out using the Charge-Coupled Device (CCD) to implement the analog shift register. The principle of this technique is similar to the Bucket-Brigade-Like Devices technique except that the discrete analog information is handled in the form of charges. The conversion of input voltages and currents into charges is carried out by charge converters (CC). At the output the charges are converted back into voltages and currents.

- **Boundary Scan**

Boundary scan techniques utilize ADC and DAC converters which are existed in many mixed-signal circuits. ADC and DAC converters are used to digitize the analog outputs before storing them in the scan cell registers and shifting them to external pins, and to convert digitized analog inputs to be shifted into the scan path to primary output as shown in Figure 3-9 [Milo98].

The analog inputs can be controlled by primary inputs, and the analog outputs can be observed by primary outputs of the analog part.

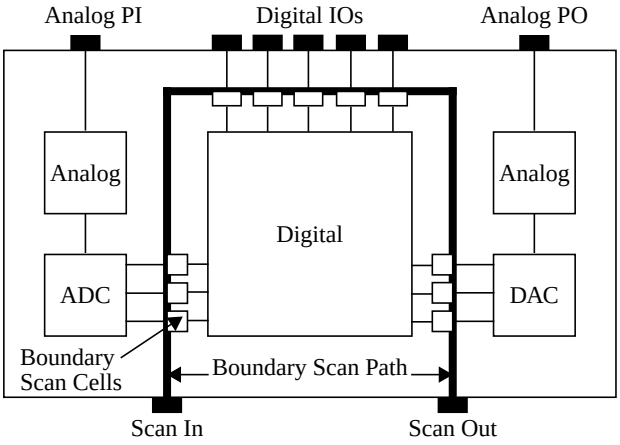


Figure 3-9: Boundary Scan Techniques [Milo98]

In this technique, the analog tests are separated from digital ones, furthermore, the analog parts of a complex mixed-signal circuit should be divided into analog blocks i.e. filters, operation amplifiers, ADCs, DACs, phase-locked loops and others to enhance their ability of identifying the faulty blocks. The identification of the faulty blocks can be achieved using analog shift registers and storage elements similar to the scan chain techniques.

- **Analog Test Bus**

The analog test bus is widely used to access the internal nodes of a mixed-signal circuit where the nodes of interest are provided for controlling the input stimuli (analog test bus AT1) and observing the associated response (analog test bus AT2) as shown in Figure 3-10 [Robe97].

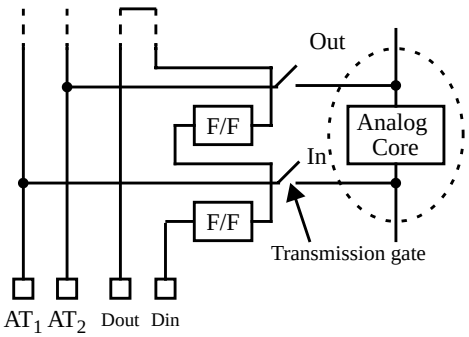


Figure 3-10: An analog test bus configuration [Robe97]

Recently, a standard analog test bus for mixed-signal circuits called IEEE P1149.4 was defined. The IEEE P1149.4 is extending to IEEE 1149.1 for digital circuits [Soma96c, Sunt96, Sunt99, Osse99, Kac03]. The IEEE 1149.4 standard analog test bus can detect open and short faults in a board's wiring interconnection which consist of 80%-90% of all board failures.
The standard is aimed at board level, thus the other analog test problems at other IC test levels (cf. Section 3.2) are not solved using this standard.
In summary, the IC developers are often not very willing to insert DfT structures into their analog circuitry because of the risk of degrading the performance, especially for high frequency and high performance circuitry. Moreover, the DfT approaches require additional circuitry which increase the chip area. The additional circuitry increases the die manufacturing costs and the probability of faults in the chip.

3.5.6. Built-In Self-Test (BIST)

The idea of BIST is to build some parts of the test circuitry (i.e. test generators and response analyzers) on the same die as the desired circuit [Sunt96]. Such structures can provide many advantages for testing analog and mixed-signal circuits [Robe97]:

(1) facilitation of design for test,
(2) a hierarchical test solution for all test levels (wafer, package, board and system),
(3) a reduction in interconnection length and device loading effects, and
(4) standardization which simplifies the automation and the integration of test into present day CAD facilities.

BIST methodologies are often aimed at specific analog and mixed signal circuits such as ADC/DAC converters and filters. In this section, we will discuss the relevant BIST schemes reported in the test literature.

- **BIST for mixed-signal circuits**

The *hybrid Built-In Self-Test (HBIST)* [Ohle91, Ohle96] is used to test mixed-signal circuits which include a complex digital kernel system and peripheral analog sub-circuits at the input and the output (A-D-A structure). Multiplexers implemented by CMOS transmission gates are used to isolate the circuit under test from the environment and place it in the test mode. The test process is performed in two sequential steps, the first step for testing the digital kernel system and the second for testing the analog sub-circuit. In this structure, shift registers such as

“BILBO” or “LFSR” registers and the multiple input signature register (MISR) are used to achieve the test pattern generation and the signature analysis on the chip.

The *mixed Analog Digital Built-In Self-Test (MADBIST)* [Tone93, Robe97] is based on the A-D-A structure and employed for mixed-signal telecommunication ICs such as MODEM and CODEC for the signal-to noise ratio (SNR) test. The digital kernel system of this structure is a DSP. The test stimuli is generated relying on the oversampling sigma-delta modulators [Veil95, Robe95, Huar98, Dufo99, Dufo00]. The single tone signal such as sine wave or multi-tone test signals [Lu94] can be generated using the sigma-delta modulator. The evaluation of on-chip measurements such as the SNR can be carried out using a kernel DSP.

The *Histrogram-based Analog Built-In Self-Test (HABIST)* [Fris97] assumes the CUT is embedded between D/A and A/D. The histrogram of the CUT is used as a signature. The test stimulus vector can be generated from an external generator or a built-in generator. An access method to each test point is provided, and the histrogram of the signal at each test point is generated. Finally, the signature of the CUT is obtained by comparing the histrogram of the CUT with the one expected.

The *oscillation Built-In Self-Test (OBIST)* [Arab97] is based on an oscillation-test strategy which converts the circuit under test into an oscillator in the test mode. The oscillation frequency of the circuit under test is evaluated on-chip by a digital circuitry and compared with a fault-free one to decide whether the CUT is faulty or not. The main advantage of this structure is that it does not require test vector generators.

- **BIST for analog circuits**

BIST techniques for analog circuits are proposed for specific classes of circuits. A BIST approach for switched-capacitor filters is proposed in [Huer93b]. This approach exploits the fault tolerance technique (hardware redundancy) using partial replication of the circuit under test. The resulting continuous signals can be compared in the time domain via a circuit voter. Also the authors in [Chat93] utilize the hardware redundancy to develop a BIST (concurrent error detection) scheme based on the continuous checksum for linear analog circuits represented by state variable equations.

In [Chao95], the authors suggest BIST and fault diagnosis techniques for analog circuits in the frequency domain. This scheme exploits the following circuits: (1) the white noise generator as a test generator, (2) the programmable window filter to select the frequency range of interest, and (3) the peak detector to detect the peak response at a certain frequency point or in a frequency range.

In [Mir97], a BIST methodology was developed for sigma-delta modulators based on a circuit reconfiguration and comparison. In this methodology, a test stimuli generator is assumed to be available on-chip to generate single or multi-tone test signals. This structure is used for the production test due to the short time testing as well as not needing any digital signal processing capabilities. In [Mir96b], unified BIST approach is suggested for fully differential analog circuits based on boundary scan techniques. In [Chat96], a low cost *DC* BIST technique is developed for linear circuits. A simple *DC* generator and error checking circuitry are implemented on-chip.

In [Vari00], the authors propose a BIST structure to improve the fault detectability in the time domain. Pulse trains with a varying pulse width are generated using a digital LFSR serving as transient test stimuli for the CUT. The signature is a sequence of digital bits resulting from the comparator with a reference voltage. Traditional scan techniques can be used to analyze the obtained signature.

The main shortcoming of the BIST technique is the need for extra on-chip hardware which may cause the degradation of the system performance and leads to an increase of the chip area overhead.

3.5.7. Fault Diagnosis

The analog fault diagnosis [Band85, Liu91, Huer93a] is usually required at the earliest stages in the test flow like e.g. the design characterization stage. Since the fault diagnosis becomes a very expensive task at higher levels of the test flow, it is in some cases not possible to repair or replace faulty components at the board level. The fault diagnosis is utilized (a) to determine the cause of the failure for analysis and correction purposes, and (b) to modify the circuit to be less sensitive to the faults.

The fault diagnosis concentrates on the following processes: fault detection, fault location and fault identification. The fault location problem intends to locate faulty elements, whilst the fault identification problem concentrates on the computation of actual element values from measurements.

The fault diagnosis methods can be generally divided into simulation before test (SBT) and simulation after test (SAT). Simulation before test techniques [Cate96, Fann99, Liu99, Yoon99, Amin00, Raja00, Amin01] are normally used to locate and identify structural and local parametric faults, while simulation after test techniques [Wey87, Liu91, Slam92, Huan98, Cher99, Wors00, Cher01, Star01, Liu02] are employed for global parametric faults.

Simulation before test (SBT) consists of three tasks: (1) fault dictionary construction, (2) optimum test stimuli generation and measurement selection, and (3) fault identification.

The fault dictionary can usually be built up using fault simulation. The fault-free circuit is first simulated, then the faulty circuits are simulated. The good and the faulty responses are collected and stored in a look-up table called *fault dictionary.* The stored circuit responses in the fault dictionary may be DC, AC and time-domain signals. Therefore, the approaches to construct the fault dictionary can be classified according to the kind of circuit analysis, DC, frequency-domain and time-domain approaches [Band85].

Optimum measurement selection is aimed at reducing the number of measurements without affecting the diagnosibility of a circuit, in other words to ensure that all faults in circuit elements can be identified. On the other hand, the input stimuli are carefully selected to excite the CUT so that the effect of a fault can be propagated to an observable node.

Some faults have the same effect on the circuit response. Such faults should be aggregated in groups called *ambiguity groups* [Sten89]. Consequently, it is desirable to determine ambiguity groups before performing the fault location process.

The actual values of measurements are compared with measurements which are stored in the fault dictionary in order to identify the faults. Hence, the fault identification process can be considered as a pattern recognition problem. The techniques that are used in pattern recognition such as maximum likelihood measures, fuzzy distance, matching methods and neural networks can be applied for fault diagnosis of analog circuits.

The main shortcomings of SBT techniques are: (1) They rely on the fault model. (2) It is time-consuming since each fault in the fault list should be simulated. (3) The size of the dictionary may cause a storage problem.

Simulation after test employs the circuit topology and a set of measurements to solve a set of independent equations in order to estimate the element values of a circuit. If the number of independent measurements is large enough, in this case all circuits elements can be identified. In contrast, if a limited number of measurements are avaliable, thus, a few faulty elements can be identified. In this case, the circuits elements are partitioned into two groups, a fault-free group and a faulty group [Band85]. The deviation of the elements in the faulty group can be determined by using the measured data and nominal values of circuit elements in the fault-free group. The deviation of the circuit elements is obtain by solving fault diagnosis equations. If the element values are outside of the tolerance range, the elements are regarded as faulty.

3.5.8. Testability Analysis

The testability analysis concept has been described in several ways [Huer93a]. Coming from fault diagnosis, testability is strictly tied to the concept of the element-value solvability problem, which gives information about the solvability of the analog test problem [Mane98]. The testability analysis provides prior information as to whether the problem is uniquely solvable or not. This information includes optimal test points, optimal measurements, ambiguity groups, testable elements (which are can be isolated) and untestable elements (which are assumed to be nominal).
The testability measure is given quantitatively by the rank of the sensitivity matrix constructed from the derivatives of output performances with respect to circuit elements.
On the other hand, the testability analysis as coming from the digital test is based on the combination of the controllability and observability of a circuit node.
The testability analysis can be also defined as the relative degree of difficulty in testing of circuit nodes, elements, or key parameters for particular fault models and given test signals [Prie81, Beck94, Beck95, Kerk94].
The testability analysis algorithm can be used as a guideline for test signal generation, design for testability, measurement selection, and fault diagnosis.

The testability analysis of analog circuits is achieved in many previous works based on the sensitivity analysis. The sensitivity-based testability analysis starts with calculating the circuit transfer function of a circuit. The sensitivity matrix (Jacobian Matrix) is constructed by differentiating the transfer function with respect to the circuit elements in the frequency domain [Iucu86]. The testability measure is evaluated mathematically by the maximum number of linearly independent columns (column-rank of the Jacobian matrix) [Sen79]. If the rank of the Jacobian matrix is equal to the number of circuit elements, this indicates that all faults in circuit elements can be identified. Otherwise, additional test nodes must be added or the number of testable elements must be reduced to be equal to the rank of the testability matrix.
The similar algorithm can be utilized in the time domain for testing of nonlinear circuits [Beck94, Beck95]. The testability matrix (sensitivity matrix) is constructed as a function of the time. The testability measure is equal to the rank of the testability matrix.
In [Hemi90], rank-based approaches are combined with statistical methods in order to test nonlinear circuits. After dependencies among the circuit parameters are detected, the dependent elements are removed from the sensitivity matrix. Furthermore, the approach selects an

optimal set of measurements taking the measurement errors into account to compute the determination accuracy of the circuit elements.

An improvement of the testability analysis in the frequency domain is proposed by constructing the testability matrix as polynomial matrix *P(s)* which is represented by a linear combination of suitable orthogonal polynomials [Cate87]. The testability measure *T* coincides with number of linearly independent columns of the proposed polynomial matrix $T = rank(C)$ where *C* is the matrix composed of the coefficients obtained by expanding the polynomials *P(s)* into a series of orthogonal polynomials.

A similar algorithm is proposed in [Liu96] for small linear circuits, however, the Jacobian matrix is constructed using the coefficients of the input impedance, the output impedance and the transfer function which are called the basic functions.

The above mentioned algorithms have several limitations:

- They suffer from numerical errors, thus the rank of the Jacobian matrix is considered an estimate of the true testability.
- The computational time is very long because it depends on the complex frequency *s* or time samples.
- The computation of the coefficients of the polynomial matrix and their sensitivities for large circuits is very high.

As a result, the testability analysis based on the symbolic analysis is a natural choice for overcoming these limitations.

In [Carm91], the polynomial matrix *P(s)* is generated from symbolic sensitivity functions in symbolic form. The numerical testability matrix *B* is constituted by the coefficients of polynomial functions of *P(s)*. The entries of the testability matrix are independent of the complex frequency *s*. The testability measure *T* is determined by evaluating the rank of the numerical matrix *B*. A further improvement for simplifying the symbolic computation was proposed by [Mane98, Fedi98a. Fedi98b, Fedi99]. The transfer function is expressed as a rational function and the numerator and the denominator of the transfer function are expressed as a polynomial. The Jacobian matrix B_c is constructed in symbolic form by the derivation of the coefficients of the numerator and the denominator with respect to the circuit elements. The testability measure is determined by evaluating the rank of the matrix B_c. The derivatives of the numerator and the denominator with respect to the circuit elements can be calculated using the symbolic analysis of analog circuits such as Determinant-Decision-Diagrams [Shi00, Pi02].

In low testability circuits, where the rank of the testability matrix is less than the number of the circuit elements, the testability analysis is strictly tied to the ambiguity group concept [Sten89]. An ambiguity group consists of the elements that produce the same values of measurements. Therefore, it is desirable to determine the ambiguity groups before constructing the fault diagnosis equations.
Several methods are proposed for identifying the ambiguity groups such as using QR factorization [Sten89]. The ambiguity groups can be determined by finding the null space of the testability matrix, in other words finding the linearly dependent columns of the testability matrix. The zero-value rows of null space matrix correspond to the definitely testable elements, and the nonzero-value rows and the not orthogonal rows correspond to the elements that belong to the same ambiguity group. The null space of the testability matrix can be computed by *QR* factorization [Star00, Pang01, Liu02] or by singular value decomposition (*SVD*) [Liu94, Mane03] of the testability matrix.

The testability analysis approach based on the testability transfer factor (TTF) is proposed in [Huyn98, Huyn99]. This algorithm is similar to the digital testability analysis techniques [John89] which combine the controllability and observability concepts of circuit nodes [John89, Abra90]. The testability transfer factors for fundamental analog circuit elements such as resistors, capacitors, diods, transistors, and others are calculated. The circuit is modeled using a signal flow graph (SFG) which represents the propagation of the test information from primary input to primary output. The TTF represents the weight of the SFG. The controllability and the observability of circuits nodes are calculated based on the TTFs of circuit elements. Then, they are combined to compute the testability for each node of a circuit. This algorithm can be used for test signal generation and for test node insertion [Zhan99].
There are some limitations to this algorithm: (1) it is very time consuming, and (2) TTF gives the low sensitivity of the parametric faults. Hence, hierarchical techniques can be utilized to speed up the computational time [Soma01]. In [Stan02], a new definition for the testability transfer factor is proposed to improve the low sensitivity of the parametric faults. However, solving the new nonlinear equations of the controllability and the observability is a very time-consuming task.

The testability analysis based on the component connection model (CCM) is proposed in [Chen79, Sen79, Wey87]. The circuit under test is represented by its component connection model (CCM) which can be described by these equations:

$$a = L_{11}b + L_{12}u$$
$$y = L_{21}b + L_{22}u$$

where u and y represent the column vectors of accessible test inputs and outputs, a and b denote the input and output column vectors, and L_{ij} are the connection matrices generated from the circuit topology. The global column rank of the matrix L_{21} determines the testability. In [Huan98a, Huan98b], an algorithm is developed to generate the matrix L_{21} which provides the maximum testability. This approach can be employed for the self-testing fault diagnosis [Wey87]. The elements of a circuit are divided into two groups, the first group contains the known good elements, and the second group contains unknown elements. The elements in the second group can be estimated based on the known elements, inputs u, and outputs y.
The self-testing approach is extended by [Ho01] for the hierarchical fault diagnosis of analog integrated circuits. Further applications for this approach are to develop a test program generator for the fault diagnosis of analog/mixed-signal circuits [Huan97], and to select test points to maximize the testability of the analog circuits [Huan98c].

In this thesis, a new testability analysis algorithm will be presented. This algorithm is based on the well-known pole and zero analysis. The analog circuit is represented by their transfer function in the pole-zero form. The testability measure can be easily computed depending on the number of the poles and zeros of the transfer function. The ambiguity groups can also be easily determined depending on the pole and zero sensitivities. Unlike the previous methods, which interpret the ambiguity group as the linearly dependent columns of the testability matrix, our method will provide a new interpretation of the ambiguity groups based on circuit theory.

3.5.9. Test and Measurement Selection

Selecting an optimal set of measurements to detect or locate faults is an essential problem; it is related to test point selection and ambiguity sets determination. Measurement selection can be used to (1) reduce the testing time cost, (2) maximize the fault coverage, (3) maximize the fault identification in the fault diagnosis problem.
The analog and mixed-signal circuits have a large number of specifications. Checking all specifications can result in prohibitive testing times. For this reason many approaches are proposed

for selecting the relevant specifications to reduce the cost of the production test without affecting the quality of the test in terms of fault coverage.

In [Milo89], the authors propose a methodology for selecting an optimal set of *DC* tests for wafer test to detect catastrophic faults. This algorithm is extended in [Milo90, Milo94, Chao97] for detecting parametric faults and for reducing the production test time. The parametric fault coverage and the average test time for each specification test set are computed. Tests that have very low fault coverage are eliminated from the test set, and the remaining tests are optimally ordered to optimize the testing time.

In [Huss91] an algorithm based on the graph technique is proposed. The test selection problem is transformed into a direct graph problem. Each node in a graph represents a test set, and each branch represents the test cost. Dijkstra's algorithm is then employed to find the shortest path that represents the best choice of a test set in terms of the shortest test time.

Several algorithms based on the sensitivity analysis are proposed for the selection test points [Sten87, Soun90, Dai90, Sten91, Lu93, Spaa95, Spaa96a, Spaa96b, Hami93, Lind95, Lind97, Lind99, Pron00]. In [Sten87, Soud90, Sten91], the analog circuit is represented by linear model $Ax = b$, where A is the sensitivity matrix, x is the deviation of circuit elements, and b is the deviation of the output response. *QR* factorization is used to decompose the sensitivity matrix, then, selecting the test points is equivalent to selecting independent columns of the sensitivity matrix.

A similar algorithm is proposed in [Spaa95, Spaa96a, Dai90] for selecting the test points. The singular value decomposition (*SVD*) is utilized instead of the *QR* decomposition to factorize the sensitivity matrix in [Spaa95, Spaa96a]. The sensitivity matrix in [Dai90] is a function of time instead of frequency.

In [Hami93], the authors propose a measurement selection approach based on differential and incremental sensitivity. The circuit graph is used to represent the relationship between circuit elements and output performances. An optimization algorithm is used to determine which performances should be measured to guarantee maximum fault coverage.

In [Slam94], analog fault observability based on the sensitivity analysis is introduced. The objective of this method is to select the adequate frequencies and test nodes that improve the detectability of the fault. A similar algorithm is proposed in [Mir96a] based on the diagnosibility region.

In [Lind95, Lind99], a novel approach for the measurement selection algorithm called characteristic observation inference is proposed. A new parametric fault model is introduced based

on individual specification. In this approach, a universal set of specifications is given. From this universal set, a minimal number of measurements is selected that represent a set of observations characterizing the state of the circuit under test with respect to parametric faults. For each given circuit specification, a corresponding test inference criterion is computed based on the logistic discrimination analysis. The satisfaction/violation of the circuit specifications can be inferred from the observations of the circuit under test. In [Pron00], the measurement selection approach based on the sensitivity analysis and the Wavelet transform is proposed for testing parametric faults.

In this thesis, an algorithm for measurement selection is proposed. The concept of the element testability will be introduced. This concept is defined as the difficulty in testing the circuit elements with respect to circuit specifications which are related to the poles and zeros of a circuit. The element testability of the circuit elements is computed based on the sensitivities of the poles and the zeros of the circuit. The selected specifications that have to be measures guarantee the high fault coverage and reduce the test time by avoiding redundant measurements to be performed. Also, the selected measurements can be employed to break up the ambiguity groups if the goal of the test is fault diagnosis.

Chapter 4

Testability Analysis for Analog Circuits

4.1. Introduction

The testability analysis concept is related to the concept of the element-value solvability problem, which gives information about the solvability of the analog test problem (cf. Section 3.5.8). The testability information includes the number of testable elements that can be identified, the number of untestable elements that cannot uniquely be identified, the ambiguity groups, and the optimal nodes to be tested. In other words, the testability analysis provides the information which has to be available before the formulation of the network equations for the fault diagnosis problem. Furthermore, the testability information can be used as a guideline for design for testability (DfT), measurement selection, and test signal generation.

As mentioned in Section 3.5.8, the testability of analog circuits can be achieved using numerical methods or symbolic methods. However, both methods suffer from some shortcomings. Numerical methods such as *QR* factorization [Sten89] or *SVD* decomposition [Liu94] suffer from numerical errors. In this case, the rank of the Jacobian matrix is considered an estimate. Furthermore, the computational time is very long because it depends on the complex frequency s or time samples. On the other hand, symbolic methods [Fedi99, Star00, Pang01, Mane03] can be employed only for small circuits. Moreover, the cost of coefficient sensitivities is very high. In this chapter, we will propose a new testability analysis method which can overcome the disadvantages of the previous works.

This chapter presents a novel methodology for the testability analysis for linear time-invariant analog circuits based on the well-known pole and zero analysis and on the pole and zero sensitivity analysis.
This methodology provides information which includes the number of testable and untestable elements, the ambiguity groups, and the optimal nodes to be tested. Such information is essential for designers to make nodes accessible for testing and for test engineers to plan tests and to provide prior information about the uniquely identified elements by these tests.

The pole and zero analysis provides valuable information for the circuit designers in many domains:

1) In the control system analysis, the location of poles determines the stability of a system [Koa95].
2) For amplifier circuits, the location of the poles and zeros of the forward amplifier gives insight into the performance and the stability of the closed-loop feedback amplifier. Moreover, it provides the information for the compensation circuits to keep the stability of the amplifier circuits [Sedr98].
3) In filter design, the poles and zeros determine filter characteristics [Herp86].
4) In symbolic analysis, the poles and zeros are utilized for the simplification of the symbolic transfer function [Anal01, Half03].
5) If the poles and zeros are available, determining the time and frequency responses of the system can be a simple task [Lee92].
6) The pole and zero analysis can be also employed for model order reduction [Pill95].

On the other hand, pole and zero sensitivity analysis is interesting in a wide range of problems, for example:

1) Pole sensitivity provides fundamental information about system stability and design optimization [Koa95].
2) Pole and zero sensitivity enables designers to follow the direction and magnitude changes caused by element changes [Herp86].
3) Pole and zero sensitivity is used to extract a behavioral model for the analog circuits [Mant93, Chr01, Huan03].
4) If the pole and zero sensitivities are provided, transient and AC sensitivities can easily be computed [Lee92].

Parametric faults caused by manufacturing process variations are usually modeled by small deviations of the circuit elements. The detection of parametric faults is regarded as a much more difficult problem than the detection of structural faults i.e. catastrophic faults (cf. Section 3.5). The normalized differential sensitivity given in Eq. (2-5) can simply model parametric faults based on the first-order approximation [Slam92]. Hence, parametric faults, which are modeled using the normalized differential sensitivity, will be employed in our testability analysis methodology.

4.2. Methodology

The general overview of the testability analysis algorithm is depicted in Figure 4-1.

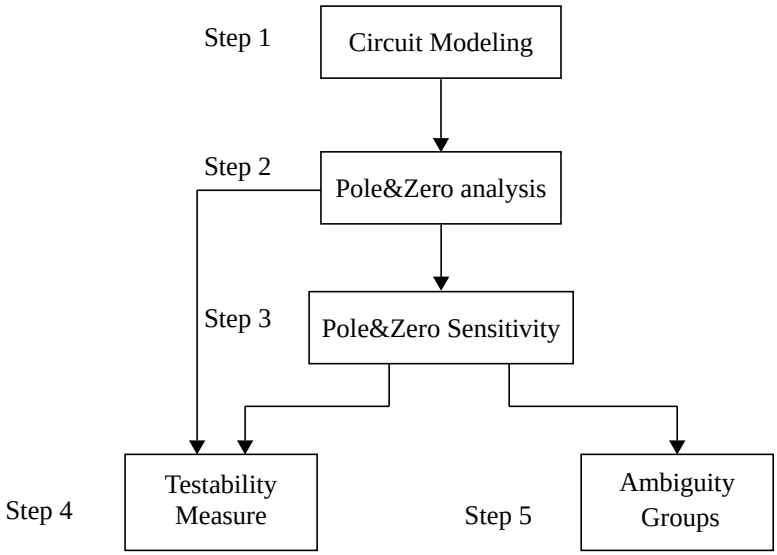


Figure 4-1: Testability Analysis flowchart

In the first step, the linear time invariant (LTI) analog circuit is represented in the Laplace domain by its transfer function which can be obtained by exploiting the modified nodal analysis or by exploiting the state-variable equations. Furthermore, controllability and observability concepts are introduced from the control theory. We will show that both concepts are strictly related to the testability analysis.

In step 3, the locations of the poles and zeros of the transfer function are determined. A pole and zero problem is transformed into an eigenvalue problem which can be solved by utilizing the *QZ* algorithm.

The pole and zero sensitivities with respect to the circuit elements are computed in step 3 by exploiting the adjoint method.
In step 4, the testability measure of the circuit is computed based on the number of poles and zeros in addition to the *DC* gain of the transfer function.
In step 5, the ambiguity groups are determined based on the pole and zero sensitivities.

As a result, the pole and zero sensitivity analysis is employed for the first time to our knowledge in order to compute the testability measure and to determine the ambiguity groups in analog circuits. The testability measure is related to the number of the poles and zeros of a linear circuit in addition to the *DC* gain. A new interpretation of the ambiguity groups is given based on the circuit theory rather than the mathematical interpretation given by linearly dependent columns of the testability matrix. The relationship between the testability measure and the controllability/observability from control theory will also be discussed.

Furthermore, the pole and zero analysis and pole and zero sensitivity analysis can be employed for further test methodologies such as element testability and measurement selection as will be discussed in Chapters 5, 6, and 7.

The details of the above testability analysis algorithm will be discussed in the following sections.

4.2.1. Circuit Modeling

A linear time-invariant system can be described in the Laplace domain using the transfer function which can be obtained using the modified nodal analysis or the state-variable equations. In this section, the generation of the transfer function using the modified nodal analysis and the state-variable equations is presented. Furthermore, the controllability and observability concepts are introduced from the control theory.

4.2.1.1. Modified Nodal Analysis

The modified nodal analysis of the analog circuits is given by Eq. (4-1) (cf. Section 2.4.2)

$$[Y][x] = [b] \tag{4-1}$$

where Y is the system matrix constituted by the modified nodal analysis, x is the solution vector which can be composed of currents and voltages and b is the source vector. The system

matrix Y can be expressed as $Y = G + sC$, where G is the conductance matrix, C is the capacitance matrix, and s is the complex frequency variable.

According to Cramer's rule, the transfer function can be expressed as the ratio of the determinant $\Delta(s)$ and cofactors $\Delta_{ij}(s)$ of the modified nodal matrix Y as given in the Eq. (4-2).

$$H(s) = \frac{\Delta_{ij}(s)}{\Delta(s)} = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_m s^m}{b_0 + b_1 s + b_2 s^2 + \ldots + b_n s^n} = \frac{\sum_{i=0}^{m} a_i s^i}{\sum_{i=0}^{n} b_i s^i} = \frac{N(s)}{D(s)} \qquad m < n \tag{4-2}$$

Many numerical algorithms can be used to generate the transfer function of the system described by Eq. (4-2) directly from the modified nodal matrix such as the interpolation method [Liu91, Vlac94] and matrix-based methods [Hass98]. The interpolation method relies on the Discrete Fourier Transform (DFT) that can generate the transfer function in one symbol namely the complex frequency variable s. The matrix-based methods rely on the modified nodal matrix and Cramer's rule to generate the full symbolic transfer function directly from the circuit description. In this thesis, the matrix-based methods (modified nodal analysis) are utilized to generate the transfer function using the AnalogInsydes software [Anal01] based on the Mathematica environment [Wolf99].

4.2.1.2. State-Variable Equations

A linear invariant-time system with r input sources and m outputs can be described by a coupled set of n first order linear differential equations. These equations are called state-variable equations and are given by Eq. (4-3).

$$\begin{aligned} x'(t) &= A \cdot x(t) + B \cdot u(t) \\ y(t) &= C \cdot x(t) + D \cdot u(t) \end{aligned} \tag{4-3}$$

where, $x(t)$ is the n x 1 state vector, $x'(t)$ is the derivative of the state vector with respect to the time, $u(t)$ is the r x 1 input vector, $y(t)$ is the m x 1 output vector, and matrices A, B, C, D, which are determined by the given network, are n x n, n x r, m x n, and m x r, respectively. The state vector $x(t_o)$ at time t_o consisting of linearly independent state variables is defined as the minimal amount of information at time instant t_o. If the state vector $x(t_o)$ is known, the state vector $x(t)$ at every future time instant $t > t_o$ is uniquely determined by the Eq. (4-3) which describes the linear system.

The Laplace transform of the state-variable equations can be described in vector form as follows:

$$\begin{aligned} sX(s) - x(0) &= AX(s) + BU(s) \\ Y(s) &= CX(s) + DU(s) \end{aligned} \tag{4-4}$$

where *x(0)* is the initial conditions of the state-variable vector at time *0*. By solving Eq. (4-4) yields

$$\begin{aligned} X(s) &= \underbrace{(sI - A)^{-1}BU(s)}_{\text{zero-state response}} + \underbrace{(sI - A)^{-1}x(0)}_{\text{zero-input response}} \\ Y(s) &= \underbrace{[C(sI - A)^{-1}B + D]U(s)}_{\text{zero-state response}} + \underbrace{C(sI - A)^{-1}x(0)}_{\text{zero-input response}} \end{aligned} \tag{4-5}$$

where *I* is the identity matrix. The output response *Y(s)* is divided into two responses, the zero-state response the and zero-input response. The output response *Y(s)* is equal to the zero-state response by setting the initial conditions to zero and equal to the zero-input response by setting the input *U(s)* to zero. The transfer function of the system is equal to *H(s) = Y(s) / U(s)* with *x(0) = 0*, and is given (considering only the single input and single output, SISO system)

$$H(s) = C(sI - A)^{-1}B + D = \frac{C\,adj[sI - A]B + D\,det(sI - A)}{det(sI - A)} = \frac{N(s)}{D(s)} \tag{4-6}$$

where *adj* denotes to the adjoint of the matrix *(sI - A)* and *det* denotes to the determinant of the matrix *(sI - A)*. The state-variable equations can be set up using the circuit topology (the Pottle-Dervisoglu algorithm) [Schw89]. Then the Souriau-Fram algorithm can be used to set up the transfer function *H(s)* from the state-variable equations [Liu91].

Equation *D(s) = 0* from Eq. (4-2) or equation *det(sI-A) = 0* from Eq. (4-6) is called the *characteristic equation*. The roots of the *D(s) = 0* (identical to determinant of the modified nodal matrix *det(Y) = 0*) are called the poles of the circuit, at which the transfer function is equal to infinity. The roots of *det(sI - A) = 0* are called the eigenvalues of the state matrix *A* which are the same as the poles of the transfer function. The poles of a circuit are independent of the input signal or where the signal is applied, therefore, they are called natural frequencies of the circuit [Vlac03]. The order of the network is equal to the number of the poles or the number of the eigenvalues of the system (eigenvalues of the state matrix *A*).

The network is said to be completely controllable at time instant $t = t_0$ if there exists an input *u(t)* that can bring the state variables from the initial conditions $x(t_o)$ to any final state *x(t)*. Thus, the controllability depends on the matrices *A* and *B*. When a natural frequency of the network cannot be excited from an input, it is said to be non-controllable at this input. Non-controllable natural frequencies may cause a state variable to be unstable, independent of the input excitation [Schw89].

Theorem 1: If a network of order *n* has *r* inputs, a necessary and sufficient condition for all natural frequencies to be controllable from all *r* inputs is that the controllability matrix has a rank of *n* [Schw89].

$$Q = \left[A \;\; AB \;\; A^2 B \;\; \ldots \;\; A^{n-1} B\right] \tag{4-7}$$

A network is said to be completely observable if every state variable of the system affects some of the outputs. Thus, the observability concept is related to the state variable of the system output, in other word the observability is related to the matrices *A* and *C*. If the state variables cannot be observed by measurement of the system outputs, the state variable is said to be non-observable.

Theorem 2: If a network of order *n* has *m* outputs, a necessary and sufficient condition for all natural frequencies to be observable at the *m* outputs is that the observability matrix has a rank of *n* [Schw89].

$$P = \left[C^T \;\; A^T C^T \;\; [A^2]^T C^T \;\; \ldots \;\; [A^T]^{n-1} C^T\right] \tag{4-8}$$

where *T* denotes to the transpose of the matrix.

4.2.2. Pole-Zero Analysis

It is often convenient to factorize the numerator and denominator polynomials of the transfer function (the Eq. (4-2)) and to write the transfer function in terms of those factors:

$$H(s) = \frac{N(s)}{D(s)} = K_m \frac{(s-z_1)(s-z_2)\ldots(s-z_m)}{(s-p_1)(s-p_2)\ldots(s-p_n)} = K_m \frac{\prod_{i=1}^{m}(s-z_i)}{\prod_{i=1}^{n}(s-p_i)} \tag{4-9}$$

or

$$H(s) = \frac{N(s)}{D(s)} = \frac{k_1}{(s-p_1)} + \frac{k_2}{(s-p_2)} + \ldots + \frac{k_n}{(s-p_n)} = \sum_{i=1}^{n} \frac{k_i}{(s-p_i)} \tag{4-10}$$

or

$$H(s) = \frac{N(s)}{D(s)} = K_0 \frac{\left(1-\frac{s}{z_1}\right)\left(1-\frac{s}{z_2}\right)\cdots\left(1-\frac{s}{z_m}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\cdots\left(1-\frac{s}{p_n}\right)} = K_0 \frac{\prod_{i=1}^{m}\left(1-\frac{s}{z_i}\right)}{\prod_{i=1}^{n}\left(1-\frac{s}{p_i}\right)} \qquad (4\text{-}11)$$

where $K_m = a_m / b_n$, $K_0 = a_0 / b_0$ (K_0 is the *DC* gain), k_i is the residue that corresponds to the pole p_i, and s is the complex frequency $s = \sigma + j\omega$. The roots z_i of the numerator polynomial *N(s) (N(s) = 0)* are called zeros of the transfer function and the roots of the denominator polynomial *D(s) (D(s) = 0)* are called poles of the transfer function; *m* and *n* are the number of the zeros and poles, respectively. The coefficients of the numerator and denominator polynomials are real, therefore the poles and zeros must be either real or appear in complex conjugate pairs. The poles of the network depend only on the network structure and are independent of the input excitation. In contrast, the zeros of the network depend on the place to which the source is applied and also depend on the point where the output is measured.

The poles and the zeros of a linear circuit together with the real constant K_m or K_0 completely determine the transfer function as a function of the complex frequency *s*. The transfer function is normally represented by the pole and zero diagram on the complex *s*-plane, whose axes represent the real and imaginary parts of the complex variable *s* as shown in Figure 4-2.

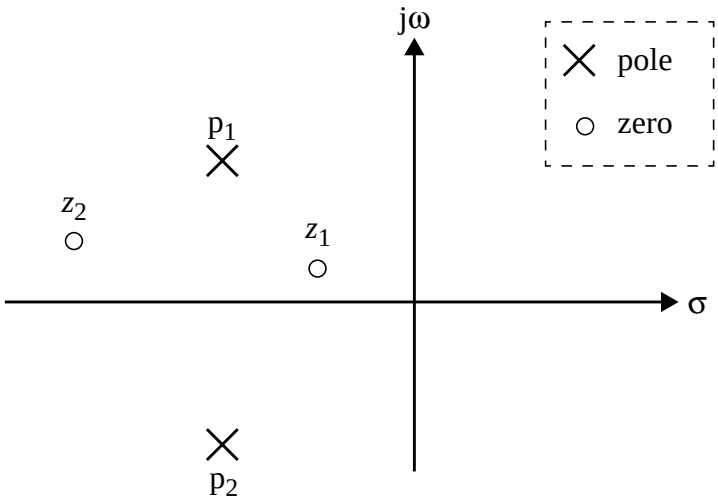


Figure 4-2: Pole and zero representation in *s*-plane

The poles and zeros of the transfer function can effectively define the system response. Particularly, the poles of the transfer function directly define the components of the homogenous

response. This response is called the natural response that depends only on the system structure.

$$y(t) = \sum_{i=1}^{n} C_i e^{\lambda_i t} = \sum_{i=1}^{n} C_i e^{p_i t} \tag{4-12}$$

where the constants C_i are determined from the given initial conditions, and the exponents λ_i are the roots of the characteristic equation (e.g. the poles of the transfer function or the eigenvalues of the state matrix A). The locations of the poles in the complex s-plane determine the stability of the system. If the poles are located in the left-half plan, this means that the components of the system response are decayed, hence the system is stable. On the other hand, if the poles are located in the right-half plane that corresponds to an exponentially increasing components Ce^{pt}, the system is defined as unstable.

The complete system response is divided into two responses, the natural and the forced response. The natural response results from the initial conditions of the storage elements e.g. capacitors or inductors. The forced response results from the input excitations. The complete system response can be directly obtained from Eq. (4-10) using the inverse Laplace transform.

Also, the response of the system in the frequency domain can be obtained using the poles and zeros of the transfer function by substituting $j\omega$ for s directly into the factorized form of the transfer function.

$$H(j\omega) = \frac{(j\omega - z_1)(j\omega - z_2)\ldots(j\omega - z_m)}{(j\omega - p_1)(j\omega - p_2)\ldots(j\omega - p_n)} \tag{4-13}$$

The magnitude and phase angle of the complete response can be written in terms of the magnitudes and angles of the poles and zeros

$$\begin{aligned} |H(j\omega)| &= K\frac{\prod_{i=1}^{m} |(j\omega - z_i)|}{\prod_{i=1}^{n} |j\omega - p_i|} \\ \angle H(j\omega) &= \sum_{i=1}^{m} \angle(j\omega - z_i) - \sum_{i=1}^{n} \angle(j\omega - p_i) \end{aligned} \tag{4-14}$$

As a result, if the poles and zeros can be determined, the time response (Eq. (4-12) and the frequency response (Eq. (4-14) of the system can easily be obtained.

The poles and zeros of the system can usually be computed by two methods. The first method calculates the poles and zeros from the transfer function which are expressed in the numerator and the denominator form. Thus, calculating the poles and zeros is transformed into finding the roots of the polynomial. The Newton-Raphson algorithm is an algorithm which can be used to calculate the roots of the polynomial [Vlac94]. In the second method, calculating the poles and zeros is transformed into the generalized eigenvalue problem. Thus, the poles and zeros can be calculated directly from the system matrix. Many iterative methods are used to calculate the eigenvalues of the system matrix such as the QR algorithm and the QZ algorithm [Golu96]. Since the QZ algorithm is used in this thesis to estimate the poles and zeros of the system, it is useful for explain how the QZ algorithm is used for computing the poles and zeros of the transfer function (based on [Vlac94]).

The generalized eigenvalue problem has the following form [Anal01]:

$$(A - \lambda B)z = 0 \qquad z^T(A - \lambda B) = 0 \tag{4-15}$$

where A and B are real valued matrices, λ is the eigenvalue vector of the matrix pencil *(A,B)*, and z and z^T are the right and left eigenvectors corresponding to λ (z^T denotes to the Hermitian conjugate of z).

The system matrix constructed by modified nodal analysis can be written as $Y = G + sC$, where G and C are real matrices and s is the complex frequency variable, thus the generalized eigenvalue problem can be expressed in following form:

$$det[sC + G] = \prod_i (\alpha_i + \beta_i s) \tag{4-16}$$

where α_i are complex and β_i are real. Either α_i or β_i may be zero. The matrices C and G need not have any special form and may be singular. The natural frequencies f_i are the ratios:

$$f_i = \frac{\alpha_i}{\beta_i} \tag{4-17}$$

If β_i becomes too small (based on a tolerance) this is detected and the natural frequency is defined to exist to infinity and not calculated [Mant90]. The denominator of the transfer function is now known. Next, the numerator is obtained by determining another matrix closely related to the modified nodal matrix *Y*. Rewrite the system equations and equation for the output as:

$$Yx = b \qquad F - d^t x = 0 \tag{4-18}$$

where F is the network function taken as a linear combination of the solution vector x. Eq. (4-18) can be written as a single matrix equation:

$$\begin{bmatrix} Y & 0 \\ -d^t & 1 \end{bmatrix} \begin{bmatrix} x \\ F \end{bmatrix} = \begin{bmatrix} b \\ 0 \end{bmatrix} \tag{4-19}$$

The output of interest F can result from Cramer's rule:

$$F = \frac{det \begin{bmatrix} Y & b \\ -d^t & 0 \end{bmatrix}}{det \begin{bmatrix} Y & 0 \\ -d^t & 1 \end{bmatrix}} = \frac{detY_a}{detY} \tag{4-20}$$

The desired numerator is the determinant of the matrix Y_a and the zeros of the numerator can be obtained by the QZ algorithm.

$$Y_a = \begin{bmatrix} Y & b \\ -d^t & 0 \end{bmatrix} = s \begin{bmatrix} C & 0 \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} G & b \\ -d^t & 0 \end{bmatrix} = sC_a + G_a \tag{4-21}$$

Consequently, the poles and zeros of the transfer function can be estimated by invoking the QZ algorithm twice, once for the poles with C and G, and once for the zeros with C_a and G_a.

4.2.3. Pole-Zero Sensitivity

The general sensitivity formula of the eigenvalue with respect to the parameter h is given [Hale88]:

$$\frac{\partial \lambda_k}{\partial h} = -\left. \frac{z^T \frac{\partial H}{\partial h} z}{z^T \frac{\partial H}{\partial \lambda} z} \right|_{\lambda = \lambda_k} \tag{4-22}$$

where H is the system matrix, λ_k is the eigenvalue of the matrix H, z and z^T are the right and left eigenvectors corresponding to λ. If the matrix H can be expressed in terms of the state variable matrix A ($H = A - sI$ where $s = \lambda$), the Eq. (4-22) can be reduced to the well-known perturbation formula [Gol96]

$$\frac{\partial \lambda_k}{\partial h} = -\left. \frac{z^T \frac{\partial A}{\partial h} z}{z^T z} \right|_{\lambda = \lambda_k} \tag{4-23}$$

The pole and zero sensitivity can be computed relying on the adjoint method [Vlac94], and the resulted formula is the same as the Eq. (4-22). The network function ϕ related to the complex frequency s and parameter h is equal to zero at the network zeros z_i:

$$\phi(s, h)\big|_{s = z_i} = 0 \tag{4-24}$$

The parameter h is considered as the independent variable and z_i as the dependent variable. By differentiating Eq. (4-24) based on the chain rule yields

$$\frac{\partial h}{\partial \phi} + \frac{\partial \phi}{\partial s}\frac{\partial s}{\partial h}\bigg|_{s = z_i} = 0 \tag{4-25}$$

and zero sensitivity is given

$$\frac{\partial z}{\partial h} = \frac{\partial s}{\partial h}\bigg|_{s = z_i} = -\frac{\dfrac{\partial \phi}{\partial h}}{\dfrac{\partial \phi}{\partial s}}\bigg|_{s = z_i} = -\frac{\dfrac{\partial \phi}{\partial h}}{(X^a)^t C X}\bigg|_{s = z_i} \tag{4-26}$$

where X and $(X^a)^t$ are the solution of the direct and adjoint system which are computed by replacing the s by z_i, C is the capacitance matrix. It is clear that Eq. (4-26) is identical to Eq. (4-22) with $H = Y = G + sC$, and the derivative of the function ϕ with respect the element h is computed by the adjoint methods and is given (cf. Appendix *A*)

$$\frac{\partial \phi}{\partial h} = (X^a)^t \frac{\partial Y}{\partial h} X - (X^a)^t \frac{\partial b}{\partial h} \tag{4-27}$$

The pole sensitivity cannot be computed as the zero sensitivity, since the system matrix Y becomes singular at the pole p_i. Thus, the solution X^a and X of the adjoint and direct system cannot be obtained. Therefore, the system matrix Y is decomposed into lower and upper triangular matrices $Y = LU$. The differentiate with respect to the parameter h yields

$$\frac{\partial Y}{\partial h} = \frac{\partial L}{\partial h} U + L \frac{\partial U}{\partial h} \tag{4-28}$$

By pre- and postmultiply Eq. (4-28) by two (so far unknown) vectors $(X^a)^t$ and X respectively, to get the scalar equation:

$$(X^a)^t \frac{\partial Y}{\partial h} X = (X^a)^t \frac{\partial L}{\partial h} U X + (X^a)^t L \frac{\partial U}{\partial h} X \tag{4-29}$$

The vectors are now defined as the solutions of

$$UX = e_n \tag{4-30a}$$

$$L^t X^a = l_{nn} e_n \tag{4-30b}$$

where e_n is the *nth* unit vector and l_{nn} is the *(n, n)* entry of the matrix L. As Y is singular, $l_{nn} = 0$ (partial or full pivoting may be required to ensure the $l_{nn} = 0$) and the right-hand side of the Eq. (4-30b) is, in fact, a zero vector. Thus, $X^a{}_n$ can be arbitrarily chosen (normally, $X^a{}_n = 1$). Substituting Eq. (4-30) into Eq. (4-29) yields

$$(X^{a\,t}) \frac{\partial Y}{\partial h} X = (X^{a\,t}) \frac{\partial L}{\partial h} e_n + l_{nn} e_n^t \frac{\partial U}{\partial h} X \tag{4-31}$$

Since L is a lower triangular matrix, the product $((\delta L / \delta h) e_n)$ is reduced to a vector in which all entire are zero except the last one which is $\delta l_{nn}/\delta h$, that is, $(\delta L/\delta h) e_n = (\delta l_{nn}/\delta h) e_n$. This vector is per multiplied by $(X^a)^t$ and only its last entry, $x^a{}_n = 1$, appears in the product. Moreover, en $\delta U/\delta h$ will be a zero vector, as U is the upper triangular with $u_{nn} = 1$. These steps reduce Eq. (4-31) to

$$(X^{a\,t}) \frac{\partial Y}{\partial h} X = \frac{\partial l_{nn}}{\partial h} \tag{4-32}$$

which is the basic equation for computing pole sensitivity. At this point it is noted that at a pole the relation $l_{nn}(s,h) = 0$ can be used in place of the $\phi(s,h) = 0$, the relation required for the zero sensitivity. Applying Eq. (4-32) in the zero sensitivity (Eq. (4-26), the pole sensitivity for p_i becomes

$$\frac{\partial p_i}{\partial h} = -\left. \frac{\dfrac{\partial l_{nn}}{\partial h}}{\dfrac{\partial l_{nn}}{\partial s}} \right|_{s = p_i} = -\frac{(X^{a\,t}) \dfrac{\partial Y}{\partial h} X}{(X^{a\,t}) CX} \tag{4-33}$$

where $i = 1,..., n$.

Like the zero sensitivity formula, the pole sensitivity formula (Eq. (4-33)) is the same as the Eq. (4-22).

Partial or full pivoting may be required for the term l_{nn} to become zero. In such cases, the LU decomposition is modified to $\Pi_1 T \Pi_2 = LU$ and Eq. (4-32) becomes

$$(X^{a\,t}) \Pi_1 \frac{\partial Y}{\partial h} \Pi_2 X = \frac{\partial l_{nn}}{\partial h} \tag{4-34}$$

where Π_1 and Π_2 are permutation matrices. Eq. (4-33) is also modified in a similar way.

Normally, the pole and zero sensitivity is expressed in normalized form

$$S_h^z = \frac{h}{z}\frac{\partial z}{\partial h} \qquad S_h^p = \frac{h}{z}\frac{\partial p}{\partial h} \tag{4-35}$$

If the pole is given by the real and the imaginary parts $p = \sigma + j\omega$, the normalized sensitivity becomes (the same formula is valid for a zero sensitivity)

$$S_h^p = \frac{h}{\sigma}\frac{\partial \sigma}{\partial h} + j \cdot \frac{h}{w}\frac{\partial \omega}{\partial h} = S_h^\sigma + j \cdot S_h^\omega \tag{4-36}$$

Based on the pole and zero sensitivity, the *Q*-factor and pole frequency sensitivities can be also computed [Vlac94] as we will see in the next chapter.

4.2.4. Testability Measure

A testability measure provides quantitative information about the degree of solvability of the circuit under test starting from the circuit topology and given test points (cf. Section 3.5.9). The analog circuits are considered a low testability if all circuit elements cannot be identified. In this case, the testability measure shows how many faulty elements can be identified and how many elements must be assumed to be nominal with a given test point set.

The transfer function of the circuit under test obtained in factorized form can be written

$$H(s) = K_0(h_i)\frac{\left(1-\frac{s}{z_1(h_i)}\right)\left(1-\frac{s}{z_2(h_i)}\right)\ldots\left(1-\frac{s}{z_m(h_i)}\right)}{\left(1-\frac{s}{p_1(h_i)}\right)\left(1-\frac{s}{p_2(h_i)}\right)\ldots\left(1-\frac{s}{p_n(h_i)}\right)} = K_0(h)\frac{\prod_{l=1}^{m}\left(1-\frac{s}{z_l(h_i)}\right)}{\prod_{j=1}^{n}\left(1-\frac{s}{j(h_i)}\right)} \tag{4-37}$$

where the *DC* gain K_0, poles p_j and zeros z_l of the transfer function are a function of the circuit elements h_i (where $i = 1,2,\ldots, k$; k is the number of circuit elements). We assume the poles and zeros of the transfer function are distinct (they are all different), but the general case is discussed in Section 4.4.

The testability measure based on Eq. (4-37) is separated into three parts. The first part depends only on the poles of the transfer function. In other words, the first part of testability measure depends only on the circuit topology and is independent of the input signals and circuits nodes. We will refer to the first part of the testability measure as T_p (where T denotes to the testability and p denotes to the poles of the circuit). The testability T_p is given by Eq. (4-38)

$$T_p = n \tag{4-38}$$

where n is the number of the poles of the transfer function given by Eq. (4-34).

As a result, since this part depends only on the circuit structure, the number of the poles of the transfer function is the same as the order of the circuits given by Eq. (4-39).

$$n = n_{LC} - n_L - n_C \tag{4-39}$$

where n is the circuit order (or circuit complexity), n_{LC}, is the total number of energy storage elements, n_C, is the total number of independent capacitive loops, and n_L, is the total number of independent inductive cutsets (cf. Section 2.4.1).

The second part of the testability measure relies on the zeros of the transfer function. We refer to the second part of the testability measure as T_z (where T denotes to the testability and z denotes to the zeros of the transfer function) and is given by the following equation

$$T_z = m \tag{4-40}$$

where m is the number of the zeros.

The third part of the testability measure depends on the *DC* gain $K_0 = a_0 / b_0$ (s --> 0) and is referred to as T_{K0}.

$$T_{K_0} = c \tag{4-41}$$

where $c = 1$ if the *DC* gain is a function of the circuit elements, otherwise c = 0. The value of c can be computed using *DC* sensitivity. If *DC* sensitivity at a certain circuit node is different from 0, this leads to $c = 1$, otherwise $c = 0$.

The total testability measure T_t of the circuit under test is equal to the sum of the three parts of the testability measure at a circuit node

$$T_t = T_p + T_z + T_{K_0} = n + m + c \tag{4-42}$$

Consequently, the testability measure of the circuit under test at a certain node depends on the number of the poles, the number of the zeros, and *DC* gain K_0 at that node. This result can simply be deduced by relying on Eq. (4-37). The following equations can be constructed based on Eq. (4-37): $p_j = f(h_i)$ (where $j = 1,2,..., n$ and $i = 1, 2,..., k$), $z_l = f(h_i)$ (where $l = 1, 2,..., m$ and $i = 1, 2,..., k$), and $K_0 = f(h_i)$. Thus, the testability measure is the same as the number of the pole, zero and *DC* gain equations which are a function of the circuit elements.

Eq. (4-42) can be expressed based on the circuit matrix Y using the Eq. (4-19):

$$T_t = rank(Y_a) + rank(Y) + c \tag{4-43}$$

where $Y_a = \begin{bmatrix} Y & b \\ -d^t & 0 \end{bmatrix}$ and $Y = \begin{bmatrix} Y & 0 \\ -d^t & 1 \end{bmatrix}$

The rank of the matrices Y_a and Y represent the number of the zeros and poles, respectively. Thus, the testability measure can be obtained directly from the circuit matrix.

If more than one test node is considered, the testability measure is given

$$T_t = n + m_1 + c_1 + m_2 + c_2 + \ldots + m_l + c_l \tag{4-44}$$

where n in the number of the poles and m_1, m_2,..., m_l are the number of the zeros at nodes *1*, *2*,..., l respectively, the c_1, c_2,..., c_l are the *DC* gain at nodes *1*, *2*,..., l respectively, and l is the number of circuit nodes. For example, if two nodes in the circuit are considered to be accessible, the testability measure is given $T_t = n + m_1 + m_2 + c_1 + c_2$, where n is the poles and m_1, m_2 are the number of the zeros at node *1* and node *2*, respectively, and the c_1, c_2 are the *DC* gain at nodes *1*, and *2*,respectively.

If the circuit has e elements and the testability measure at node i is $T_t = r$ (where $r < e$), thus only r elements can be identified and $(e - r)$ elements must be assumed as not faulty (low-testability circuits [Pang01]). Consequently, the testability can be used as a guide for test node selection. It is worthwhile to note that the minimum number of the testable elements is the same as the number of the poles of the transfer function.

If the number of the circuit elements are equal to the number of the poles and the number of the zeros at circuit node plus 1, the maximum testability is obtained (all circuit elements can be identified).

If the transfer function has poles and zeros in the same position, (the poles and zeros result from the same circuit elements), these zeros cause the pole cancellation case. In this case, the natural frequency of the system will be different from the system poles. The testability measure in pole-zero cancellation case is given

$$T_t = n + m_1 + c_1 + m_2 + c_2 + \ldots + m_l + c_l - n_{pz} \tag{4-45}$$

where n_{pz} is the number of the cancelled poles and zeros.

In order to illustrate the testability measure based on the pole and zero analysis, we will give the *3-RC* ladder circuit as an example, as shown in Figure 4-3

.

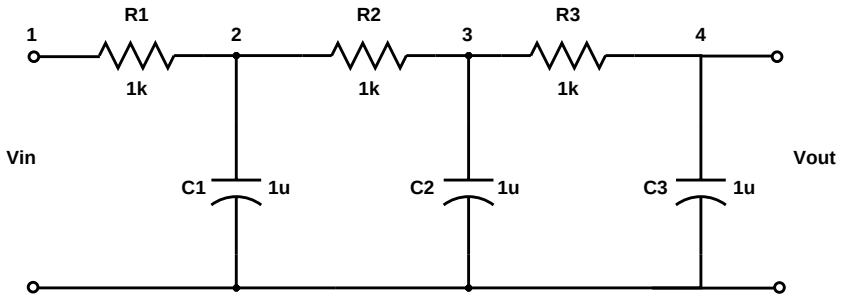


Figure 4-3: The 3-RC ladder circuit

Based on the modified nodal analysis the system equations of the circuit can be written as

$$\begin{bmatrix} \frac{1}{R_1} & -\frac{1}{R_1} & 0 & 0 & 1 \\ -\frac{1}{R_1} & \frac{1}{R_1}+\frac{1}{R_2}+sC_1 & -\frac{1}{R_2} & 0 & 0 \\ 0 & -\frac{1}{R_2} & \frac{1}{R_2}+\frac{1}{R_3}+sC_2 & -\frac{1}{R_3} & 0 \\ 0 & 0 & -\frac{1}{R_3} & \frac{1}{R_3}+sC_3 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_{Vin} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_{in} \end{bmatrix}$$

The transfer functions at node *4*, node *3* and node *2* of the circuit are given ($V_1 = V_{in}$ and $V_4 = V_{out}$)

$$H_4(s) = \frac{V_{out}}{V_{in}} = \frac{10^9}{10^9 + 6\times10^6 s + 5000s^2 + s^3}$$

$$H_3(s) = \frac{V_3}{V_{in}} = \frac{10^6(10^3 + s)}{10^9 + 6\times10^6 s + 5000s^2 + s^3}$$

$$H_2(s) = \frac{V_2}{V_{in}} = \frac{10^3(10^6 + 3000s + s^2)}{10^9 + 6\times10^6 s + 5000s^2 + s^3}$$

The poles and zeros of the transfer functions computed by the *QZ* algorithm and the testability measure are given in Table 1.

In 3-RC ladder circuit, the *DC* gain K_0 is independent of the circuit elements ($K_0 = 1$ at any node), thus $c = 0$.

All circuit elements can be identified using nodes (3, 2) or (4, 3, 2), otherwise the circuit is in low testability case (i.e. the testability measure is less than the number of the circuit elements).

Table 1: Pole and zero analysis of the 3-RC ladder circuit and the testability measure

<table>
<tr><td>Poles</td><td>Zeros at node 4</td><td>Zeros at node 3</td><td>Zeros at node 2</td></tr>
<tr><td>-198.062</td><td rowspan="3">No zeros</td><td rowspan="3">-1000</td><td>-381.966</td></tr>
<tr><td>-1554.96</td><td rowspan="2">-2618</td></tr>
<tr><td>-3246.98</td></tr>
<tr><td>$T_p = 3$</td><td>$T_{zm1} = 0$</td><td>$T_{zm2} = 1$</td><td>$T_{zm3} = 2$</td></tr>
<tr><td rowspan="3">Testability measure</td><td>T_t at node 4 = 3</td><td>T_t at node 3 = 4</td><td>T_t at node 2 = 5</td></tr>
<tr><td colspan="3">T_t at node 4 and 3 = 4 and T_t at node 3 and 2 = 6</td></tr>
<tr><td colspan="3">T_t at node 4 and 2 = 5 and T_t at node 4, 3, and 2 = 6</td></tr>
</table>

This result obtained by our algorithm are identical to the results that were obtained by the rank of the testability matrix (linearly independent columns) constructed either by the sensitivity matrix (the matrix entries are a function of the frequency) [Sen79, Dai90, Liu94, Beck94, Pang01] or by the coefficient sensitivity matrix (the matrix entries are independent of the frequency) [Mane98, Fedi99, Liu96, Pi02, Mane03].

4.2.5. Ambiguity Group Analysis

Generally, the value of the testability measure of an analog circuit is less than the number of its elements. This leads to a low testability of the circuit under test, therefore, the ambiguity group concept will now be introduced.

An ambiguity group is a set of elements where the faulty elements cannot uniquely be identified from each others. In other words, the faults in the ambiguity group elements produce the same value of measurements, taking into consideration element tolerances and measurement errors. Mathematically, the ambiguity group is defined as the dependent columns of the testability matrix which correspond to the circuit elements.

In this section, we will introduce a new algorithm for the determination of the ambiguity groups based on pole and zero sensitivity. Moreover, the algorithm provides a new interpretation of the ambiguity groups based on the circuit theory, unlike the other algorithms which only give a mathematical interpretation according to the linearly dependent columns of the testability matrix.

The poles and zeros of the transfer function determine the characteristic of the frequency and time response. Therefore, the deviation of the pole and zero locations under a fault from the original positions will affect the circuit specifications either in time or in frequency domains. The ambiguity group can be divided into two classes, pole ambiguity group and zero ambiguity group. The pole ambiguity groups, like testability measure T_p, depend on the poles of the transfer function. The pole ambiguity groups are determined as follows:

If the pole sensitivity with respect to the elements h_1, h_2,..., h_i ($i <= k$ number of the circuit elements) is the same, this leads the elements h_1, h_2,..., h_i belong to the same pole ambiguity group.

In other words, if two poles have the same sensitivity with respect to the elements h_1 and h_2 (the same deviation caused by the elements h_1 and h_2), their effects on the time or frequency responses are also the same. Therefore, the measurements cannot distinguish faulty element h_1 from faulty element h_2.

From the 3-RC ladder circuit, the pole sensitivities are given in Table 2.

Table 2: Pole Sensitivity with respect to the circuit elements

h	S^{p1}_h	S^{p2}_h	S^{p3}_h
R_1	-0.54313	-0.10757	-0.34929
R_2	-0.34929	-0.54313	-0.10757
R_3	-0.10757	-0.34929	-0.54313
C_1	-0.10757	-0.34929	-0.54313
C_2	-0.34929	-0.54313	-0.10757
C_3	-0.54313	-0.10757	-0.34929

Thus, the ambiguity groups are given in Table 3.

Table 3: Ambiguity groups at node 4

Groups	1	2	3
Elements	R_1, C_3	R_2, C_2	R_3, C_1

On the other hand, the zero ambiguity groups are determined as follows:

If two elements have the same zero sensitivities, they belong to the same zero ambiguity groups.

For example the 3-RC ladder circuit, the zero sensitivities at node 3 and node 2 are given in Table 4.

Table 4: Zero sensitivities at node 2 and 3

Elements h	Zero sensitivity at node 3	Zero sensitivity at node 2	
	S^{z}_{h}	S^{z1}_{h}	S^{z2}_{h}
R_1	0	0	0
R_2	0	-0.27639	-0.7236
R_3	-1	-0.7236	-0.27639
C_1	0	0	0
C_2	0	-0.7236	-0.27639
C_3	-1	-0.27639	-0.7236

The total ambiguity groups at a given circuit node is constructed mathematically by intersection of the pole ambiguity groups and the zero ambiguity groups. This means that the zero ambiguity groups obtained by zero sensitivities break up the pole ambiguity groups obtained by pole sensitivities. In this case, the two elements, which have different pole and zero sensitivities, affect the pole and zero location in a different manner, which means that they also affect the circuit response in different manner. For the 3-RC example, the zeros at node 3 breaks up the ambiguity groups $\{R_1, C_3\}$ and $\{R_3, C_3\}$ and the zeros at node 2 lead to break up all ambiguity groups in the 3-RC ladder circuits.

In summary, the total ambiguity group can be determined as follows:

The element h_1 and the element h_2 belong to the same ambiguity group, if the pole and zero sensitivities associated to the element h_1 are the same as the pole and zero sensitivities associated to the element h_2.

As a result, the ambiguity group can be interpreted as a group of circuit elements which affect the poles and zeros of a circuit in the same way.

4.2.6. Testability Analysis and Controllability/Observability

The system is said to be controllable if the rank of the controllability matrix Q is equal to the number of the system state variables (cf. Eq. (4-7)). On the other hand, the system is said to be

observable if the rank of the observability matrix P is equal to the number of the system state variables (cf. Eq. (4-8)).

In electrical circuits, the state of the circuit at t_0 represents the condition of the circuit at $t = t_0$, and related to the energy storage of the circuit, or the voltage (or electric charge) across the capacitor and currents (or magnetic fluxes) through the inductors. For $t > t_0$ the behavior of the circuit is completely characterized by these variables [Chao95a]. The number of the circuit states is the same as the order of the circuit which is also the same as the number of the eigen-values of the state matrix A or the number of the poles of the transfer function.
If the transfer function has no pole-zero cancellation, the rank of the matrix $(sI - A)$ is the same as the order of the circuit n [Koa95]. This leads to that the controllability and observability matrices have the rank equal to n. It is sufficient to check the rank of the matrix $(sI - A)$ to determine whether the system is completely controllable (observable) or not, without the need to the matrix B or C. Since the rank of the matrix $(sI - A)$ is the same as the number of the eigenvalues of the state matrix A or the number of the poles, leading the testability measure T_p to be the same as the rank of the controllability or observability matrices.
In pole-zero cancellation, the testability measure will be decreased by the same number of the cancelled poles and zeros. Also, the testability measure is equal to the minimum value of the rank of the controllability and observability matrices: $T_p = mim(rank(P), rank(Q))$.
The state-variables of a circuit, which are selected as the independent capacitor voltages or independent inductor currents, do not belong to the same ambiguity group.
In the 3-RC ladder circuit, the capacitors C_1, C_2, and C_3, whose voltages represent the state-variables, belong to the different ambiguity groups. Furthermore, the voltages across these capacitors are controllable and observable in terms of the controllable or observable states.

Furthermore, based on the pole and zero sensitivities the nonobservable states of the linear analog circuit can be determined. If the pole sensitivity with respect to the capacitor is equal to the zero sensitivity with respect to the same capacitor, leading the state, which is represented by the voltage of this capacitor, is not observable.

4.3. Simulation Examples

Before introducing the simulation examples, we will summarize the ambiguity group algorithm proposed in [Liu94, Mane03] for comparison purpose. The algorithm steps

I) construct the sensitivity matrix (Jacobian matrix) *B (m x n)* as a function of the frequency [Liu94]. The Jacobian matrix can also be constructed by taking coefficient sensitivities with respect to the circuit elements [Man03].

II) perform the Singular Value Decomposition *(SVD)* of the sensitivity matrix $B = U\ W\ V^T$. The matrices U *(m x m)* and V *(n x n)* are unitary matrices and *W* is a diagonal matrix $W = diag\{\sigma_1, \sigma_2,..., \sigma_p\}$, where $p = min(m, n)$ and σ_i are called singular values of matrix *B*. The singular values appear in this order $\sigma_1 >= \sigma_2 >=..., \sigma_p >= 0$.

III) find the null space *N* of the matrix *B* using unitary matrix *U* or *V* according to *min(n, m)*.

IV) element *i* and *j* are in the same ambiguity group iff rows *i* and *j* of *N* are-non-zero and not orthogonal to each other.

In this section we will present some examples based on the AnalogInsydes software in Mathematica environment. The first and second example are taken from [Liu94] and [Mane03] for comparison purpose. The fourth example is introduced to explain the pole-zero cancellation.
In order to validate our results, we will perform some measurements on some circuit performances (specifications) in the time and frequency domain using the Saber simulator [Anal97].

4.3.1. The 7-RC Ladder Circuit

The 7-RC ladder circuit is shown in Figure 4-4.

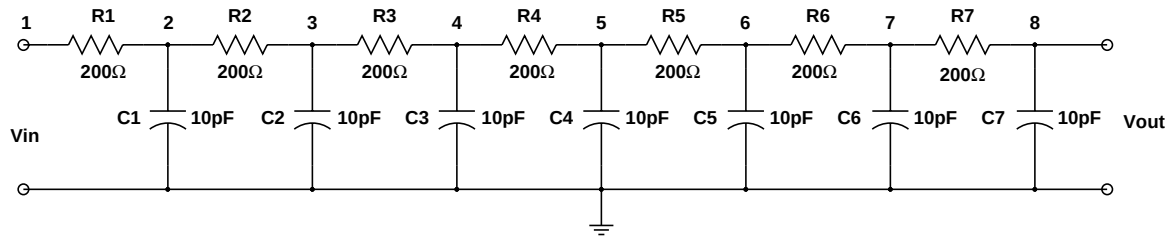


Figure 4-4: The 7-RC ladder Circuit

The poles of the circuit are given in Table 5.

Table 5: The poles of the 7-RC ladder circuit

P1	P2	P3	P4	P5	P6	P7
$-1.913\ 10^9$	$-1.669\ 10^9$	$-1.309\ 10^9$	$-8.954\ 10^8$	$-5\ 10^8$	$-1.909\ 10^8$	$-2.1852\ 10^7$

Since there is no zero at node 8 (the output node), and *DC* gain is independent of the circuit elements ($K_0 = 1$ at all circuit nodes, thus $c = 0$), the testability measure is equal to the number of the poles ($T_t = 7$). This is the same as the rank of the observability matrix *Q*.

In order to determine the ambiguity groups, the pole sensitivities are given in Table 6.

Table 6: Pole sensitivities of the 7-RC ladder circuit

h	S^{p1}_h	S^{p2}_h	S^{p3}_h	S^{p4}_h	S^{p5}_h	S^{p6}_h	S^{p7}_h
R_1	-0.011527	-0.044115	-0.092131	-0.14727	-0.2	-0.241202	-0.263753
R_2	-0.092131	-0.241202	-0.241202	-0.092131	0	-0.092131	-0.241202
R_3	-0.2	-0.2	0	-0.2	-0.2	0	-0.2
R_4	-0.263753	-0.011527	-0.241202	-0.044115	-0.2	-0.092131	-0.14727
R_5	-0.241202	-0.092131	-0.092131	-0.241202	0	-0.241202	-0.092131
R_6	-0.14727	-0.263753	-0.092131	-0.011527	-0.2	-0.241202	-0.044115
R_7	-0.044115	-0.14727	-0.241202	-0.263753	-0.2	-0.092131	-0.011527
C_1	-0.044115	-0.14727	-0.241202	-0.263753	-0.2	-0.092131	-0.011527
C_2	-0.14727	-0.263753	-0.092131	-0.011527	-0.2	-0.241202	-0.044115
C_3	-0.241202	-0.092131	-0.092131	-0.241202	0	-0.241202	-0.092131
C_4	-0.263753	-0.011527	-0.241202	-0.044115	-0.2	-0.092131	-0.14727
C_5	-0.2	-0.2	0	-0.2	-0.2	0	-0.2
C_6	-0.092131	-0.241202	-0.241202	-0.092131	0	-0.092131	-0.241202
C_7	-0.011527	-0.044115	-0.092131	-0.14727	-0.2	-0.241202	-0.263753

The ambiguity groups are given in Table 7.

Table 7: The ambiguity groups at node 8 (the output)

Groups	1	2	3	4	5	6	7
Elements	R_1, C_7	R_2, C_6	R_3, C_5	R_4, C_4	R_5, C_3	R_6, C_2	R_7, C_1

Note that the capacitors do not belong to the same ambiguity groups because their voltages present the state variables of the circuit.

The normalized sensitivity (cf. Section 2.4.3.4, also cf. Appendix A) of low-pass frequency computed using Saber simulator to validate the above results are given in Table 8:

Table 8: The normalized sensitivity of low-pass frequency

Elements	R_1, C_7	R_2, C_6	R_3, C_5	R_4, C_4	R_5, C_3	R_6, C_2	R_7, C_1
Sensitivities	-0.262	-0.236	-0.195	-0.146	-0.0956	-0.0496	-0.0147

This result is identical to the reported one in [Liu94]. Furthermore, we will compute the test-ability measure and determine the ambiguity groups at another node for example at node 4. The testability measure at node 4 is equal to $T_t = 7 + 4 = 11$ (7 poles, 4 zeros, and $c = 0$). The zeros at node 4 are given in Table 9:

Table 9: The zeros of the circuit at node 4

Z_2	Z_3	Z_4	Z_5
$-1.766\ 10^9$	$-1.17365\ 10^9$	$-5\ 10^8$	$-6.03073792\ 10^7$

The zero sensitivities w.r.t. the elements of the 7-RC lader circuit are given in Table 10:

Table 10: Zero sensitivities

h	S^{z1}_h	S^{z2}_h	S^{z3}_h	S^{z4}_h
R_1	0	0	0	0
R_2	0	0	0	0
R_3	0	0	0	0
R_4	-0.0519901	-0.183634	-0.333333	-0.431043
R5	-0.333333	-0.333333	0	-0.333333
R6	-0.431043	-0.0519901	-0.333333	-0.183634
R7	-0.183634	-0.431043	-0.333333	-0.0519901
C1	0	0	0	0
C2	0	0	0	0
C3	0	0	0	0
C4	-0.183634	-0.431043	-0.333333	-0.0519901
C5	-0.431043	-0.0519901	-0.333333	-0.183634

Table 10: Zero sensitivities

C6	-0.333333	-0.333333	0	-0.333333
C_7	-0.0519901	-0.183634	-0.333333	-0.431043

The zero ambiguity groups at node 4 are {R_4, C_7}, {R_5, C_6}, {R_6, C_5}, and {R_7, C_4} and the other elements are definitely testable. Thus, there are no more ambiguity groups because all pole ambiguity groups are broken up by the zero ambiguity groups.

4.3.2. Continuous-Time State-Variable Filter

The continuous-time state-variable circuit shown in Figure 4-5 provides low-pass, high-pass, and band-pass filters [Kami97].

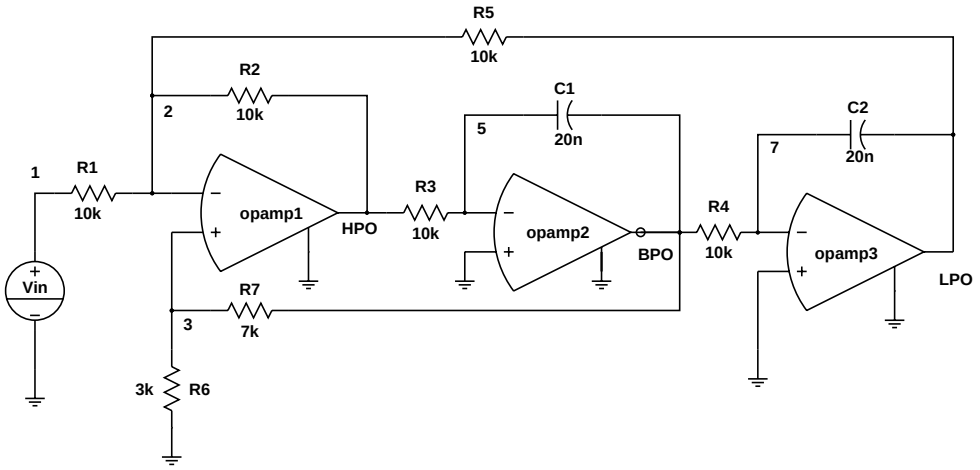


Figure 4-5: The schematic of the continuous-time state-variable circuit

The poles of the state-variable filter are given in Table 11.

Table 11: The Poles of the state-variable filter

P_1	P_2
2250. + 4465.13 i	-2250. - 4465.13 i

The zeros of the state-variable filter at nodes, LPO, BPO, and HPO are given in Table 12.

Table 12: The circuit zeros at node HPO, BPO, and LPO

LPO	no zeros	
BPO	Z_2 = - 1/1000001 C_2 R_4 = -0.005	
HPO	Z_1 = - 1/1000001 C_1R_3 = -0.005	Z_2 = - 1/1000001 C_2 R_4 = -0.005

The *DC* gain is a function of the circuit elements (*c =1*), thus the testability measure is given in Table 13.

Table 13: Testability measure

T_t (LPO)	T_t (BPO)	T_t (HPO)
3	4	5

The pole sensitivities are given in Table 14.

Table 14: Pole Sensitivities

h	S^{p1}_h	S^{p2}_h
R_1	$3.5.\ 10^{-7}$ + 0.167967 i	$3.5.\ 10^{-7}$ - 0.167967 i
R_2	0.5 - 0.083982 i	0.5 + 0.083982 i
R_3	- 0.5 + 0.251951 i	- 0.5 - 0.251951 i
R_4	- 0.5 - 0.251951 i	- 0.5 + 0.251951 i
R_5	- 0.5 - 0.08398 i	- 0.5 + 0.08398 i
R_6	$3.15\ 10^{-7}$ - 0.35273 i	$3.15\ 10^{-7}$ +0.35273 i
R_7	$-\ 3.15\ 10^{-7}$ + 0.35273 i	$-\ 3.15\ 10^{-7}$ - 0.35273 i
C_1	- 0.5+ 0.251951 i	- 0.5 - 0.251951 i
C_2	- 0.5 - 0.251951 i	- 0.5 + 0.251951 i

The ambiguity groups for low-pass filter are given in Table 15.

Table 15: Ambiguity groups at LPO

Groups	1	2	3	4	5	6	7
Elements	R_1	R_2	R_5	R_6	R_7	R_3, C_1	R_4, C_2

Thus, the elements R_1, R_2, R_5, R_6, and R_7 are testable elements while the elements R_3, C_1 belong to the same ambiguity group. Therefore, either R_3 or C_1 must be assumed to be nominal. The elements R_4, C_2 also belong to the same ambiguity group, therefore either R_4 or C_2 must be assumed to be nominal.

The zero sensitivities at node BPO and HPO are given in Table 16.

Table 16: Zero Sensitivities at nodes BPO and HPO

h	S^z_h (BPO)	S^z_h (HPO)	
R_1	0	0	0
R_2	0	0	0
R_3	0	-1	0
R_4	-1	0	-1
R_5	0	0	0
R_6	0	0	0
R_7	0	0	0
C_1	0	-1	0
C_2	-1	0	-1

The zero ambiguity group is the same as the pole ambiguity group, hence the zeros cannot break up the ambiguity groups. The ambiguity groups at the nodes LPO, BPO, and HPO of the filter are the same.

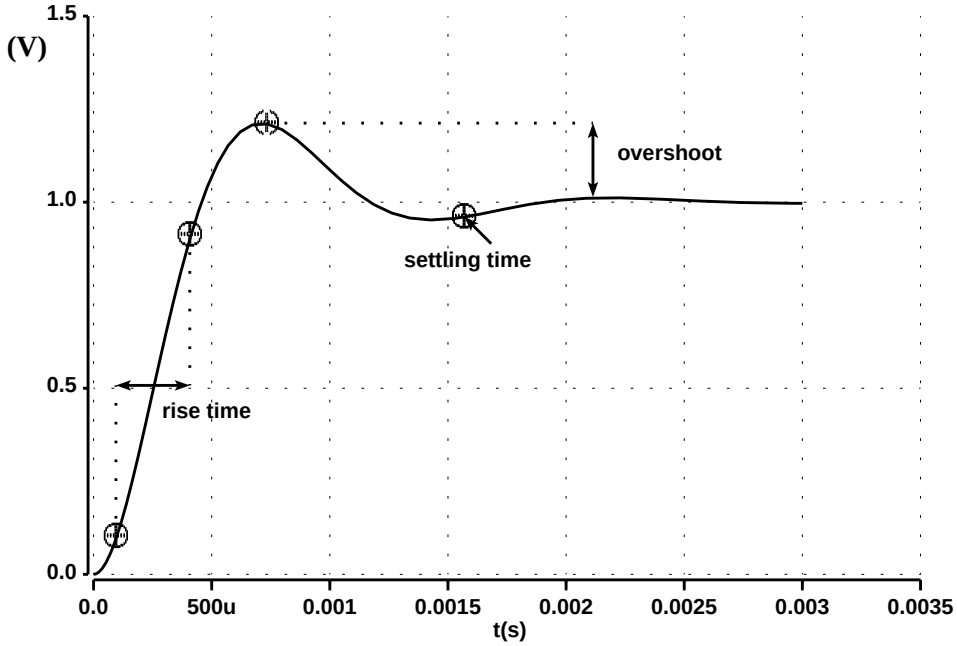


Figure 4-6: Step response of the state-variable filter (V_{in}=*-1 v*)

In order to validate our results, we will take an example of some measurements of the time domain specifications. The time step response of the state-variable filter at the output LPO is produced using Saber simulator as shown in Figure 4-6 (V_{in} = *-1 volt*). We will select three time domain specifications namely rise time, settling time and maximum overshoot. The nominal values of these specifications as well as the faulty specifications caused by +20% deviation of each element in the circuit is given in Table 17 by assuming that a single fault may occur. The measured specifications caused by the deviation of elements R_3 and C_1 or R_4 and C_2 can not be distinguished.

Table 17: Rise time, settling time, and maximum overshoot specifications

h	rise time (μsec)	settling time (sec)	maximum overshoot (v)
nominal	314.64	0.0015689	0.19899
R_1 +20%	300.95	0.0015003	0.19736
R_2 +20%	287.5	0.00097944	0.19754
R_3 +20%	331.91	0.001816	0.23017
R_4 +20%	360.41	0.0011584	0.16855
R_5 +20%	350.08	0.0015816	0.22673
R_6 +20%	334.3	0.0010622	0.15694
R_7 +20%	290.72	0.0015562	0.27061
C_1 +20%	332.12	0.001813	0.23144
C_2 +20%	360.1	0.0011587	0.16861

Low-cutoff frequency, bandwidth, and high-cutoff frequency are selected as examples for frequency domain specifications to be measured. These specifications are given in Table 18.

Table 18: The low-cutoff frequency, bandwidth, and high-cutoff frequency specifications

h	Low-cutoff frequency (Hz)	bandwidth (Hz)	high-cutoff frequency (Hz)
nominal	1057.3	725.07	603.97
R_1 +10%	1064.6	707.7	599.29
R_2 +10%	1100.3	788.87	637.49
R_3 +10%	1024.7	650.61	566.2
R_4 +10%	986.76	714.62	586.83

Table 18: The low-cutoff frequency, bandwidth, and high-cutoff frequency specifications

h	Low-cutoff frequency (Hz)	bandwidth (Hz)	high-cutoff frequency (Hz)
R_5 +10%	997.09	693.34	581.09
R_6 +10%	1031.7	770.91	618.09
R_7 +10%	1079.2	679.78	590.92
C_1 +10%	1024.7	650.51	566.2
C_2 +10%	986.76	714.62	586.83

The ambiguity group algorithm proposed in [Liu94, Mane03] depends on the selected specification. In other words, the ambiguity groups are different from one specification to another i.e. the ambiguity groups in the time domain are different from the ambiguity groups in the frequency domain. Even for the same domain they may be different i.e. in the frequency domain the ambiguity groups related to the amplitude may be different from the ambiguity groups related to the phase. In contrast, our algorithm is independent of specifications because the algorithm is based on the pole and zero sensitivities. As previously mentioned, the poles and zeros can characterize the time and frequency specifications.

The ambiguity groups for the time-continuos state-variable filter in [Mane03] are given in Table 19.

Table 19: The ambiguity groups at node LPO, BPO, and HPO

Group	1	2	3	4
Elements	R_6, R_7	R_1, R_2, R_5	C_2, R_4	C_1, R_3

The fault in element R_1 can be distinguished from the faults in element R_2, R_5 (cf. the measured specifications Table 17 and Table 18). Hence, the element R_1 cannot belong to the ambiguity group of the elements R_2 and R_5. Furthermore, the absolute value of the difference between the nominal and the actual value of the elements R_2 and R_5 is approximately equal (i.e. 1057.3 - 1031.7 = 26.6 and 1057.3 - 1079.2 = - 21.9), hence they belong to the same ambiguity group (the magnitude of the performance is taken into account). The same can be said for elements R_6 and R_7. Thus, only the absolute value of the difference between the nominal and the actual value are taken into account. The direction of the variation is not considered. In our algorithm, this result can easily be obtained by comparing the absolute value of

the pole sensitivities associated to the elements R_6 and R_7 or R_2 and R_5. As a result, the ambiguity groups related to the magnitude or phase of the transfer function can be obtained from the pole sensitivities.

In summary, the ambiguity groups are related to the measurements which in turn rely on the pole and zero location. The relationship between the ambiguity groups (or pole and zero sensitivities) and time and frequency domain specifications will be discussed in more detail in Chapter 5.

4.3.3. Leapfrog Filter

The schematic of the leapfrog is shown in Figure 4-7 [Kami97]

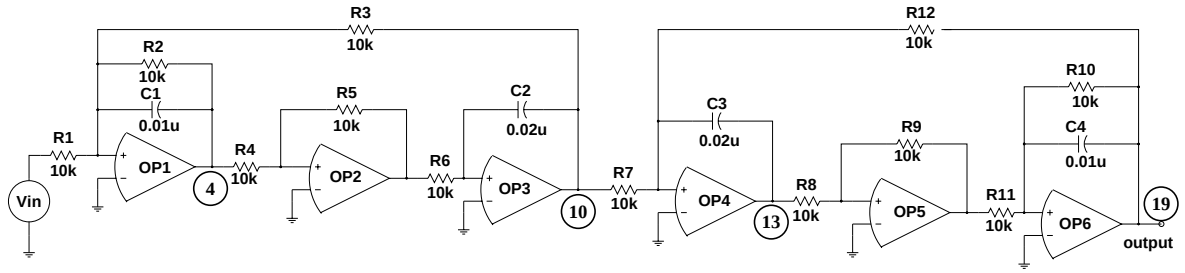


Figure 4-7: The schematic of the leapfrog

The poles of the filter are given in Table 20.

Table 20: The poles of the leapfrog filter

P1	P2	P3	P4
-5000.01 - 4999.97 i	-5000.01 + 4999.97 i	-5000.01 - 4999.98 i	-5000.01 + 4999.98 i

The testability measure at the output is $T_t = 5$ ($c = 1$).

The pole sensitivities are given in Table 21.

Table 21: Pole sensitivities

h	$S^{p_1}_h$	$S^{p_2}_h$	$S^{p_3}_h$	$S^{p_4}_h$
R1	-10^{-6} i	-10^{-6} i	0	0
R2	$-5\ 10^{-7} + i$	$-5\ 10^{-7} - i$	0	0
R3	-0.5 - 0.5 i	-0.5 + 0.5 i	0	0
R4	-0.5 - 0.5 i	-0.5 + 0.5 i	0	0

Table 21: Pole sensitivities

R5	0.5 + 0.5 i	0.5 - 0.5 i	0	0
R6	-0.5 - 0.5 i	-0.5 + 0.5 i	0	0
R7	0	0	$- 5\ 10^{-7}$	$- 5\ 10^{-7}$
R8	0	0	-0.5 - 0.5 i	-0.5 + 0.5 i
R9	0	0	0.5 + 0.5 i	0.5 - 0.5 i
R10	0	0	$- 10^{-6} + i$	$- 10^{-6} + i$
R11	0	0	-0.5 - 0.5 i	-0.5 + 0.5 i
R12	0	0	-0.5 - 0.5 i	-0.5 + 0.5 i
C1	-0.5 + 0.5 i	-0.5 - 0.5 i	0	0
C2	-0.5 - 0.5 i	-0.5 + 0.5 i	0	0
C3	0	0	-0.5 - 0.5 i	-0.5 + 0.5 i
C4	0	0	-0.5 + 0.5i	-0.5 - 0.5i

The ambiguity groups are given in Table 22.

Table 22: Ambiguity groups at the output node

Groups	1	2	3	4	5	6	7	8	9
Elements	R_3, R_4, R_6, C_2	R_8, R_{11}, R_{12}, C_3	R_1, R_7	R_2	C_4	R_9	C_1	R_5	R_{10}

In order to validate the ambiguity groups, the normalized sensitivities of low-pass frequency (frequency domain specification) and rise time (time domain specification) with respect to the filter elements are computed using the Saber simulator and are given in Table 23 (cf. Appendix A).

Table 23: Normalized sensitivities of the low-pass frequency and rise time

Normalized sensitivity of low-pass frequency with respect of the filter elements								
R_3, R_4, R_6, C_2	R_8, R_{11}, R_{12}, C_3	R_1, R_7	R_2	C_4	R_9	C_1	R_5	R_{10}
-0.379	-0.591	$-6.\ 10^{-6}$	0.379	-0.15	0.59	-0.00649	0.229	0.411
Normalized sensitivity of rise time with respect of the filter elements								
R_3, R_4, R_6, C_2	R_8, R_{11}, R_{12}, C_3	R_1, R_7	R_2	C_4	R_9	C_1	R_5	R_{10}
0.484	0.592	-0.0074	-0.649	0.125	-0.555	-0.21	-0.44	-0.428

The zero at node 10 is equal to $z|_{10}$ = -10000 and zero sensitivities is given in Table 24.

Table 24: Zero sensitivities at node 10

Zero sensitivities with respect to the circuit elements															
R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}	C_1	C_2	C_3	C_4
0	0	0	0	0	0	0	0	0	-1	0	0	0	0	0	-1

Node 10 does not give more information about the ambiguity groups. Thus, the zero cannot break up the above ambiguity groups.

4.3.4. The 5-Pole (100Hz) low-pass filter

This example is selected from [Pan97c] to show the pole and zero cancellation effect on the testability measure and ambiguity groups. The schematic of the filter is shown in Figure 4-8.

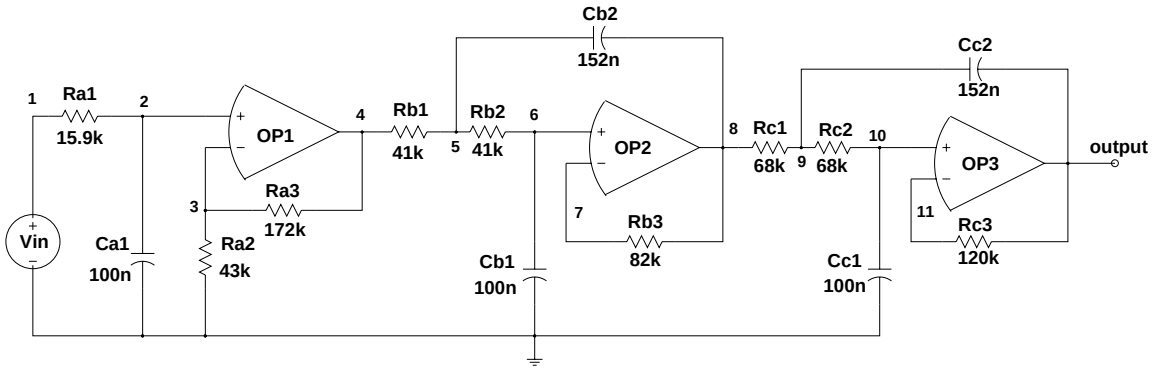


Figure 4-8: The schematic of the 5-pole low pass filter

The poles and zeros of the filter are given in Table 25.

Table 25: The poles and zeros of the filter

Poles	zeros at node 4	zeros at node 5	zeros at node 8	zeros at node 9
-160.463-115.709 i	-160.463-115.709 i			
-160.463+115.709 i	-160.463+115.709 i			
-96.75 - 69.7658 i	-96.75 - 69.7658 i	-96.75 + 69.7658 i	-96.75 + 69.7658 i	
-96.75 + 69.7658 i	-96.75 + 69.7658 i	-96.75 - 69.7658 i	-96.75 - 69.7658 i	
-628.931		-243.902		-147.059

The testability measure at the output is $T_t = 6$, (no zeros and $c = 1$). The pole sensitivities are given in Table 26.

Table 26: Pole sensitivities

h	S^{p1}_h	S^{p2}_h	S^{p3}_h	S^{p4}_h	S^{p5}_h
R_{a1}	-1	0	0	0	0
R_{a2}	0	0	0	0	0
R_{a3}	0	0	0	0	0
R_{b1}	0	$-0.5 - 5.3\ 10^{-6}$ i	$-0.5 + 5.3\ 10^{-6}$ i	0	0
R_{b2}	0	$-0.5 + 5.3\ 10^{-6}$ i	$-0.5 - 5.3\ 10^{-6}$ i	0	0
R_{b3}	0	0	0	0	0
R_{c1}	0	0	0	$-0.5 - 5.3\ 10^{-6}$ i	$-0.5 + 5.3\ 10^{-6}$ i
R_{c2}	0	0	0	$-0.5 + 5.3\ 10^{-6}$ i	$-0.5 - 5.3\ 10^{-6}$ i
R_{c3}	0	0	0	0	0
C_{a1}	-1	0	0	0	0
C_{b1}	0	-0.5 - 0.693 i	-0.5 + 0.693 i	-0	0
C_{b2}	0	-0.5 + 0.693 i	-0.5 - 0.693 i	0	
C_{c1}	0	0	0	-0.5 - 0.693 i	-0.5 + 0.693 i
C_{c2}	0	0	0	-0.5 + 0.693 i	-0.5 - 0.693 i

The ambiguity groups are given in Table 27.

Table 27: Ambiguity groups at the output

Group	1	2	3	4
Elements	R_{a1}, C_{a1}	R_{a2},R_{a3},R_{b3},R_{c3}	R_{b1}, R_{b2}	R_{c1}, R_{c2}

The other elements are definitely testable. The low-pass frequency sensitivities are computed using the Saber simulator in order to validate the above results and are given in Table 28.

Table 28: The low-pass frequency sensitivities (nominal value = 16.703 Hz)

1	2	3	4	5	6	7	8
C_{c1}	R_{c1}, R_{c2}	C_{b1}	R_{b1}, R_{b2}	C_{c2}	C_{b2}	C_{a1}, R_{a1}	R_{a2}, R_{b3}, R_{a3}, R_{c3}
-0.425	-0.251	-0.245	-0.088	-0.074	-0.069	-0.016	0

In pole-zero cancellation, the testability measure at nodes 4,5,8, and 9 is given in Table 29.

Table 29: Testability measures of 5-pole filter at nodes 4, 5, 8, and 9

T_t at node 4	T_t at node 5	T_t at node 8	T_t at node 9
2	5	4	7

Node 9 provides the best testability information in terms of the number of testable elements. The ambiguity groups at node 8 are given in Table 30.

Table 30: Ambiguity groups at node 8

Groups	1	2	3	4	5
Elements	C_{b1}	R_{b1}, R_{b2}	C_{a1}, R_{a1}	C_{b2}	R_{a2}, R_{b3}, R_{a3}, R_{c3}, R_{c1}, R_{c2}, C_{c1}, C_{c2}

The low-pass frequency sensitivities at node 8 are computed using the Saber simulator and are given in Table 31.

Table 31: Ambiguity groups at node 8

Groups	C_{b1}	R_{b1}, R_{b2}	C_{a1}, R_{a1}	C_{b2}	R_{a2}, R_{b3}, R_{a3}, R_{c3}, R_{c1}, R_{c2}, C_{c1}, C_{c2}
Sens.	-0.99	-0.458	-0.0884	0.138	0

It is worthwhile indicating that the state variables which are represented by the voltage across the capacitors C_{c1} and C_{c2} are not observable, because the pole sensitivities and zero sensitivities with respect to these capacitors are equal (cf. Section 4.2.6).

4.4. Generalization of the Testability Analysis Algorithm

In the previous examples, only *AC* ambiguity groups are considered. However, it is simply to combine *DC* ambiguity groups and *AC* ambiguity groups. From Eq (4-37) the K_0 is the *DC* gain and is a function of the circuit elements. The *DC* sensitivity is computed by the derivative of the K_0 with respect to the circuit elements (the capacitors and inductors are not considered). Furthermore, the poles and zeros are assumed to be distinct. If we consider, both, *DC* and pole-zeros sensitivities as well as the cases of repeated poles and pole-zero cancellation, the testability measure and ambiguity groups can be determined by the following matrix.

$$T_{matrix} = \begin{bmatrix} \frac{h_1}{p_1}\frac{\partial p_1}{\partial h_1} & \frac{h_1}{p_2}\frac{\partial p_2}{\partial h_1} & \cdots & \frac{h_1}{p_n}\frac{\partial p_n}{\partial h_1} & \frac{h_1}{z_1}\frac{\partial z_1}{\partial h_1} & \frac{h_1}{z_2}\frac{\partial z_2}{\partial h_1} & \cdots & \frac{h_1}{z_m}\frac{\partial z_m}{\partial h_1} & \frac{h_1}{K_0}\frac{\partial K_0}{\partial h_1} \\ \frac{h_2}{p_1}\frac{\partial p_1}{\partial h_2} & \frac{h_2}{p_2}\frac{\partial p_2}{\partial h_2} & \cdots & \frac{h_2}{p_n}\frac{\partial p_n}{\partial h_2} & \frac{h_2}{z_1}\frac{\partial z_1}{\partial h_2} & \frac{h_2}{z_2}\frac{\partial z_2}{\partial h_2} & \cdots & \frac{h_2}{z_m}\frac{\partial z_m}{\partial h_2} & \frac{h_2}{K_0}\frac{\partial K_0}{\partial h_2} \\ \vdots & \vdots & & \vdots & \vdots & \vdots & & \vdots & \vdots \\ \frac{h_k}{p_1}\frac{\partial p_1}{\partial h_k} & \frac{h_k}{p_2}\frac{\partial p_2}{\partial h_k} & \cdots & \frac{h_k}{p_n}\frac{\partial p_n}{\partial h_k} & \frac{h_k}{z_1}\frac{\partial z_1}{\partial h_k} & \frac{h_k}{z_2}\frac{\partial z_2}{\partial h_k} & \cdots & \frac{h_k}{z_m}\frac{\partial z_m}{\partial h_k} & \frac{h_k}{K_0}\frac{\partial K_0}{\partial h_k} \end{bmatrix} \quad (4\text{-}45)$$

The testability measure can be computed by the rank of the matrix T_{matrix}

$$T_t = rank(T_{matrix}) \quad (4\text{-}46)$$

The ambiguity groups are determined by the linearly dependent rows of the testability matrix.

For example, for the leapfrog filter, the *DC* sensitivity at the output is given in Table 32.

Table 32: *DC* sensitivities

DC sensitivities with respect to the circuit elements											
R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
-1	10^{-6}	1	-10^{-6}	10^{-6}	0	-1	$-2\ 10^{-6}$	$2\ 10^{-6}$	$2\ 10^{-6}$	$-2\ 10^{-6}$	1

The *DC* ambiguity groups are given in Table 33.

Table 33: *DC* ambiguity groups

Groups	1	2	3	4	5	6
Elements	R_1, R_7	R_2, R_5	R_4, R_8, R_{11}	R_3, R_{12}	R_9, R_{10}	R_6

The ambiguity groups resulting from pole-zero and *DC* sensitivities are given in Table 34.

Table 34: Total ambiguity groups

Groups	1	2	3	4	5	6	7	8	9	10	11	12
Elements	R_1,R_7	R_6,C_2	R_8, R_{11},C_3	R_2	R_3	R_4	R_5	R_9	R_{10}	R_{12}	C_1	C_4

Consequently, the combination of the *DC* and *AC* analysis provides the maximum information about ambiguity groups.

Moreover, the *DC* and pole-zero sensitivities can be used to compute the differential sensitivity of the transfer function by the derivation of Eq. (4-37) with respect to the circuit element. The resulting equation is given in Eq. (4-47)

$$S_{x_j}^{H(s)}(s, x_j) = S_{x_j}^{K_0} - \sum_{i=1}^{n} \frac{s}{s - z} S_{x_j}^{z_i} + \sum_{i=1}^{m} \frac{s}{s - p_i} S_{x_j}^{p_i} \tag{4-47}$$

The incremental sensitivity given by Eq. (2-8) can also compute the *DC* and pole-zero sensitivities. The sensitivity of the denominator can be computed as follows

$$S_{x_j}^{D} = S_{x_j}^{b_0} + \sum_{i=1}^{n} \frac{s}{s - p_i} S_{x_j}^{p_i} \tag{4-48}$$

Thus, the pole-zero sensitivity can be utilized for sensitivity analysis applications in analog testing such as fault diagnosis [Slam92, Liu94, Pang01], test signal generation [Slam95, Saab96, Hami96], and test measurement selection [Sten87,Hami93, Spaa96b].

4.5. Summary

In this chapter, a new methodology for the testability measure and ambiguity group determination was presented based on the well-known pole and zero analysis and on pole-zero sensitivity. Testability measure at a certain node of a circuit can be computed from the number of the poles and zero in addition to the *DC* gain of the transfer function. Also, the testability measure can be computed directly from the circuit matrix as given in Eq. (4-43). The ambiguity groups can be determined using the pole and zero sensitivity. Thus, the ambiguity group can be interpreted as a group of circuit elements which affect the poles and zeros (and the *DC* gain if the *DC* sensitivities are taken into account) of a circuit in the same way.

The main advantages of this methodology can be summarized as follows:

1) Our methodology is based on the pole-zero analysis and on the pole-zero sensitivity which can be employed in many applications such as stability of the control system, design and optimization of filters, compensation circuits in feedback amplifiers, simplification of the symbolic transfer function, behavioral modeling, and model order reduction.
2) The proposed methodology is independent of the frequency, unlike the sensitivity analysis where the sensitivity must be evaluated at each frequency point for the arbitrary range of the frequency. Furthermore, the normalized sensitivity is undefined at the zeros of the transfer function (the zero frequencies), and is equal to zero at the poles of the transfer

function (the pole frequencies), thus no information is provided at these frequency points (cf. Eq. 2-5).

3) This methodology provides a new interpretation of the ambiguity groups based on the circuit theory, unlike the matrix manipulation techniques which provide the mathematical interpretation given by the linearly dependent columns of the testability matrix.
4) The proposed method provides the relationship between the concept of the controllability and observability and testability measure. The controllability and observability essentially govers the existence of a solution to control problem, this is similar to the testability which also govers the solution of the diagnosis problem of the analog circuits.
5) The ambiguity groups, which are determined using numerical methods, depend on circuit specifications. Thus, the ambiguity groups are different from one specification to another. In contrast, our methodology provides the ambiguity groups which are the same for all circuit specifications in the time domain or in the frequency domain.
6) The sensitivity analysis can be achieved based on the pole-zero sensitivity analysis (cf. Eq (4-47) and Eq. (4-48)). Thus, the applications of the sensitivity analysis in an analog test such as fault diagnosis, and test signal generation can also be achieved based on the pole-zero sensitivity analysis.

The analog and mixed-signal circuits have a large number of specifications. Checking all specifications is a very time-consuming task. For this reason, an algorithm for selecting relevant specifications is required in order to reduce the test cost without affecting the quality of the test in terms of fault coverage.

In the following chapters, we will address the measurement selection problem based on the pole-zero analysis. The selection of specifications that have to be measured depends on the element testability concept which can be obtained based on the pole sensitivity.

Chapter 5

Element Testability and Measurement Selection for Second-Order Circuits

5.1. Introduction

Analog and mixed-signal circuits have large numbers of specifications. Checking all these specifications can result in prohibitive testing times. Therefore, minimizing the specifications that need to be measured is required to reduce the test cost. The reduction of the test cost can be performed by ordering the tests to achieve high fault coverage or by dropping some specifications to reduce test time [Milo98]. The shortcoming of these algorithms is that they do not provide the complete link between the circuit elements and circuit specifications.

Selecting a subset of specifications that have to be measured can be performed using the sensitivity analysis which provides the relation between the circuit elements and the performances. This relationship can be obtained by the ratio of the relative deviation of the circuit performance to the relative deviation of the circuit elements as a function of the frequency [Slam96] or the time [Dai90]. The sensitivity analysis ensures both the structural and functional test, where the circuit elements are tested by verifying the circuit functionality.

The measurement selection methods based on the sensitivity analysis are proposed in several previous works such as in [Sten87, Sten89, Dai90, Hami93, Slam96, Spaa96b]. However, since the sensitivity analysis is dependent on the frequency or the time, there is a need for handling a large matrix which is constructed by circuit sensitivities. The objective of the measure-

ment selection based on the sensitivity analysis is to improve the fault coverage, but the reduction of the test cost is not considered.

In order to overcome the shortcomings of the above-mentioned methods, we will present an algorithm for measurement selection which is independent of the frequency or the time. The aim of this algorithm is to reduce test cost by reducing the number of specifications that need to be measured. The selected specifications can serve as a signature in fault simulators to improve the fault coverage and to evaluate the test vectors applied at the inputs of the circuit under test. Also, this algorithm provides maximum information about the fault identification for fault diagnosis by breaking up the ambiguity groups.
The proposed measurement selection algorithm is based on the element testability concept which can be computed based on the sensitivity of the circuit poles. The element testability will provide the information about the difficulty in testing the circuit elements as well as the effect of the changes of the circuit elements on the circuit specifications.

We will devote this chapter to the discussion of the element testability and measurement selection for second-order circuits. Higher-order circuits will be addressed in Chapter 6.
The algorithm is valid for parametric faults which caused by manufacturing process variations and do not affect the circuit topology. This algorithm can be classified under the specification-based test.

5.2. The Algorithm

The second-order system plays an important role in understanding the analysis and the design of higher-order systems. In filter design, second-order filters can be cascaded to realize a higher-order filter. Cascade design is employed for the design of active filters which are designed by op-amps and RC circuits. A higher transfer function of the cascade is constructed by the product of the transfer function of the second-order blocks, without changing the transfer functions of the individual blocks [Sed98]. Furthermore, several higher-order systems can be approximated by second-order systems [Kou95].

The element testability and measurement selection algorithm for a prototype of a second-order circuit is given as follows:

Step 1. Represent a second-order circuit by the transfer function form in the Laplace domain which can be generated using the circuit matrix or the state-variable equations.

Step 2. Compute the poles of the transfer function by utilizing the *QZ* algorithm.

Step 3. Compute the natural response specifications (ζ, *Q*-factor, ω_n) based on the location of the circuit poles.

Step 4. Select the desired specifications (in time and frequency domains) which can be computed based on the natural response specifications. Such specifications are rise time, settling time, low-cutoff frequency, bandwidth etc.

Step 5. Compute the pole sensitivities using the adjoint methods as discussed in Section (4.2.3).

Step 6. Compute the element testability of the circuit elements with respect to the selected specifications.

Step 7. Select the specifications that have to be measured to test the circuit elements corresponding to the maximum element testability. The goal of the measurement selection is to obtain a high fault coverage for parametric faults.

Step 8. In order to reduce the test cost, drop the specifications which do not affect fault coverage.

Step 9. For the fault diagnosis, select the specifications which provide maximum information about the fault identification (i.e. select the specifications which break up the ambiguity groups).

In the next section, we will discuss the measurement selection algorithm for prototype second-order circuits in detail. Some simulation examples are presented at the end of the chapter in order to validate the proposed algorithm.

5.2.1. Mathematical Representation of Prototype Second-Order Circuits

The second order circuit can be represented by its transfer function as follows [Chua87]:

$$H(s) = \frac{Y(s)}{U(s)} = \frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5-1}$$

where ζ is the damping ration and ω_n is the natural frequency.

The characteristic polynomial for the differential equation in Laplace domain can be written (the denominator *D(s)* of the transfer function):

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \tag{5-2}$$

The roots of the characteristics equation are called the natural frequencies of the circuit (identical to the poles of the circuit) and are given:

$$s_{1,2} = -\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} = -\alpha \pm j\omega \tag{5-3}$$

$$\alpha = \zeta\omega_n \qquad \omega = \omega_n\sqrt{1-\zeta^2}$$

where the real part α called the damping factor and the imaginary part ω called damped frequency of oscillation.

The natural frequency ω_n can be computed as follows:

$$\omega_n = \sqrt{(\alpha)^2 + (\omega)^2} \tag{5-4}$$

The quality factor (*Q*-factor) is given:

$$Q = -\frac{\omega_n}{2\alpha} = \frac{1}{2\zeta} \tag{5-5}$$

The specifications ω_n, ζ, and *Q*-factor are called natural response specifications.

- **Time Domain Specifications**

The time domain specifications of the unit-step response are defined as follows [Kou95]:

Peak time t_{max} is defined as the time required to reach to the first maximum peak.

Rise time t_r is defined as the time required for the step response to rise from 10 to 90 percent of its final value.

Settling time t_s is defined as the time required for the step response to decrease and stay within a specified percentage of its final value (frequently = *5%*).

Maximum overshoot OS% is defined as the difference between the maximum value of the step response at the peak time t_{max} and the unit-step response (steady-state value) and given as:

$$OS = y_{max} - y_{unit-step} \tag{5-6}$$

The maximum overshoot is often represented as the percentage of the final value of the step response as:

$$OS\% = \frac{OS}{y_{unit-step}} \cdot 100\,\% \tag{5-7}$$

The time-domain specifications, the peak time t_{max}, the rise time t_r, the settling time t_s, and maximum overshoot *OS%* are shown in Figure 5-4.

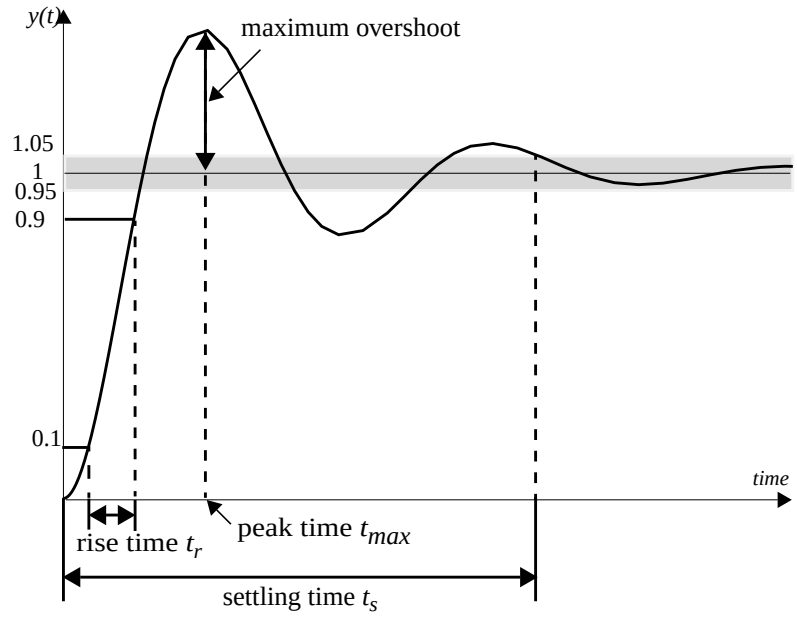


Figure 5-4: Time domain specifications of the unit-step response

These specifications can be determined as a function of the pole location of the circuit, in other words they can be evaluated as a function of the natural response specifications (ζ and ω_n). These specification are given [Kuo95]:

$$t_{max} = \frac{\pi}{\omega_n\sqrt{1-\zeta^2}} \tag{5-8}$$

$$OS\% = 100e^{-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}} \tag{5-9}$$

$$t_r \cong \frac{0.8 + 2.5\zeta}{\omega_n} \tag{5-10}$$

$$t_s \cong \frac{3.2}{\zeta\omega_n} \qquad for \quad 0 < \zeta < 0.69 \tag{5-11}$$

$$t_s = \frac{4.5\zeta}{\omega_n} \qquad for \quad \zeta > 0.69 \tag{5-12}$$

- **Frequency Domain Specification**

The following frequency-domain specifications for the second-order low-pass filter are often used in practice [Kou95]:

Resonant peak M_r is defined as the maximum value of the $|M(j\omega)|$.

Resonant frequency ω_r is defined as the frequency at which the peak resonant M_r occurs.

Bandwidth BW is defined as the frequency at which $|M(j\omega)|$ drops to 70.7 percent of, or 3dB down from its zero-frequency value.

The equations of the frequency domain specifications as a function of the natural response specifications are given

$$\omega_r = \omega_n\sqrt{1-2\zeta^2} \tag{5-13}$$

$$M_r = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \tag{5-14}$$

$$BW = \omega_n\sqrt{(1-2\zeta^2)+\sqrt{\zeta^4-4\zeta^2+2}} \tag{5-15}$$

The response of the low-pass filter in frequency-domain is shown in Figure 5-5.
Other frequency-domain specifications of all the second-order filter types which are related to the pole location (or the natural response specifications) are found in [Sedr98].

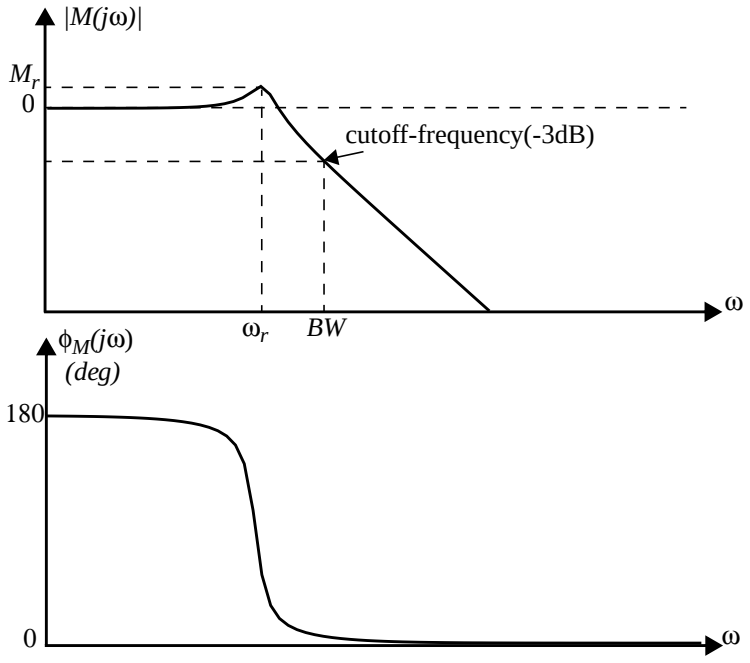


Figure 5-5: The frequency response of the second-order low-pass filter

5.2.2. Pole Sensitivity

The pole sensitivities with respect to the circuit elements are computed using the adjoint methods [Vla94] (cf. Chapter 4). This algorithm can be summarized:

1) Insert $s = p_i$ into the modified nodal matrix Y and obtain the LU factors $(Y = LU)$.

2) Use back substitution to find x from $Ux = e_n$, where e_n is the nth unit vector.

3) Use back substitution to find x^a from $L^t x^a = 0$, (setting the $x^a{}_n = 1$ and finding $x^a{}_{n-1}$ in turn).

4) For each element h_i, form $\delta Y/\delta h_i$, apply Eq. (5-16) to compute the pole sensitivity

$$\frac{\partial p_i}{\partial h} = -\frac{(X^a)^t \frac{\partial Y}{\partial h} X}{(X)^t C X} \tag{5-16}$$

5.2.3. Element Testability and Measurement Selection

The concept of the element testability ET can be defined as the degree of difficulty in testing a circuit element h with respect to a specification SP.

Mathematically, the element testability of the circuit elements with respect to the circuit specifications can be expressed as:

$$ET(h, SP) = S_h^{SP} \tag{5-17}$$

The element testability $ET(h, SP)$ can be expressed for second-order circuits with a small element deviation (small Δh) as a function of the relative deviation of a specification SP and the relative deviation of the circuit element h as

$$ET(h, SP) = \frac{\frac{\Delta SP}{SP}}{\frac{\Delta h}{h}} \tag{5-18}$$

The element testability also provides information about the effect of each element variation of the circuit on the circuit specifications.

The element testability of the circuit elements with respect to the natural response specifications can be expressed as [Herp86]

$$ET(h, \omega_n) = S_h^{\omega_n} = Re\{S_h{}^p\} \tag{5-19}$$

$$ET(h, Q) = S_h{}^Q = -S_h{}^\zeta = -\sqrt{4Q^2 - 1} \cdot Im\{S_h{}^p\} \tag{5-20}$$

$$ET(h, \zeta) = -ET(h, Q) \tag{5-21}$$

where *p* is a circuit pole and *h* is a circuit element.

The sensitivity formulas of the time domain specifications are derived based on the above equations and on the properties of the first-order sensitivity. These formulas are given in Appendix A. Then the element testability *ET(h, SP)* of the circuit elements with respect to the time-domain specification is equal to the sensitivity of the time specification *SP* associated to the circuit elements ($ET(h, SP) = S^{SP}_{h}$).

The sensitivity of the frequency domain specifications as a function of the sensitivity of the natural response specifications are given in Appendix A. These sensitivities represent the element testability *ET(h, Sp)*, where *SP* is a frequency-domain specification.

The specifications that have to be measured for testing the circuit element *h* is selected corresponding to the maximum value of the element testability as

$$SP|_{h} = max(|ET(h, SP)|) \tag{5-22}$$

5.3. Simulation Examples

5.3.1. Continuous-Time State-Variable Filter

The schematic of the continuous-time state-variable filter is given [Kami97]:

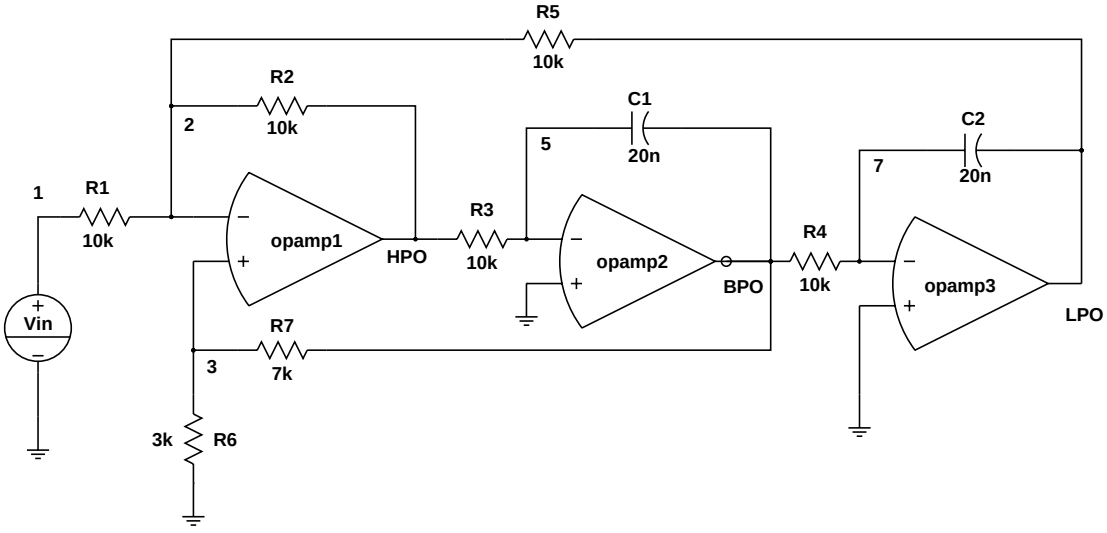


Figure 5-6: Schematic of the Continuous-Time State-Variable Filter

The poles of the filter are P_1 = 2250. + 4465.13 i and P_2 = 2250. - 4465.13 i

The pole sensitivity of the filter is given in Table 35.

Table 35: Pole sensitivities

h	$S^{p1}{}_h$	$S^{p2}{}_h$
R_1	$3.5\ 10^{-7}$ + 0.16796 i	$3.5.\ 10^{-7}$ - 0.16796 i
R_2	0.5 - 0.08398 i	0.5 + 0.08398 i
R_3	- 0.5 + 0.25195 i	- 0.5 - 0.25195 i
R_4	- 0.5 - 0.25195 i	- 0.5 + 0.25195 i
R_5	- 0.5 - 0.08398 i	- 0.5 + 0.08398 i
R_6	$3.15\ 10^{-7}$ - 0.35273 i	$3.15\ 10^{-7}$ +0.3527 i
R_7	$-\ 3.15\ 10^{-7}$ + 0.35273 i	$-\ 3.15\ 10^{-7}$ - 0.35273 i
C_1	- 0.5+ 0.25195 i	- 0.5 - 0.25195 i
C_2	- 0.5- 0.25195 i	- 0.5 + 0.25195 i

The natural response specifications are given in Table 36.

Table 36: Natural response specifications

natural frequency ω_n	*Q*-factor	damping ratio ζ
5000	1.1111	0.45

The sensitivities of the natural response specifications associated to circuit elements are computed based on Eq. (5-10), Eq (5-20) and Eq. (5-21) and are given in Table 37. These sensitivities represent the element testability *ET(h, SP)*. The absolute value of the damping ratio ζ sensitivity is identical to the absolute value of the Q-factor sensitivity. Hence only Q-factor or damping ratio ζ can be measured to test the parametric faults in the circuit elements R_1, R_6, and R_7 while the other elements can be tested by measuring the natural frequency ω_n as shown in Table 38.

Table 37: Element testability of the circuits elements w.r.t. the natural response specifications

h	*ET(h, ω_n)*	*ET(h, Q)*	*ET(h, ζ)*
R_1	$3.5\ 10^{-7}$	0.3333	-0.3333
R_2	0.5	-0.1666	0.1666
R_3	-0.5	0.5	-0.5

Table 37: Element testability of the circuits elements w.r.t. the natural response specifications

h	*ET(h, ω_n)*	*ET(h, Q)*	*ET(h, ζ)*
R_4	-0.5	-0.5	0.5
R_5	-0.5	-0.1666	0.1666
R_6	$3.15\ 10^{-7}$	-0.7	0.7
R_7	$-3.15\ 10^{-7}$	0.7	-0.7
C_1	-0.5	0.5	-0.5
C_2	-0.5	-0.5	0.5

As a result, The element testability of the resistors R_1, R_6, and R_7 with respect to the ω_n is very low. Furthermore, since ω_n sensitivity is related to the real part of the pole sensitivity, the ambiguity groups with respect to the ω_n are {R_3, R_4, C_1, C_2, R_5}, {R_1, R_6, R_7}, {R_2}.

Table 38: The specifications that have to be measured

R_1	R_2	R_3	R_4	R_5	R_6	R_7	C_1	C_2
Q or ζ	ω_n	ω_n, *Q or* ζ	ω_n, *Q or* ζ	ω_n	*Q or* ζ	*Q or* ζ	ω_n, *Q or* ζ	ω_n, *Q or* ζ

On the other hand, the element testability of the filter elements with respect to the *Q*-factor is related to the imaginary part of the poles of the transfer function, thus the ambiguity groups can be determined based on the imaginary part of the poles as {R1}, {R2, R5}, {R3, C1}, {R4,C4}, {R6}, {R7}. The specifications that have to be measured if the ambiguity groups are taken into account and given in Table 39.

Table 39: The specifications that have to be measured

R_1	R_2	R_3, C_1	R_4, C_2	R_5	R_6	R_7
Q or ζ	ω_n	*Q or* ζ	*Q or* ζ	ω_n	*Q or* ζ	*Q or* ζ

In order to compute the element testability using Eq. (5-18), the natural response specifications and their relative deviations are computed using the Saber simulator [Anal97] as given in Table 40. The deviation of the filter elements is assumed to be equal to +10%.

Table 40: Relative deviation of the natural response specifications

h	actual ω_n	$\Delta\omega_n / \omega_n$	actual Q	$\Delta Q / Q$	actual ζ	$\Delta\zeta / \zeta$
nominal	5000	0	1.1111	0	0.45	0
+10% in R_1	5000	0	1.1458	0.03123	0.4363	-0.03044
+10% in R_2	5244	0.0488	1.0925	-0.01674	0.45766	0.01702
+10% in R_3	4767.3	-0.04654	1.1653	0.04878	0.429	-0.04666
+10% in R_4	4767.3	-0.04654	1.0594	-0.04653	0.47196	0.0488
+10% in R_5	4767.3	-0.0488	1.0925	-0.01674	0.45766	0.01702
+10% in R_6	5000	0	1.0404	-0.06363	0.48	0.06666
+10% in R_7	5000	0	1.1889	0.07	0.42056	-0.06666
+10% in C_1	4767.3	-0.04654	1.1653	0.04878	0.429	-0.04666
+10% in C_2	4767.3	-0.04654	1.0594	-0.04653	0.4719	0.0488

The element testability as a function of the relative deviation of the natural response specifications and the relative deviation of the circuit elements are given in Table 41 ($\Delta h / h = 0.1$). The results in Table 41 are very close to the element testability reported in Table 37. However, the sensitivity evaluation for each element h using Eq. (5-18) requires the formulation and solution of the system equations, resulting in high computational cost. Furthermore, the incremental values $\Delta SP/\Delta h$ tend toward the differential sensitivity only in the limit as Δh --> *0*, and a very small value of Δh in computations is precluded by roundoff errors. These difficulties are avoided by using Eq. (5-17) as above discussed.

Table 41: Relative deviation of the natural response specifications computed by element testability of the circuit elements w.r.t. ζ, Q, and ω_n

h	*ET(h, ω_n)*	*ET(h, Q)*	*ET(h, ζ)*
R_1	0	0.3123	-0.3044
R_2	0.488	-0.1674	0.1702
R_3	-0.4654	0.4878	-0.4666
R_4	-0.4654	-0.04653	0.488
R_5	-0.488	-0.1674	0.1702
R_6	0	-0.6363	0.6666

Table 41: Relative deviation of the natural response specifications computed by element testability of the circuit elements w.r.t. ζ, Q, and ω_n

h	$ET(h, \omega_n)$	$ET(h, Q)$	$ET(h, \zeta)$
R_7	0	0.7	-0.6666
C_1	-0.4654	0.4878	-0.4666
C_2	-0.4654	-0.4653	0.488

The step response of the continuous-time state-variable filter is shown in Figure 5-7 (*u(t)=-1 volt*).

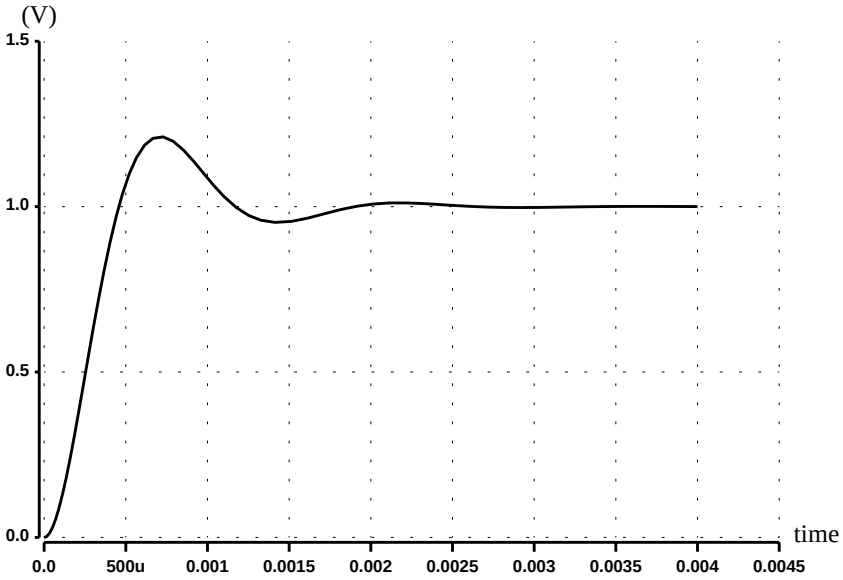


Figure 5-7: Step response of the state-variable filter

The time-domain specifications are given in Table 42.

Table 42: Time domain specifications

peak time t_{max}	settling time t_s	overshoot *OS%*	rise time t_r
0.000703582	0.00142222	20.5346	0.000385

The element testability of the circuit elements with respect to the time-domain specifications is computed by the equations given in Appendix A and given in Table 43.

Table 43: Element testability of the circuit elements w.r.t. the time-domain specifications

h	$ET(h, t_{max})$	$ET(h, t_s)$	$ET(h, OS)$	$ET(h, t_r)$
R_1	-0.0846395	0.333332	0.661673	-0.194805

Table 43: Element testability of the circuit elements w.r.t. the time-domain specifications

h	*ET(h, t_{max})*	*ET(h, t_s)*	*ET(h, OS)*	*ET(h, t_r)*
R_2	-0.45768	-0.666663	-0.330833	-0.402598
R_3	0.373041	0.999999	0.992511	0.20779
R_4	0.626959	$1.11111\ 10^{-6}$	-0.992511	0.792207
R_5	0.542319	0.333332	-0.33084	0.597402
R_6	0.177742	-0.699998	-1.38951	0.40909
R_7	-0.177742	0.699998	1.38951	-0.40909
C_1	0.373041	0.999999	0.992511	0.207793
C_2	0.626959	$1.11111\ 10^{-6}$	-0.992511	0.792207

The filter elements can be tested by selecting the specification given in Table 44.

Table 44: Measurement selection of the time-domain specifications

Element	R_1	R_2	R_3, C_1	R_4, C_2	R_5	R_6	R_7
SP	*OS*	t_s	*OS*	*OS*	t_r	*OS*	*OS*

Note that the above selected measurements provide the maximum information about the ambiguity groups. In order to reduce the test cost by reducing the specification tests, the elements R_2 and R_5 can be tested using only the rise time t_r which provides a reasonable element testability value of the element R_2 (i.e. dropping the settling time t_s does not affect the detectability of the faults in R_2 and R_5).

The element testability of the circuit elements with respect to the time-domain specifications is computed using Eq. (5-17) by Saber simulator [Anal97]. The element deviations is equal to $\Delta h/h = 0.1$. The element testability is given in Table 45. By comparing the values in both tables, we note that the element testability values reported in Table 45 are very close to the element testability values in Table 43.

Table 45: Element testability of the circuit elements w.r.t. the time-domain specifications computed by the relative deviation of the time-domain specifications

h	*ET(h, t_{max})*	*ET(h, t_s)*	*ET(h, OS%)*	*ET(h, t_r)*
+10% in R_1	-0.0752689	0.314004	0.615691	-0.177922
+10% in R_2	-0.423458	0.624879	-0.334396	-0.370442

Table 45: Element testability of the circuit elements w.r.t. the time-domain specifications computed by the relative deviation of the time-domain specifications

h	*ET(h, t_{max})*	*ET(h, t_s)*	*ET(h, OS%)*	*ET(h, t_r)*
+10% in R_3	0.368805	1.00152	0.953177	0.202077
+10% in R_4	0.623838	0.00138299	-0.940204	0.786415
+10% in R_5	0.534136	0.312574	-0.329643	0.592453
+10% in R_6	0.179649	-0.625	-1.27046	0.38961
+10% in R_7	-0.159726	0.700019	1.37846	-0.38961
+10% in C_1	0.368805	1.00152	0.953177	0.202077
+10% in R_1	0.623838	0.00138299	-0.940204	0.786415

The response of the LPO output of the filter in frequency-domain is shown in Figure 5-8.

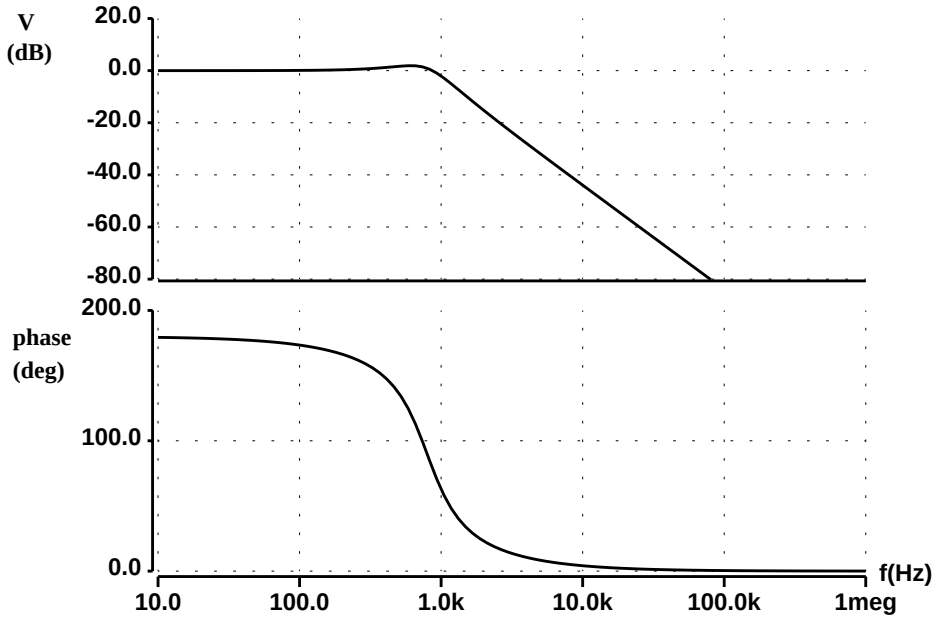


Figure 5-8: Frequency response (Bode plot) of the low-pass frequency output (LPO)

The frequency-domain specifications of the low-pass filter (LPO) are given in Table 46.

Table 46: Frequency-domain specifications of the LPO

peak resonant ω_r	peak resonant frequency M_r	bandwidth *BW*
613.831 Hz	1.2442	1038.94 Hz

The element testability of the circuit elements with respect to the frequency-domain specifications of the LPO are given in Table 47.

Table 47: Element testability of the circuit elements w.r.t. the frequency-domain specifications of the LPO

h	*ET(h, ω_r)*	*ET(h, M_r)*	*ET(h, BW)*
R_1	0.22689	0.248693	0.105891
R_2	0.386555	-0.124345	0.447054
R_3	-0.159665	0.37304	-0.341163
R_4	-0.840335	-0.37304	-0.658837
R_5	-0.61344	-0.124348	-0.552945
R_6	-0.476469	-0.522256	-0.222371
R_7	0.476469	0.522256	0.222371
C_1	0.159665	0.37304	-0.341163
C_2	-0.840335	-0.37304	-0.658837

The filter elements can be tested using the specifications given in Table 48.

Table 48: measurement section of the frequency-domain specifications

Element	R_1	R_2	R_3, C_1	R_4, C_2	R_5	R_6	R_7
SP	M_r	*BW*	M_r	ω_r	ω_r	M_r	M_r

For test time reduction, the element R_2 can be tested by ω_r, hence the BW can be considered as redundant measurement. Furthermore, we note that the resonant frequency ω_r provides reasonable element testability of the circuit elements, thus the circuit elements can be tested using only the resonant frequency ω_r.

The element testability of the circuit elements with respect to the frequency-domain specifications is computed using Eq. (5-17) by the Saber simulator. The element deviation is equal to $\Delta h/h = 0.1$. The element testability is given in Table 49.

Table 49: Element testability of the LPO computed by the relative deviation of the frequency-domain specifications

h	*ET(h, ω_r)*	*ET(h, M_r)*	*ET(h, BW)*
+10% in R_1	0.202032	0.236372	0.127813

Table 49: Element testability of the LPO computed by the relative deviation of the frequency-domain specifications

h	*ET(h, ω_r)*	*ET(h, M_r)*	*ET(h, BW)*
+10% in R_2	0.0364721	-0.12423	0.410167
+10% in R_3	-0.174054	0.370182	-0.280967
+10% in R_4	-0.794613	-0.342494	-0.672938
+10% in R_5	-0.577472	-0.12423	-0.536158
+10% in R_6	-0.480449	-0.498003	-0.302596
+10% in R_7	0.429435	0.523482	0.27205
+10% in C_1	-0.174054	0.370182	-0.280967
+10% in C_2	-0.794613	-0.342494	-0.672938

By comparing the values in two tables, we note that the values reported in Table 50 are very close to the values in Table 48.

5.3.2. Sallen-Key Bandpass Filter

The schematic of the Sallen-Key bandpass filter is shown in Figure 5-9 [Dai90].

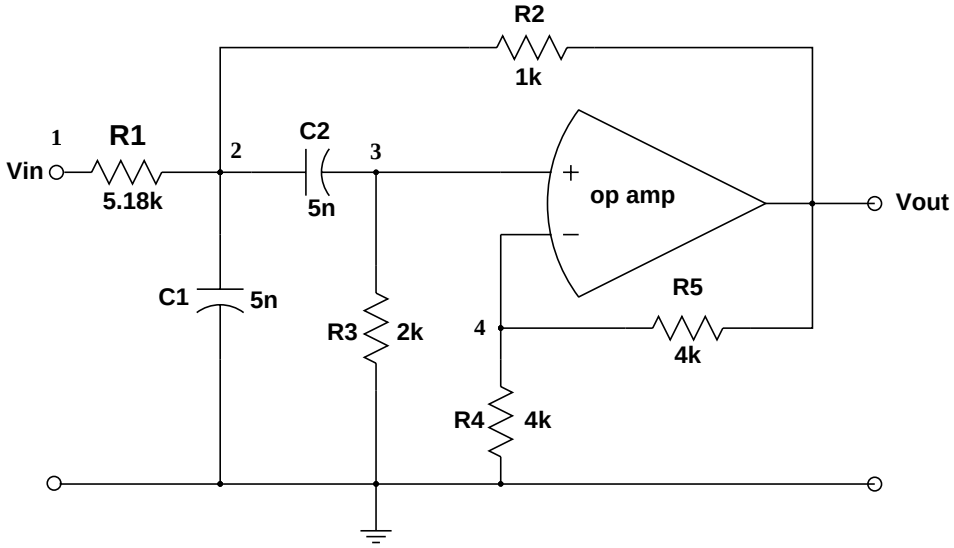


Figure 5-9: The schematic of the Sallen-Key bandpass filter

The poles of the filter are P_1 = -19309 - 153258 i and P_2 = -19309 + 153258 i

The pole sensitivities are given in Table 50.

Table 50: Pole sensitivities

h	$S^{p1}{}_h$	$S^{p2}{}_h$
R_1	-0.0809061 + 0.11577 i	-0.0809061 - 0.11577 i
R_2	-0.419094 - 0.705268 i	-0.419094 - 0.705268 i
R_3	-0.5 + 0.589497 i	-0.5 - 0.589497 i
R_4	-0.652488 i	+0.652488 i
R_5	+0.652466 i	-0.652466 i
C_1	-0.5 - 0.263251 i	-0.5 + 0.263251 i
C_2	-0.5 + 0.263251 i	-0.5 - 0.263251 i

The natural response specifications of the filter are given in Table 51.

Table 51: Natural response specifications of the filter

natural frequency ω_n	*Q*-factor	damping ratio ζ
154470	3.99995	0.125002

The sensitivities of the natural response specifications are given in Table 53.

Table 52: Sensitivities of the natural response specifications

h	$ET(h, \omega_n)$	$ET(h, Q)$	$ET(h, \zeta)$
R_1	-0.0809061	0.918888	-0.918888
R_2	-0.419094	-5.59782	5.59782
R_3	-0.5	4.67893	-4.67893
R_4	0	-5.17872	5.17872
R_5	0	5.17872	-5.17872
C_1	-0.5	-2.08947	2.08947
C_2	-0.5	2.08947	-2.08947

It is clear the filter elements can be tested by selecting the *Q*-factor or the damping ratio ζ which also provides maximum information for fault identification for fault diagnosis.

The element testability of the filter elements with respect to the natural response specifications computed using the relative deviation of the natural response specifications (computed using

the Saber simulator) are given in Table 54. In this case, the relative deviation of the filter elements is assumed to be equal to ($\Delta h / h = 0.05$).

Table 53: Element testability computed by relative deviation of the natural response specifications

h	*ET(h, ω_n)*	*ET(h, Q)*	*ET(h, ζ)*
R_1+5%	-0.077685	0.918761	-0.918761
R_2+5%	-0.402667	-4.2798	4.2798
R_3+5%	-0.481647	5.90682	-5.90682
R_4+5%	0	-3.9563	3.9563
R_5+5%	0	6.98834	-6.98834
C_1+5%	-0.481647	-1.85527	1.85527
C_2+5%	-0.481647	2.26328	-2.26328

The step response of the filter is shown in Figure 5-10.

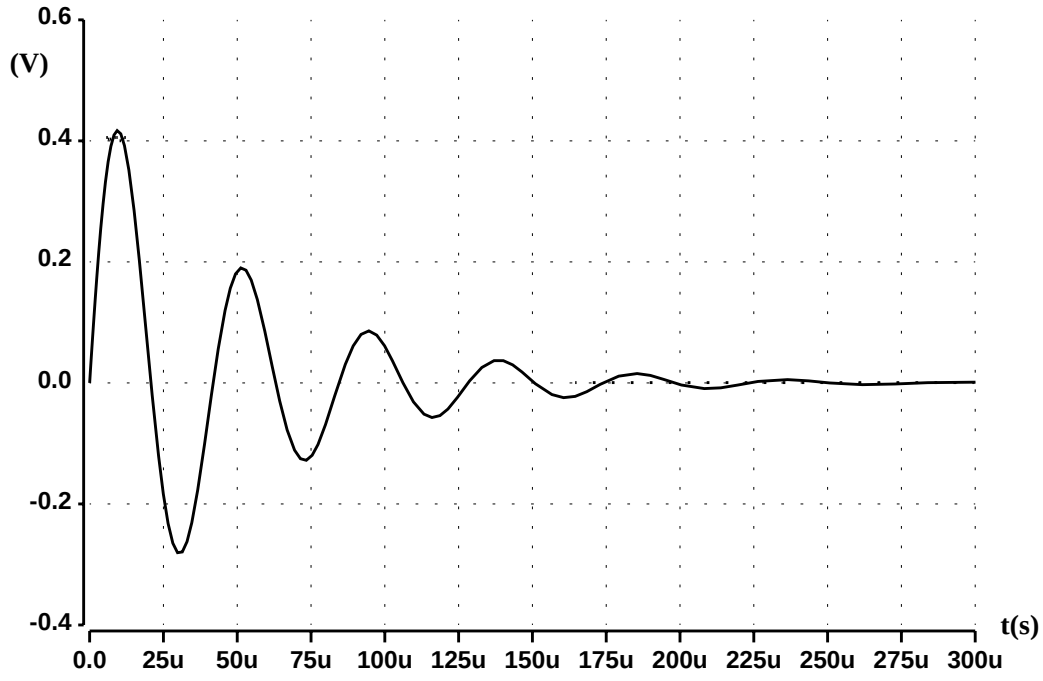


Figure 5-10: Step response of the Sallen-Key bandpass filter

The time-domain specifications of the filter are given in Table 54.

Table 54: Time-domain specifications of the filter

peak time t_{max} (µsec)	settling time t_s (µsec)	overshoot *OS%*	rise time t_r (µsec)
20.4987	165.728	67.3139	7.20205

The element testability of the circuit elements with respect to the time-domain specifications are given in Table 55.

Table 55: Element testability of the filter elements w.r.t. the time-domain specifications

h	*ET(h, t_{max})*	*ET(h, t_s)*	*ET(h, OS%)*	*ET(h, t_r)*
R_1	0.0663206	0.999794	0.369472	-0.177208
R_2	0.507948	-5.17873	-2.25081	-1.99151
R_3	0.425731	5.17893	1.88133	-0.814307
R_4	0.082202	-5.17872	2.08229	1.4547
R_5	-0.082202	5.17872	2.08229	-1.4547
C_1	0.533166	1.58947	-0.840145	1.08693
C_2	0.466834	2.58947	0.840145	-0.0869285

Clearly, the filter elements can be tested by selecting the settling time t_s. The other specifications can be considered as redundant. However, the ambiguity groups {R3, R5} have to be broken up by other measurements. In this case, a further measurement like e.g. rise time t_r can be selected for measurement.

The element testability of the filter elements with respect to the time-domain specifications computed using the relative deviation of the time-domain specifications (computed using Saber simulator) are given in Table 56. In this case, the relative deviation of the filter elements is assumed to be equal to ($\Delta h / h = 0.05$).

Table 56: Element testability computed using the relative deviation of the time-domain specifications

h	*ET(h, t_{max})*	*ET(h, t_s)*	*ET(h, OS%)*	*ET(h, t_r)*
R_1+5%	0.0643121	1.00032	0.355959	-0.169716
R_2+5%	0.511892	-3.95669	-2.08769	1.9718
R_3+5%	0.428135	6.54603	1.92792	-0.818975

Table 56: Element testability computed using the relative deviation of the time-domain specifications

R_4+5%	0.0885387	-3.95688	-1.89973	1.38562
R_5+5%	0.0711757	6.98793	2.18155	-1.45465
C_1+5%	0.52858	-1.40738	-0.807507	1.08209
C_2+5%	0.46221	2.81318	0.83264	-0.0917998

The response of the filter in frequency domain is shown in figure 5-11.

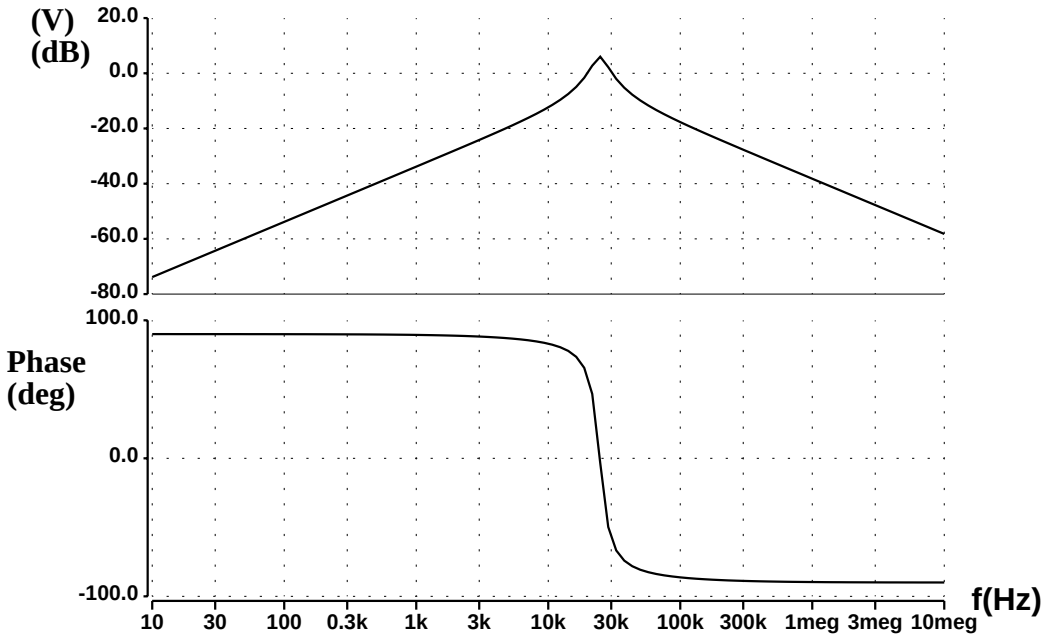


Figure 5-11: The response of the filter in frequency domain

The frequency-domain specifications of the filter are given in Table 57.

Table 57: The frequency-domain specifications of the filter

low-frequency f_L*(Hz)*	high-frequency f_H *(Hz)*	bandwidth *BW (Hz)*	f_{max}*(Hz)*
21702.9	27849.1	6146.17	24584.7

The element testability of the filter elements are given in Table 58.

Table 58: Element testability of the filter elements w.r.t. the frequency-domain specifications

h	*ET(h,* f_L*)*	*ET(h,* f_H*)*	*ET(h, BW)*	*ET(h,* f_{max}*)*
R_1	0.0348487	-0.196661	-0.999794	-0.0809061

Table 58: Element testability of the filter elements w.r.t. the frequency-domain specifications

h	$ET(h, f_L)$	$ET(h, f_H)$	$ET(h, BW)$	$ET(h, f_{max})$
R_2	-1.12427	0.286079	5.17873	-0.419094
R_3	0.089418	-1.08942	-5.17893	-0.5
R_4	-0.652378	0.652378	5.17872	0
R_5	0.652378	-0.652378	-5.17872	0
C_1	-0.763216	-0.236784	1.58947	-0.5
C_2	-0.236784	-0.763216	-2.58947	-0.5

The filter elements can be tested by selecting the *BW*. However, the ambiguity groups {R_2, R_4}, and {R_3, R_5} can be broken up by selecting another specification such as high-cutoff frequency f_H. The other specifications can be considered to be redundant.

The element testability of the filter elements with respect to the frequency-domain specifications computed using the relative deviation of the frequency-domain specifications (computed using the Saber simulator) are given in Table 59. In this case, the relative deviation of the filter elements is assumed to be equal to ($\Delta h / h = 0.05$).

Table 59: Element testability computed using the relative deviation of the frequency-domain specification

h	$ET(h, f_L)$	$ET(h, f_H)$	$ET(h, BW)$	$ET(h, f_{max})$
R_1+5%	0.0311764	-0.185955	-0.952673	-0.077685
R_2+5%	-1.05191	0.268824	4.93251	-0.402667
R_3+5%	0.0791327	-1.02676	-4.93183	-0.481647
R_4+5%	-0.601361	0.620004	4.9328	0
R_5+5%	0.653958	-0.633252	-5.17856	0
C_1+5%	-0.727404	-0.232756	1.51391	-0.481647
C_2+5%	-0.233737	-0.726448	-2.46627	-0.481647

The results in both Table 60 are closed to the results reported in Table 59.

The selection of the circuit specifications that have to be measured is so far considered for each domain (i.e. the time-domain and the frequency-domain). However, the combination between the specifications which need to be selected in the both domains is also possible.

5.4. Summary

In this chapter, we have presented a methodology for selecting the circuit specifications that must be measured. The selected measurements can be utilized for obtaining high fault coverage or evaluating the test vectors in a fault simulator, reducing the test cost by reducing the number of tests without affecting the fault coverage, and for breaking up the ambiguity groups if the fault diagnosis is the goal of a test. The measurement selection algorithm is based on the concept that is called the element testability. The element testability concept provides information about the difficulty in testing the circuit elements (parametric faults caused by process variation) with respect to circuit specifications as well as providing the information about the effect of the variations of the circuit elements on the circuit specifications. The values of the element testability can be easily obtained via the sensitivities of the circuit poles.

The measurement selection algorithm can be applied for first-order and second-order circuits which form the basic of the construction of higher-order circuits. The measurement selection algorithm for higher-order circuits is discussed in the next chapter.

Chapter 6

Element Testability and Measurement Selection for Higher-Order Circuits

6.1. Introduction

For higher-order circuits, we can no longer use the damping ratio ζ, the Q-factor, and the natural frequency ω_n which are defined for prototype second-order systems. However, if the system dynamics can be accurately represented by a pair of complex-conjugate dominant poles, we can still use ζ, Q, and ω_n to indicate the dynamics of the transient response.

In this chapter, we present an algorithm for element testability and measurement selection for higher-order circuits that can be approximated by the second-order circuits. Then, the algorithm discussed in the previous chapter for measurement selection can be employed in order to reduce test time, improve fault coverage, and provide maximum information for fault identification.

6.2. The algorithm

For higher order circuits, we have these two cases: (a) the higher order circuit has two complex-conjugate dominant poles, and (b) the higher order circuit has no dominant pole.

a) The higher order circuit has two complex-conjugate dominant poles. In this case, the algorithm for element testability and measurement selection can be summarized as follows:

Step 1. Represent the higher-order circuits in the transfer function form in the Laplace domain which can be generated using the circuit matrix or using the state-variable equations as discussed in Section (4.2.1).

Step 2. Compute the poles of the transfer function by utilizing the *QZ* algorithm as discussed in Section (4.2.2).

Step 3. Consider the effect of the two complex-conjugate dominant poles and neglect the effect of the other poles.

Step 4. Compute the natural response specifications (ζ, Q, ω_n) based on the location of the dominant poles.

Step 5. Select the desired specifications (in the time and frequency domains) which are related to the natural response specifications.

Step 6. Compute the sensitivities of the dominant poles using the adjoint methods as discussed in Section (4.2.3).

Step 7. Compute the element testability of the circuit elements with respect to the desired specifications based on the sensitivity of the natural response specifications.

Step 8. Select the measurements which correspond to the maximum element testability to be performed to test parametric faults in circuit elements.

b) The higher order circuit has no dominant pole. In this case, the algorithm can be, thusly, summarized:

Step 1. Approximate a higher-order circuit by a second-order circuit using model-order reduction techniques. In our algorithm, a moment matching algorithm called the asymptotic waveform evaluation (AWE) algorithm [Pill95] is used for approximating a higher-order circuit by a second-order one.

Step 2. Compute the natural response specifications (ζ, Q-factor, ω_n) based on the location of the approximate poles.

Step 3. Select the desired specifications (in the time and frequency domains) which are related to the natural response specifications.

Step 4. Compute the pole sensitivities with respect to the elements of the original circuit using the AWE algorithm.

Step 5. Compute the element testability of the circuit elements with respect to the desired specifications based on the sensitivity of the natural response specifications.

Step 6. Select the measurements which correspond to the maximum element testability to be performed to test parametric faults in circuit elements.

The circuit representation and pole-zero calculation were discussed in Chapter 4, hence we will discuss how the approximation of the a higher order circuit by a second-order one.

6.2.1. Dominant Poles

The location of the poles of a transfer function in the *s*-plan greatly affects the transient and frequency responses of the system. It is important to extract the poles that have a dominant effect on the system response. These poles are called *dominant poles* [Kou95].

The *s*-plan regions can be divided into two regions according to the dominant and insignificant poles as shown in Figure 6.1. The poles that are close to the imaginary axis in the left-half *s*-plan have a dominant effect on the time and frequency responses, whereas in contrast, the poles that are far away from the imaginary axis have neglected effects on the time and frequency responses. The distance *D* between the two regions can be determined if the value of the real part of a pole is at least 5 to 10 times of a dominant poles [Kou95].

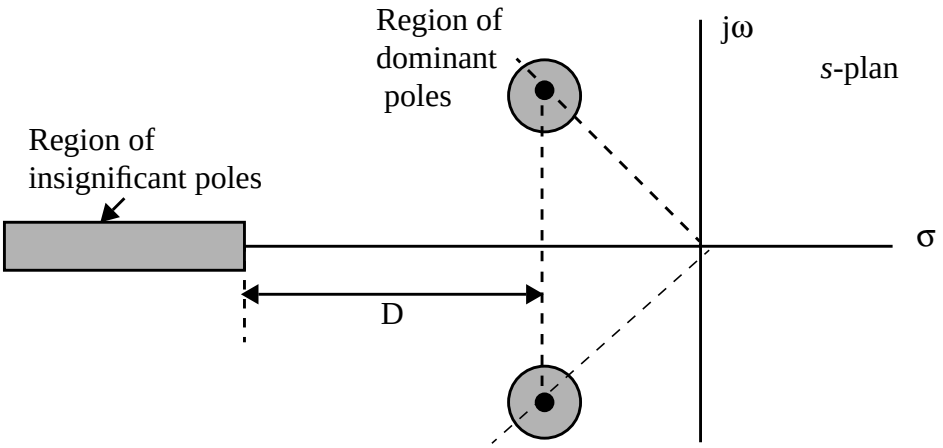


Figure 6-1: Region of dominant and insignificant poles in the *s*-plan

Example: Consider the following transfer function

$$M(s) = \frac{1}{(s+20)(s^2+2s+2)}$$

The poles of the transfer function are P_1 = -20, P_2 = -2+i, P_3 = -2-i. The effect of P_1 can be neglected. Then the approximate transfer function can be given as

$$M(s) \cong \frac{1}{s^2+2s+2}$$

If a higher-order circuit can be approximated with reasonable accuracy by a second-order circuit, the natural response specifications described in the previous chapter can still employ it for element testability computation and measurement section.

6.2.2. Model-Order Reduction

Model-order reduction techniques approximate the higher-order system by the lower-order system with reasonable accuracy in order to reduce the effort of the analysis and the design. The reduction is performed by extracting the dominant poles (eigenvalues) of higher-order circuits that have a dominant effect on the transient and frequency responses.

Moment matching used in the linear systems analysis as a method of model-order reduction and is employed to extract a small set of dominant poles from a large network. The information is obtained from the Taylor series and the Páde approximation of the original system. Many algorithms of moment matching are proposed such as asymptotic waveform evaluation (AWE) [Chip94, Pill95], Arnoldi algorithm [Silv95], and Lanczos algorithm [Feld95].
The asymptotic waveform evaluation (AWE) method can be easily understood and implemented [Chip94, Pill95]. Moreover, AWE provides an efficient method for the sensitivity analysis which is the motivation for selecting this method.
AWE extracts a small approximate set of poles and residues, or a small approximate transfer function; for a large network that may hundreds of actual poles. The CPU cost is approximately equal to a *DC* analysis of the network. In our algorithm, we will only extract the two complex-conjugate dominant poles.
The AWE consists of two main steps: (1) moment generation, and (2) moment matching.

6.2.2.1. Moment Generation

The moments of the transfer function can be generated using either the modified nodal analysis (MNA) formulation [Chip94] or the state space formulation [Pill95].

- **MNA Formulation**

The MNA of the linear network in the Laplace domain can be given

$$[Y(s)][X(s)] = \left[b\right] \tag{6-1}$$

where *Y(s)* is the modified nodal matrix, *X(s)* is the solution vector which can be composed of currents and voltages, and *b* is the source vector.

Y(s) and *X(s)* are a function of the complex frequency *s*. The system matrix *Y(s)* can be expressed as $Y = G + sC$, where *G* and *C* are real matrices and *s* is the complex frequency variable.

Expanding X(s) in a Maclaurin series yields

$$\left[G + sC\right]\left[M_0 + M_1 s + M_2 s^2 + \ldots\right] = \left[b\right] \tag{6-2}$$

Equating like powers of *s* gives a recursive relationship for the moments:

$$GM_0 = b \tag{6-3}$$

$$GM_i = -CM_{i-1} \tag{6-4}$$

Because the matrices G and C represent sparse matrices, the solution of Eq. (6-3) and Eq. (6-4) can be accomplished efficiently. Furthermore, any invertible matrix *G* can be decomposed into triangular matrices $G = LU$. Thus, the computational cost of the moments is equal to one *LU* decomposition. This is approximately equal in *CPU* time to a *DC* solution of the circuit equations.

The number of the moments necessary depends on the order of the approximation. In general, when construction a *q*-pole approximate transfer function, *2q* moments are needed.

- **State Space Formulation**

The differential state equations for a circuit driven by the single input *u(t)* are given

$$\begin{aligned} x'(t) &= A \cdot x(t) + B \cdot u(t) \\ y(t) &= C \cdot x(t) + D \cdot u(t) \end{aligned} \tag{6-5}$$

Applying the Laplace Transform to these equations yields

$$\begin{aligned} sX(s) - x(0) &= AX(s) + BU(s) \\ Y(s) &= CX(s) + DU(s) \end{aligned} \tag{6-6}$$

Assuming $u(t) = \delta(t)$ $(U(s) = 1)$ and $x(0) = 0$ then

$$\begin{aligned} X(s) &= (sI - A)^{-1} B = \left[(I - sA^{-1})(-A)\right]^{-1} B \\ X(s) &= -A^{-1}(I - sA^{-1})^{-1} B \end{aligned} \tag{6-7}$$

Expanding $(I - sA^{-1})^{-1}$ about $s = 0$:

$$X(s) = -A^{-1}(I + sA^{-1} + s^2 A^{-2} + s^3 A^{-3} + \ldots)B \tag{6-8}$$

The vector of the coefficients of the powers of *s* are directly related to the moments of the impulse response at all the state variables:

$$M_0 = -A^{-1}B \tag{6-9}$$

$$M_i = -A^{-(i+1)}B = A^{-1}M_{i-1} \tag{6-10}$$

The *LU* factorization of the matrix *A* is employed once to obtain the moment M_0 and recursively to obtain the higher moments M_i.

6.2.2.2. Moment Matching

The transfer function of a linear circuit can be expressed as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_m s^m}{1 + b_1 s + b_2 s^2 + \ldots + b_n s^n} \qquad m < n \tag{6-11}$$

If the input is equal to the single impulse function $\delta(t)$, this leads to $H(s) = V_{out}(s)$.

The transfer function in the complex frequency domain (the Laplace domain) can be expanded as series in powers of *s*:

$$H(s) = M_0 + M_1 s + M_2 s^2 + M_3 s^3 + \ldots \tag{6-12}$$

From the Eq. (6-11) and the Eq. (6-12) yields

$$(1 + b_1 s + b_2 s^2 + \ldots)(M_0 + M_1 s + M_2 s^2 + M_3 s^3 + \ldots) = a_0 + a_1 s + a_2 s^2 + \ldots \tag{6-13}$$

The coefficients of the numerator a_i*'s* can be expressed in terms of the moments M_i*'s* and the denominator b_i*'s:*

$$\begin{aligned} a_0 &= M_0 \\ a_1 &= M_0 b_1 + M_1 \\ a_2 &= M_0 b_2 + M_1 b_1 + M_2 \\ &\ldots \\ a_q &= M_0 b_q + M_1 b_{q-1} + M_2 b_{q-2} + \ldots + M_{q-1} b_1 + M_q \end{aligned} \tag{6-14}$$

The coefficients of the denominator b_i*'s* can be expressed in terms of the moments M_i*'s* and given in matrix form:

$$\begin{bmatrix} M_0 & M_1 & \ldots & M_{q-1} \\ M_1 & M_2 & \ldots & M_q \\ \ldots & \ldots & \ldots & \ldots \\ M_{q-1} & M_q & \ldots & M_{2q-1} \end{bmatrix} \begin{bmatrix} b_q \\ b_{q-1} \\ \ldots \\ b_1 \end{bmatrix} = - \begin{bmatrix} M_q \\ M_{q+1} \\ \ldots \\ M_{2q-1} \end{bmatrix} \tag{6-15}$$

or

$$M_h b_v = M_v \tag{6-16}$$

where q is the order of the approximate transfer function which needs 2q moments to be computed.

The poles p_j of the approximate transfer function can be computed by finding the roots of the denominator polynomial

$$D(s) = 1 + b_1 s + b_2 s^2 + \ldots + b_q s^q \tag{6-17}$$

The residues of the transfer function can be obtained using the following equation

$$\begin{bmatrix} 1 & 1 & \ldots & 1 \\ p_1^{-1} & p_2^{-1} & \ldots & p_q^{-1} \\ \ldots & \ldots & \ldots & \ldots \\ p_1^{-q+1} & p_1^{-q+1} & \ldots & p_q^{-q+1} \end{bmatrix} \begin{bmatrix} k_1 \\ k_2 \\ \ldots \\ k_q \end{bmatrix} = \begin{bmatrix} M_0 \\ M_1 \\ \ldots \\ M_{q-1} \end{bmatrix} \tag{6-18}$$

The approximate transfer function can be expressed in pole-residue form as

$$H_q(s) = \sum_{i=1}^{q} \frac{k_i}{s - p_i} \tag{6-19}$$

In the time domain, an approximate impulse response can be given by

$$h(t) = \sum_{i=1}^{q} k_i e^{p_i t} \tag{6-20}$$

The steps involved in obtaining a low order approximation to a higher order circuit response via moment matching can be summarized:

I) Find the *2q* moments using the MNA formulation (Eq. (6-3) and Eq. (6-4)) or using the state space formulation (Eq. (6-9) and Eq. (6-10)).

II) Obtain a set of polynomial coefficients $\{b_q, b_{q-1}, b_{q-2}, \ldots, b_1\}$ form the solution of q equations in q unknowns in terms of the *2q* moments $\{M_0, M_1, \ldots, M_{2q-1}\}$ using Eq. (6-15).

III) Obtain the roots of the resulting characteristic equation Eq. (6-17).

IV) Find corresponding residues by solving Eq. (6-18)

V) Compute the required time-domain response as a sum of q exponential (Eq. (6-20)).

6.2.3. Pole and Zero Sensitivity Calculation in AWE

The transfer function of a linear system can be expressed in form of a ratio of the two polynomials namely the numerator and the denominator. The roots of the numerator and denominator polynomials are the zeros and poles of the linear circuit, respectively.

In order to compute the root sensitivity of the polynomial *P(s)*, first define the polynomial as

$$P(s) = \sum_{k=0}^{q} b_k s^k \tag{6-21}$$

where b_k is the coefficients of the polynomial *P(s)*.

Then the polynomial *P(s)* is evaluated at a root p_j, and the chain rule is applied to obtain the root sensitivity:

$$\left.\frac{\partial P}{\partial h}\right|_{s=p_j} = 0 = \sum_{k=0}^{q}\left(\frac{\partial b_k}{\partial h} p_j^{\,k} + k b_k \frac{\partial p_j}{\partial h} p^{k-1}\right) \tag{6-22}$$

where *h* is a circuit element.

Rearranging the Eq. (6-22) in terms of the pole sensitivity of interest,

$$\frac{\partial p_j}{\partial h} = -\frac{\sum_{k=0}^{q} \frac{\partial b_k}{\partial h} p_j^{\,k}}{\sum_{l=0}^{q} l b_l p^{l-1}} \tag{6-23}$$

Zero sensitivity can be computed in the same manner.

The sensitivity of the denominator coefficients can be calculated as follows:

$$M_h b_v = M_v \tag{6-24}$$

The coefficients can be computed by inverting M_h

$$b_v = M_h^{-1} M_v \tag{6-25}$$

The coefficient sensitivities are given as (for simplicity the index of the coefficients b have been not written)

$$\frac{\partial b}{\partial h} = M_h^{-1}\frac{\partial M_v}{\partial h} + \frac{\partial M_h^{-1}}{\partial h} M_v \tag{6-26}$$

Using the identity

$$\frac{\partial M_h^{-1}}{\partial h} = -M_h^{-1}\frac{\partial M_h}{\partial h} M_h^{-1} \tag{6-27}$$

the coefficient sensitivities are given as

$$\frac{\partial b}{\partial h} = M_h^{-1}\left(\frac{\partial M_v}{\partial h} - \frac{\partial M_h}{\partial h} b_v\right) \tag{6-28}$$

The sensitivity of the numerator coefficients $\delta a/\delta h$ can be computed by differentiating the Eq. (6-14) with respect to the circuit elements.

The moment sensitivity can be computed according to the MNA formulation (Eq. (6-3) and Eq. (6-4)) or according to the state space formulation (Eq. (6-9) and Eq. (6-10)).

The moment sensitivity according to the state space formulation can be written as [Pill95]

$$\frac{\partial M_0}{\partial h} = y^T \frac{\partial A}{\partial h} M_0 - y^T \frac{\partial B}{\partial h} \tag{6-29}$$

where y^T is the solution of the adjoint system given by the following equation.

$$A^T y = c \tag{6-30}$$

where c is a column vector with all zeros and a 1 in the row corresponding to the node of interest.

The sensitivities of the higher order moments can also be calculated recursively using the original and adjoint solution. In summary

$$\frac{\partial M_j}{\partial h} = \left(\sum_{i=1}^{j} y^T \frac{\partial A}{\partial h} M_{j-i} \right) - y_j^T \frac{\partial B}{\partial h} \tag{6-31}$$

where y_i is the vector for the *ith* adjoint solution:

$$y_i = (A^{-i-1})^T c \tag{6-32}$$

On the other hand, the moment sensitivity can be computed using the MNA formulation. The moments can be generated by

$$\begin{aligned} GM_0 &= b \\ GM_i &= -CM_{i-1} \end{aligned} \tag{6-33}$$

By differentiating these equations yields

$$\frac{\partial M_0}{\partial h} = G^{-1} \frac{\partial G}{\partial h} M_0 + G^{-1} \frac{\partial b}{\partial h} \tag{6-34}$$

$$\frac{\partial M_i}{\partial h} = -G^{-1} \left(\frac{\partial G}{\partial h} M_i + \frac{\partial C}{\partial h} M_{i-1} + \frac{\partial M_0}{\partial h} C \right) \tag{6-35}$$

For resistors (conductors), the moment sensitivity can be expressed as

$$\left. \frac{\partial M_0}{\partial h} \right|_{h=r,g} = G^{-1} \frac{\partial G}{\partial h} M_0 + G^{-1} \frac{\partial b}{\partial h} \tag{6-36}$$

$$\left. \frac{\partial M_i}{\partial h} \right|_{h=r,g} = -G^{-1} \left(\frac{\partial G}{\partial h} M_i + \frac{\partial M_0}{\partial h} C \right) \tag{6-37}$$

For capacitors and inductors, the moment sensitivity can be expressed as

$$\left.\frac{\partial M_0}{\partial h}\right|_{h = c,\, l} = G^{-1}\frac{\partial b}{\partial h} \tag{6-38}$$

$$\left.\frac{\partial M_i}{\partial h}\right|_{h = c,\, l} = -G^{-1}\left(\frac{\partial C}{\partial h}M_{i-1} + \frac{\partial M_0}{\partial h}\,C\right) \tag{6-39}$$

In order to determine the moment sensitivity corresponding to one output, the moment sensitivities are then multiplied by the vector d^T, where d^T is a column vector with all zeros and a "1" corresponding to the output of interest.

The sensitivities of the approximate poles and zeros found by AWE show excellent correlation with those of the original circuit and provide useful information in both the time and the frequency domain [Lee92].

6.2.4. Element Testability and Measurement Selection

The concept of the element testability *ET* for higher-order circuits can be defined as the degree of difficulty in testing a circuit element *h* with respect to a specification *SP*. Mathematically, the element testability of the circuit elements with respect to the circuit specifications can be expressed as:

$$ET(h, SP) = S_h^{SP} \tag{6-40}$$

where S_h^{SP} is the sensitivity of a specification *SP* with respect to the circuit element *h*.

The element testability provides the information about the effect of each element variation of the circuit on the circuit specifications.

The element testability of the circuit elements with respect to the natural response specifications (the *Q*-factor, damping ratio ζ, and natural frequency ω_n) can be expressed as a function of the pole sensitivity

$$ET(h, \omega_n) = S_h^{\omega_n} = Re\{S_h^{\,p}\} \tag{6-41}$$

$$ET(h, Q) = S_h^{\,Q} = -S_h^{\,\zeta} = -\sqrt{4Q^2 - 1}\cdot Im\{S_h^{\,p}\} \tag{6-42}$$

$$ET(h, \zeta) = -ET(h, Q) \tag{6-43}$$

The sensitivities of the approximate poles reflect the effect of the variations of the circuit elements on the circuit specifications in the original circuit.

The sensitivity formulas of time domain specifications are derived based on the above equations and the properties of the first-order sensitivity that are given in Appendix A. Then the element testability *ET(h, SP)* of the circuit elements with respect to time-domain specifications is equal to the sensitivity of the time-domain specification *SP* associated to the circuit elements ($ET(h, SP) = S_h^{SP}$).

The sensitivity of the frequency domain specifications as a function of the sensitivity of the natural response specifications are given in Appendix A. These sensitively represent the element testability *ET(h, SP)*, where *SP* is a frequency-domain specification.

The specification that have to be measured to test the circuit element *h* is selected corresponding to the maximum value of the element testability as

$$SP|_h = max(|ET(h, SP)|) \tag{6-44}$$

6.3. Simulation Examples

6.3.1. RLC Circuit

The schematic of the RLC circuit is given in Figure 6-2.

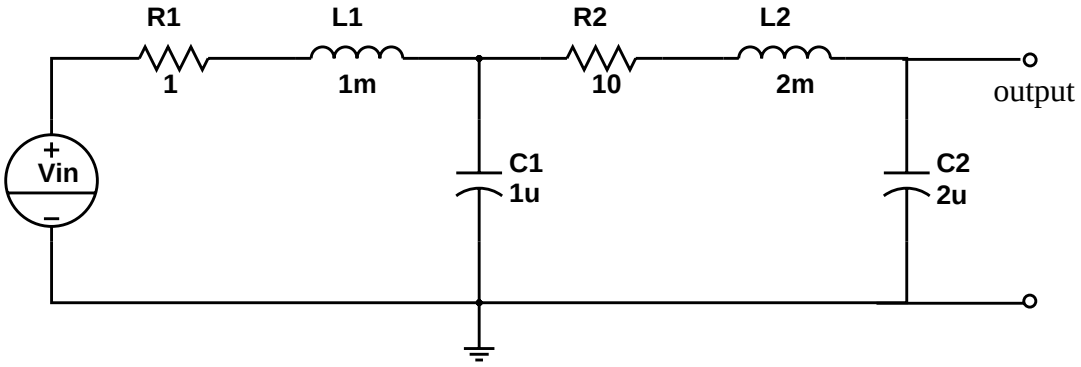


Figure 6-2: The schematic of the RLC circuit

The poles of the RLC circuit are given in Table 60.

Table 60: Poles of the original RLC circuit

P_1	P_2	P_3	P_4
-1678.71 + 12431.3 i	-1678.71 - 12431.3 i	-1321.29 + 39837.5 i	-1321.29 - 39837.5 i

The moments of the approximate second-order circuit are given in Table 61.

Table 61: Moments of the output

M_0	M_1	M_2	M_3
1	-0.000023	$-6.491\ 10^{-9}$	$2.86753\ 10^{-13}$

The coefficients of the denominator are given in Table 62.

Table 62: The coefficients of the denominator polynomial

b_1	b_2
0.0000195812	$6.94137\ 10^{-9}$

The poles of the second-order circuit (the roots of the polynomial $P(s)=1+b_1s+b_2s^2$) are given in Table 63.

Table 63: The poles of the approximate second-order circuit

P_1	P_2
-1410.47 - 11919.5 i	-1410.47 + 11919.5 i

The step responses of the original circuit and the approximate second-order circuit are shown in Figure 6-3.

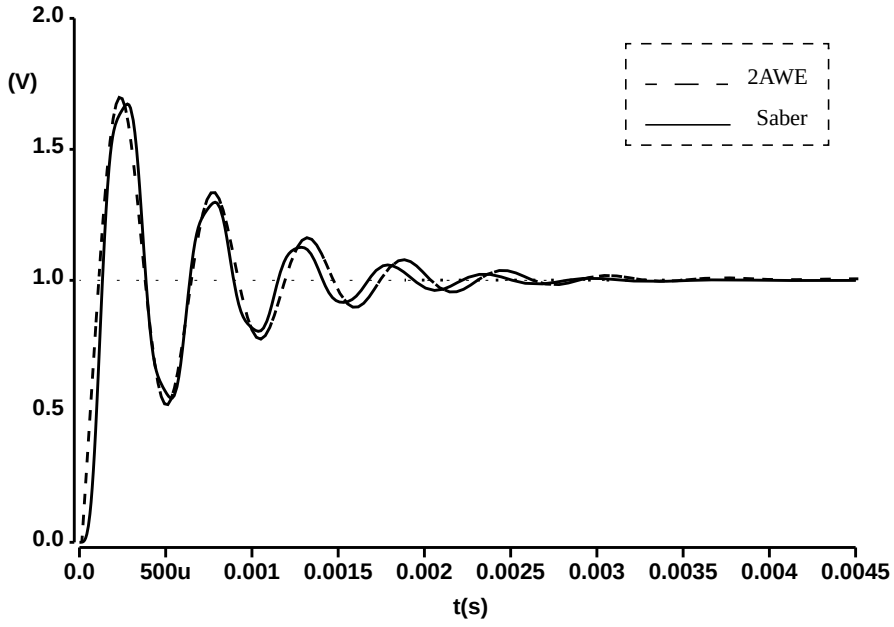


Figure 6-3:.Step time response of the original and approximate circuits

The natural response specifications (ω_n, ζ, and Q) of the approximate second-order circuit computed by the pole location of the approximate second-order circuit are given in Table 64.

Table 64: The natural response specifications of the approximate second-order circuit

ω_n	Q	ζ
12002.7	4.25484	0.117513

The pole sensitivity of the approximate second-order circuit with respect to the original circuit are given in Table 65.

Table 65: The pole sensitivities of the approximate second-order circuit

	S^{p1}_h	S^{p2}_h
R_1	0.000226022 - 0.0147718 i	0.000226022 + 0.0147718 i
R_2	0.00818852 - 0.104675 i	0.00818852 + 0.104675 i
C_1	-0.0683852 + 0.0197076 i	-0.0683852 - 0.0197076 i
C_2	-0.427408 - 0.0794309 i	-0.427408 + 0.0794309 i
L_1	-0.213796 + 0.033687 i	-0.213796 - 0.033687 i
L_2	-0.290411 + 0.0260363 i	-0.290411 - 0.0260363 i

The time domain specifications of the original circuit computed using the Saber simulator [Anal97] are given in Table 66.

Table 66: The time response specifications of the original circuits

t_r	t_s	$OS\%$	t_{max}
67.269 μsec	0.0018314 sec	67.181	278.08 μsec

The time domain specifications of the approximate second-order circuit computed by Eq. (5-12) to Eq (5-16) are given in Table 67.

Table 67: Time response specifications of the approximate circuit

t_r	t_s	$OS\%$	t_{max}
91.125 μsec	0.0022688	68.9531	263.567 μsec

The sensitivities of the natural response specifications are given in Table 68.

Table 68: Sensitivities of the natural response specifications

	ω_n *Sensitivities*	*Q Sensitivities*	ζ *Sensitivities*
R_1	0.000226022	0.124832	-0.124832
R_2	0.00818852	0.884577	-0.884577
C_1	-0.0683852	-0.166543	0.166543
C_2	-0.427408	0.671248	0.671248
L_1	-0.213796	-0.284679	0.284679
L_2	-0.290411	-0.220025	0.220025

The element testability of the circuit elements with respect to the time-domain specifications are given in Table 69.

Table 69: Element testability of the filter elements w.r.t. the time-domain specifications

	ET(h, t_{max})	*ET(h, t_s)*	*ET(h, OS%)*	*ET(h, t_r)*
R_1	-0.00197362	-0.125058	-0.0470513	0.0333004
R_2	-0.0205722	-0.892766	-0.333411	0.229384
C_1	0.0707168	0.234929	0.0627728	0.0236564
C_2	0.41801	-0.243841	-0.253004	0.607686
L_1	0.217782	0.498476	0.1073	0.13734
L_2	0.293491	0.510436	0.082931	0.231319

The specifications to be measured for testing the circuit elements are given in Table 70.

Table 70: Specifications to be measured

R1	R2	C1	C2	L1	L2
t_s	t_s	t_s	t_r	t_s	t_s

In order to reduce the test time by reducing the number of circuit specifications, the RLC circuit elements can be tested by selecting the settling time t_s. The other specifications can be considered as redundant.

In a similar manner, the element testability of the circuit elements with respect to the frequency-domain specifications can be computed.

6.3.2. Leapfrog Filter

The schematic of the leapfrog is shown in Figure 6- 4 [Kami97]

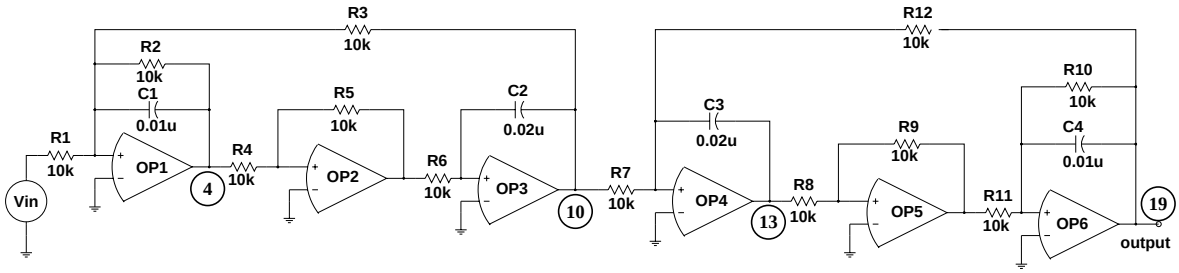


Figure 6- 4: The schematic of the leapfrog

The step response of the leapfrog filter is shown in Figure 6-5.

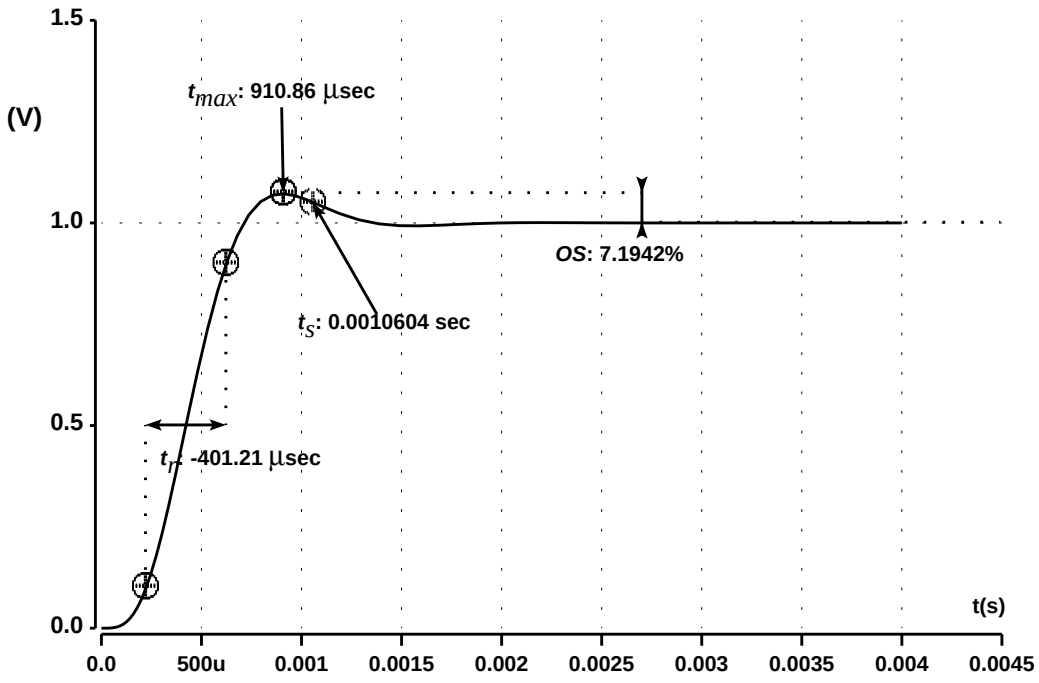


Figure 6-5: Step response of the leapfrog filter

The poles of the filter are given in Table 71.

Table 71: The poles of the leapfrog filter

P1	P2	P3	P4
-5000.01 - 4999.97 i	-5000.01 + 4999.97 i	-5000.01 - 4999.98 i	-5000.01 + 4999.98 i

The poles of the approximate second-order circuits are given in Table 72.

Table 72: The pole of the approximate second-order circuit

P1	P2
-3750 - 3307.17 i	-3750 + 3307.17 i

The time domain specifications are given in Table 73.

Table 73: The time domain specifications

rise time	maximum overshoot	settling time	t_{max}
401.21 msec	7.1942%	0.0010604 sec	910.86 msec

The frequency response of the filter is shown in Figure 6-6.

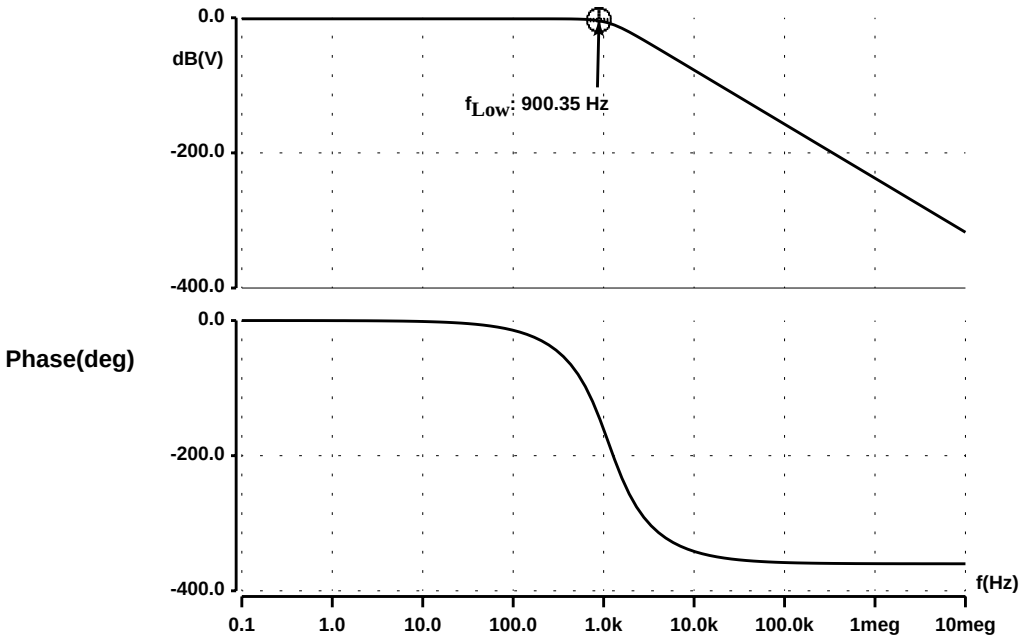


Figure 6-6: Bode plot of the output of the leapfrog filter

The low-cutoff frequency is only selected as an example to be measured in the frequency domain. Furthermore, we will combine the specifications of the time and frequency domain to select the specifications that are needed to be measured.

The sensitivities of the approximate poles are given in Table 74.

Table 74: The pole sensitivities of the approximate second-order filter

	$S^{p1}{}_h$	$S^{p2}{}_h$
R1	$2.5\ 10^{-7} + 4.7245\ 10^{-7}$ i	$2.5\ 10^{-7} - 4.7245\ 10^{-7}$ i
R2	0.25 + 0.47245 i	0.25 - 0.47245 i
R3	-0.375 - 0.236228 i	-0.375 + 0.236228 i
R4	-0.375 - 0.236228 i	-0.375 + 0.236228 i
R5	0.375 + 0.236228 i	0.375 - 0.236228 i
R6	-0.375 - 0.236228 i	-0.375 + 0.236228 i
R7	$-2.5\ 10^{-7}$	$-2.5\ 10^{-7}$
R8	-0.375 - 0.236228 i	-0.375 + 0.236228 i
R9	0.375 + 0.236228 i	0.375 - 0.236228 i
R10	0.25 + 0.47245 i	0.25 - 0.47245 i
R11	-0.375 - 0.236228 i	-0.375 + 0.236228 i
R12	-0.375 - 0.236228 i	-0.375 + 0.236228 i
C1	-0.12499 + 0.236228 i	-0.12499 - 0.236228 i
C2	-0.375 - 0.236228 i	-0.375 + 0.236228 i
C3	-0.375 - 0.236228 i	-0.375 + 0.236228 i
C4	-0.12499 + 0.236228 i	-0.12499 - 0.236228 i

The element testability of the leapfrog filter elements is given in Table 75.

Table 75: Element testability of leapfrog filter specifications

	$ET(h, t_s)$	$ET(h, t_{max})$	$ET(h, OS)$	$ET(h, t_r)$	$ET(h, f_L)$
R1	$1.66\ 10^{-7}$	$-7.857\ 10^{-7}$	$3.39\ 10^{-7}$	$-5.42\ 10^{-7}$	$5.62\ 10^{-7}$
R2	0.166659	-0.785711	3.39258	-0.542051	0.562105
R3	0.166659	0.642859	-1.69631	0.521027	-0.531055
R4	0.166659	0.642859	-1.69631	0.521027	-0.531055
R5	-0.166659	-0.642859	1.69631	-0.521027	0.531055
R6	0.166659	0.642859	-1.69631	0.521027	-0.531055
R7	$2.5\ 10^{-7}$	$2.5\ 10^{-7}$	0	$2.5\ 10^{-7}$	$-2.5\ 10^{-7}$
R8	0.166659	0.642859	-1.69631	0.521027	-0.531055
R9	-0.166659	-0.642859	1.69631	-0.521027	0.531055

Table 75: Element testability of leapfrog filter specifications

	$ET(h, t_s)$	$ET(h, t_{max})$	$ET(h, OS)$	$ET(h, t_r)$	$ET(h, f_L)$
R10	0.166659	-0.785711	3.39258	-0.542051	0.562105
R11	0.166659	0.642859	-1.69631	0.521027	-0.531055
R12	0.166659	0.642859	-1.69631	0.521027	-0.531055
C1	0.333322	-0.142869	1.69631	-0.0210374	0.0310647
C2	0.166659	0.642859	-1.69631	0.521027	-0.531055
C3	0.166659	0.642859	-1.69631	0.521027	-0.531055
C4	0.333322	-0.142869	1.69631	-0.0210374	0.0310647

The specifications that need to be measured in order to test the circuit elements are given in Table 76.

Table 76: Specifications to be measured

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	C1	C2	C3	C4
UN	*OS*	*OS*	*OS*	*OS*	*OS*	*UN*	*OS*	*OS*	*OS*	*OS*	*OS*	*OS*	*OS*	*OS*	*OS*

where UN indicates to that the element can not be tested (untestable elements).

Note that the circuit elements can be tested by selecting only the maximum overshoot OS% to improve the fault coverage.

The resistors R_1 and R_7 are untestable using the above specifications. However, they can be tested by computing the *DC* gain sensitivity with respect to the circuit elements as shown in Table 77.

Table 77: *DC* gain sensitivities

DC gain sensitivities with respect to the circuit elements											
R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
-1	10^{-6}	1	-10^{-6}	10^{-6}	0	-1	$-2\ 10^{-6}$	$2\ 10^{-6}$	$2\ 10^{-6}$	$-2\ 10^{-6}$	1

For fault diagnosis purpose, the ambiguity groups can be determined based on the algorithm proposed in Chapter 4 and they are given in Table 78.

Table 78: Ambiguity groups

Groups	1	2	3	4	5	6	7	8	9
Elements	R_3, R_4, R_6, C_2	R_8, R_{11}, R_{12}, C_3	R_1, R_7	R_2	C_4	R_9	C_1	R_5	R_{10}

6.4. Discussion

In this section, the difference between our method and the previous works will briefly be discussed.

The sensitivity analysis provides the relationship between the circuit elements and performance specifications. This kind of analysis ensures both the structural and functional test where the circuit elements are tested through verifying circuit functionality. In this sense, our method is similar to the proposed method in [Slma95, Slam96]. However, the sensitivity analysis is a function of frequency as well as being the goal of the test method for improving fault coverage by extracting the adequate frequency to test the circuit elements. Furthermore, this method does not consider the reduction of the test time and the fault identification problem. The fault observability concept is similar to our element testability concept. However, the observability provides the difficulty in testing the circuit elements as a function of frequency, whilst the element testability concept is independent of the frequency.

The authors in [Liu94, Fedi99, Pang01, Mane03] suggest an algorithm for determining the ambiguity groups, and the authors in [Sten87, Spaa96b] propose an algorithm for reducing the test cost by prediction of the circuit behavior. In contrast, our method can be employed for reducing the test cost without sacrificing fault coverage. Furthermore, for the fault diagnosis problem the ambiguity groups can be determined and specifications which can break them up can be selected for measuring. The previous works mentioned mostly consider the transfer function or the node voltages in the frequency domain for measuring. In contrast, our method can select specifications in both the time and the frequency domain to be measured.

6.5. Summary

In this chapter, the concept of element testability which reflects the difficulty in testing of the circuit elements for higher-order circuits was presented. Based on this concept, the circuit specifications that need to be measured can be selected in order to reduce the test cost by reducing the number of circuit specifications. The higher-order circuit is approximated by the second-order one, then the element testability can be obtained based on the pole sensitivities of the approximate second-order circuit which reflect the effect of the variations of the original circuit elements on the circuit specifications. For the fault identification problem, the ambiguity groups can be determined using the algorithm proposed in Chapter 4.

Chapter 7

Testability Analysis of Nonlinear Circuits

7.1. Introduction

In this chapter, we will extend the ambiguity groups determination and measurement selection algorithms proposed in the previous chapters for linear analog circuits to cover nonlinear analog circuits. The ambiguity groups determination algorithm for nonlinear circuits is also based on the sensitivities of the poles and zeros of the linearized circuit. The measurement selection algorithm is based on the testability of the parameters of the linearized circuits which can be obtained relying on the pole and zero sensitivities. This algorithm can be also employed to improve the fault coverage and to reduce the test cost by reducing the number of specifications that have to be measured.

The measurement selection algorithm proposed in [Milo94, Chao97] to improve the fault coverage and to reduce the test cost by reducing the number of the specifications that have to be measured. This algorithm does not provide the complete link between circuit specifications and the circuit parameters (functional test). Furthermore, the selected measurements can not be completely utilized for the fault identification problem. In contrast, our method provides the complete link between circuit specifications and circuit parameters. In other words, the circuit parameters are tested through checking the circuit specifications. Also, the ambiguity groups can be determined for fault diagnosis purpose.

7.2. Testability Analysis Algorithm

The algorithm of testability analysis for nonlinear circuits is shown in Figure 7-1.

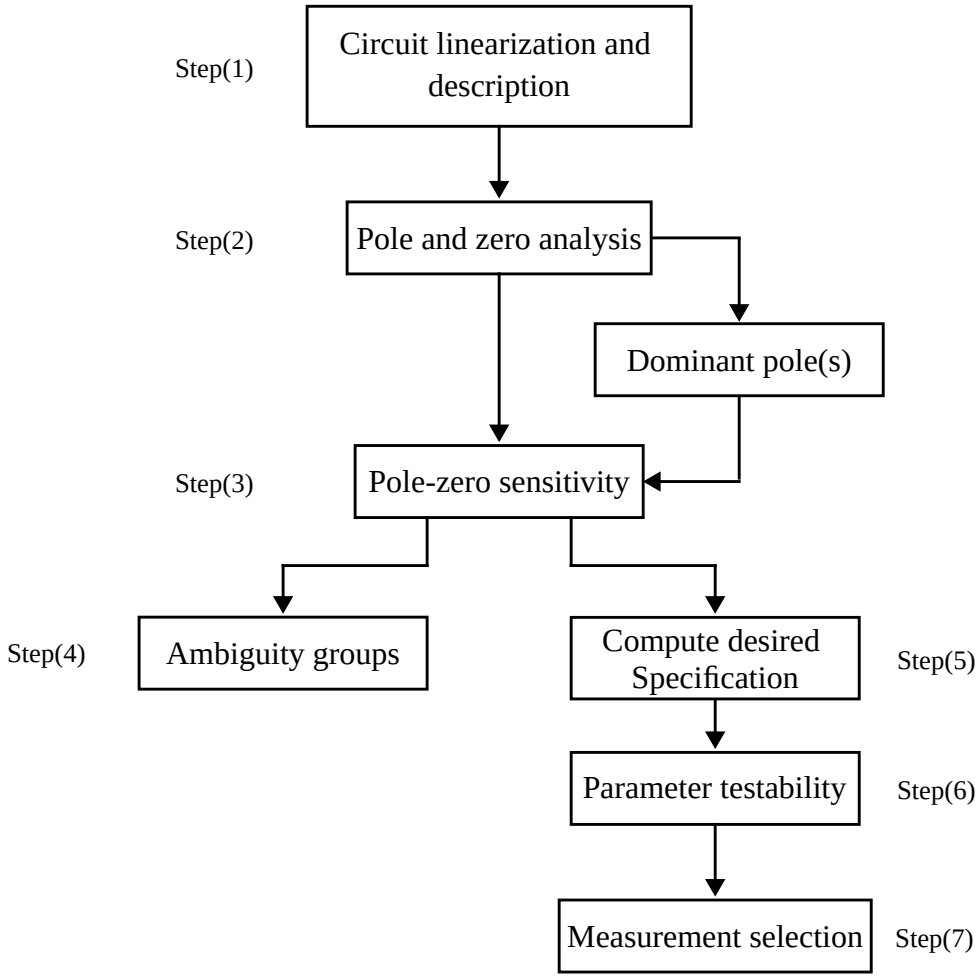


Figure 7-1: Testability analysis algorithm

In step 1, a nonlinear circuit is linearized around an operating point by replacing the nonlinear elements by their small-signal models. The linearized circuit is represented by its transfer function in the Laplace domain as a function of the complex frequency *s*.

In step 2, the pole and zero analysis is performed using the *QZ* algorithm (cf. Chapter 4). If the linearized circuit has a dominant pole, the effect of this pole is considered and effect of the other poles is neglected.

In step 3, the sensitivities of the poles and zeros are computed by utilizing symbolic analysis (cf. Chapter 2).

In step 4, the ambiguity groups is determined based on the pole-zero sensitivities.

In step 5, specifications that can be computed relying on the poles and zeros of the transfer function are determined. In this chapter, we will only consider the frequency-domain specifications. However, the time-domain specifications can be used in the similar manner.

In step 6, the parameter testability of the circuit parameters with respect to the circuit specifications is computed. In this chapter, the term *parameter* instead of the term *element* is used. Because the linearized circuit includes the elements such as resistor and capacitors as well as the parameters such as β (the forward gain current for BJT transistors) and g_m (the transconductance for MOSFET transistors). The term parameter is more general than the term element, it can mean the circuit elements or other circuit parameters.

In step 7, the specifications that correspond to the maximum parameter testability are selected to be measured in order to test the circuit parameters.

7.2.1. Circuit Linearization and Description

A linearized analog circuit will be represented in the *s*-domain. In the *s*-domain analysis a capacitance *C* is replaced by an admittance *sC*, and an inductance *L* is replaced by an impedance *sL*. The nonlinear devices such as diods and transistors are replaced by their small-signal models. The *DC* analysis is required for determining the operating point of the circuit and for computing the parameters of the small-signal models at the operating point. The equations of the linearized circuit are expressed in matrix form using modified nodal analysis as

$$[Y][x] = [b] \tag{7-1}$$

where *Y* is the admittance matrix, *x* is the vector of circuit variables (voltages or currents), and *b* is the source vector.

According to the Cramer's rule, the transfer function can be expressed as the ratio of the determinant $\Delta(s)$ and some cofactors $\Delta_{ij}(s)$ of the modified nodal matrix and given as

$$H(s)= \frac{\Delta_{ij}(s)}{\Delta(s)}= \frac{a_0 + a_1 s + a_2 s + \ldots + a_m s^m}{b_0 + b_1 s + b_2 s + \ldots + b_n s^n} \qquad m < n \tag{7-2}$$

Or the transfer function can be expressed in pole-zero form as

$$H(s) = \frac{N(s)}{D(s)} = A_m \frac{(s-z_1)(s-z_2)\ldots(s-z_m)}{(s-p_1)(s-p_2)\ldots(s-p_n)} = A_m \frac{\prod_{i=1}^{m}(s-z_i)}{\prod_{i=1}^{n}(s-p_i)} \tag{7-3}$$

where n and m are the number of the poles and zeros, respectively, and the A_m is equal to the ratio of the coefficients a_m / b_n (A_m is called *the midband gain* for amplifier circuits [Sed98]).

7.2.2. Pole and Zero Analysis

The poles and zeros of the system are computed by invoking the *QZ* algorithm as discussed in Chapter 4.

The locations of the poles of the transfer function in the *s*-plane greatly affect the frequency and transient responses of the system. Therefore, it is important to sort out the poles that have a dominant effect on the frequency and transient responses; these poles are called *dominant poles* [Kuo95]. As a result, the behavior of higher-order systems can be approximated by lower-order ones by considering only the effect of the dominant poles and neglecting the effect of the other poles. As a rule of thumb, the dominant pole is determined if this pole is separated from the nearest pole by at least two octaves (that is, a factor of four) [Sedr98].

7.2.3. Pole and Zero Sensitivity

In this chapter, we will employ the symbolic analysis (cf. Chapter 2). The simplification techniques such as simplification before generation or simplification after generation [Half03], which are used for symbolic analysis, can be utilized in order to generate an approximate transfer function. The poles of the approximate transfer function can be obtained symbolically by solving the denominator polynomial of the approximate transfer function with respect to the complex frequency s (i.e. finding the roots of the denominator polynomial) [Anal01, Somm03] or by exploiting the symbolic pole/zero approximation [Henn98]. The zeros of the approximate transfer function can be obtained by finding the roots of the nominator polynomial. The normalized differential sensitivities of the poles and zeros can be computed by applying these equations:

$$S_h^z = \frac{h}{z}\frac{\partial z}{\partial h} \tag{7-4}$$

$$S_h^p = \frac{h}{z}\frac{\partial p}{\partial h} \tag{7-5}$$

If the pole is given by the real and imaginary parts $p = \sigma + j\omega$, the normalized sensitivity becomes (the same formula is valid for the sensitivity of zeros of the transfer function))

$$S_h^p = \frac{h}{\sigma}\frac{\partial \sigma}{\partial h} + j \cdot \frac{h}{w}\frac{\partial \omega}{\partial h} = S_h^\sigma + j \cdot S_h^\omega \tag{7-6}$$

7.2.4. Ambiguity Groups

The ambiguity group is defined as the groups of circuits element which cannot be distinguished from each other by measurements made at the designed test nodes and test conditions [Dai90]. The ambiguity groups can be determined as follows:

If the pole and zero sensitivities with respect to the parameter h_1 are the same as the pole and zero sensitivities with respect to the parameter h_2, leading that the parameter h_1 and parameter h_2 to belong to the same ambiguity group.

Mathematically, the parameters h_1 and h_2 belong to the same the ambiguity group if

$$S_{h_1}^{p_i} = S_{h_2}^{p_i} \qquad S_{h_1}^{z_j} = S_{h_2}^{z_j} \tag{7-7}$$

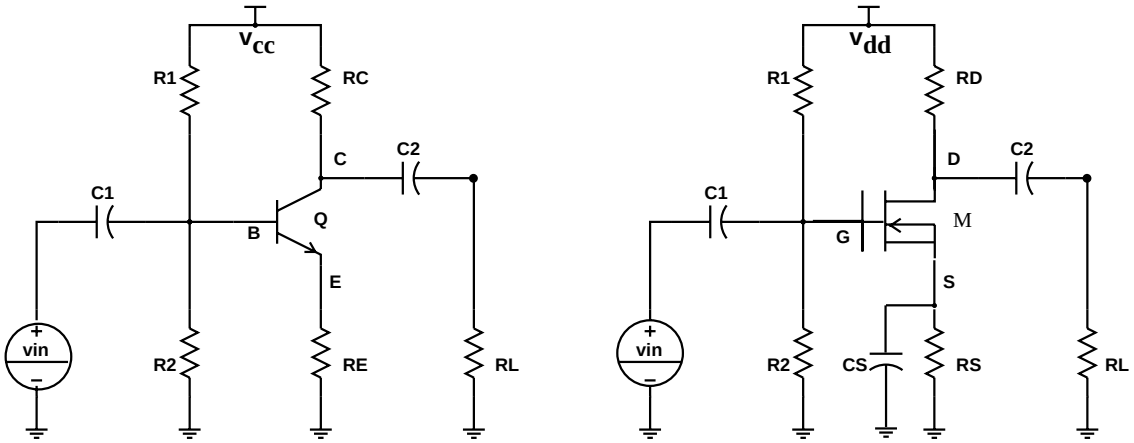
where $i = 1, 2,..., n$ and $j = 1,2,..., m$.
The ambiguity group can be generalized if the sensitivity of the midband gain A_M is taken into account. In this way, the frequency response is fully considered. The sensitivity of midband gain A_M with respect to the circuit parameters can be computed by analyzing the linearized circuit with the assumption that no storage elements in midband region is considered. The ambiguity groups associated to the midband gain A_M are determined as follows:

If the midband gain sensitivities with respect to the parameter h_1 is the same as the midband gain sensitivities with respect to the parameter h_2, leading the parameter h_1 and parameter h_2 to belong to the same ambiguity group.

The total ambiguity groups can be mathematically determined by the intersection of the pole-zero ambiguity groups and midband ambiguity groups.

7.2.5. Frequency-Domain Specifications

In this section we will discuss the frequency-domain specifications of the amplifier circuits as described in [Sedr98], a simple examples for amplifier circuits are shown in Figure 7-2.



(a) BJT common-emitter amplifier (b) MOSFET common-source amplifier

Figure 7-2: Simple examples for amplifier circuits

The transfer function of the linearized circuit as a function of the complex frequency *s* can be expressed in the general form as (band-pass function)

$$A(s) = A_M H_{LF}(s) H_{HF}(s) \tag{7-8}$$

where A_M is the midband gain, $H_{LF}(s)$ is the low-pass response with the low cutoff frequency ω_L, and $H_{HF}(s)$ is the high-pass response with the high cutoff frequency ω_H. The ω_L and ω_H are the frequencies at which the magnitude drops by 3 dB below the midband value as shown in Figure 7-3. The bandwidth is defined as $BW = \omega_H - \omega_L$. For frequencies ω much greater than ω_L the function $H_{LF}(s)$ approaches to unity. Similarly, for frequencies ω much smaller than ω_H the function $H_{HF}(s)$ approaches to unity. Thus, for $\omega_L << \omega << \omega_H$ the transfer function becomes

$$A(s) = A_M \tag{7-9}$$

The midband gain A_M is determined by analyzing the equivalent circuit (linearized circuit) with the assumption that the external capacitors (e.g. the coupling and bypass capacitors in amplifier circuits) are acting as short circuits and the internal capacitors of the transistor model are acting as open circuits. The midband gain A_M can be computed from the transfer function by approaching the complex frequency *s* to infinity.

$$A_M = A(s)\big|_{s \to \infty} \tag{7-10}$$

The low-frequency and high-frequency transfer functions can be expressed as

$$A_L(s) \approx A_M H_{LF}(s) \tag{7-11}$$

$$A_H(s) \approx A_M H_{HF}(s) \tag{7-12}$$

The low-frequency transfer function $A_L(s)$ is determined by analyzing the linearized circuit including the external capacitors (e.g. the coupling and bypass capacitors in amplifier circuits) but assuming that the transistor-model capacitors behave as perfect open circuits. On the other hand, the high-frequency transfer function $A_H(s)$ is determined by analyzing the linearized circuit including the transistor-model capacitors but assuming the external capacitors behave as perfect short circuits.

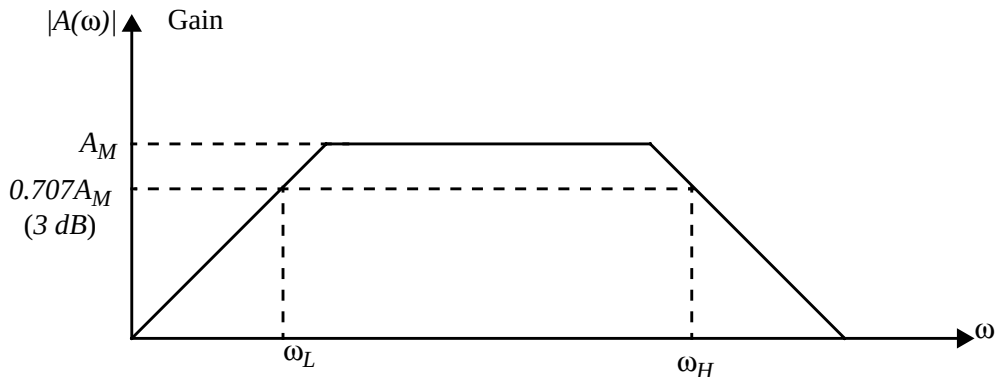


Figure 7-3: Furnace response of the linearized nonlinear circuit

7.2.5.1. The Low-Frequency Response

The low-frequency transfer function can be expressed in general form as

$$H_{LF}(\omega) = \frac{(j\omega + \omega_{z_1})(j\omega + \omega_{z_2})\ldots(j\omega + \omega_{z_n})}{(j\omega + \omega_{p_1})(j\omega + \omega_{p_2})\ldots(j\omega + \omega_{p_n})} \tag{7-13}$$

where ω_{p1}, ω_{p2},..., ω_{pn} are the low-frequency poles and ω_{z1}, ω_{z2},..., ω_{zn} are the low-frequency zeros. The low-frequency transfer function $H_{LF}(s)$ approaches to unity as s approaches to infinity, thus $A_L(s) \cong A_M$.

If the ω_{p1} is much higher than the all other low poles ($\omega_{p1} >> \omega_{p2}$,..., ω_{pn}, ω_{z1}, ω_{z2},..., ω_{zn}), the low-frequency transfer function can be approximated by

$$H_{LF}(\omega) \approx \frac{j\omega}{j\omega + \omega_{p_1}} \tag{7-14}$$

where ω_{p1} is the dominant low-frequency pole. $H_{LF}(s)$ is the transfer function of a first-order high-pass network.

In this case the low-frequency response is dominated by the low-frequency pole at $s = \omega_{p1}$ and the low-cutoff frequency (lower 3-dB frequency) is approximated by

$$\omega_L \approx \omega_{p_{1L}} \tag{7-15}$$

If a dominant low-frequency pole does not exist, an approximate formula can be driven for ω_L in terms of the poles and zeros and given [Sedr98].

$$\omega_L \approx \sqrt{\sum_{i=1}^{pn} \omega_{p_i}^2 - 2\sum_{i=1}^{zn} \omega_{z_i}^2} \tag{7-16}$$

7.2.5.2. The High-Frequency Response

The high-frequency transfer function can be expressed in general form as

$$H_{HF}(\omega) = \frac{\left(1 + \frac{j\omega}{\omega_{z_1}}\right)\left(1 + \frac{j\omega}{\omega_{z_2}}\right)\ldots\left(1 + \frac{j\omega}{\omega_{z_n}}\right)}{\left(1 + \frac{j\omega}{\omega_{p_1}}\right)\left(1 + \frac{j\omega}{\omega_{p_2}}\right)\ldots\left(1 + \frac{j\omega}{\omega_{p_n}}\right)} \tag{7-17}$$

where ω_{p1}, ω_{p2},..., ω_{pn} are the high-frequency poles and ω_{z1}, ω_{z2},..., ω_{zn} are the high-frequency zeros. The high-frequency transfer function $H_{HF}(s)$ approaches to unity as the complex frequency s approaches to infinity, thus $A_H(s) \cong A_M$.

If the ω_{p1} is much lower than the all other high poles ($\omega_{p1} << \omega_{p2},..., \omega_{pn}, \omega_{z1}, \omega_{z2},..., \omega_{zn}$), the low-frequency transfer function can be approximated by

$$H_{HF}(\omega) \approx \frac{1}{1 + \frac{j\omega}{\omega_{p_1}}} \tag{7-18}$$

where ω_{p1} is the dominant high-frequency pole. $H_{LF}(s)$ is the transfer function of a first-order low-pass network.

In this case the high-frequency response is dominated by the high-frequency pole at $s = \omega_{p1}$ and the high-cutoff frequency (upper 3-dB frequency) is approximated by

$$\omega_H \approx \omega_{p_1} \tag{7-19}$$

If a dominant low-frequency pole does not exist, an approximate formula can be driven for ω_H in terms of the poles and zeros and given [Sedr98]

$$\omega_H \approx \frac{1}{\sqrt{\sum_{i=1}^{pn} \frac{1}{\omega_{p_i}^2} - 2\sum_{i=1}^{zn} \frac{1}{\omega_{z_i}^2}}} \tag{7-20}$$

7.2.6. Parameter Testability and Measurement Selection

Parameter testability is defined as the relative degree of difficulty in testing a circuit parameter *h* with respect to a specification *SP*. Parameter testability also provides the information about the effect of the circuit parameters on the circuit specifications. Mathematically, the parameter testability can be expressed as:

$$PT(h, SP) = S_h^{SP} \tag{7-21}$$

The sensitivity of low-cutoff frequency is approximately equal to the sensitivity of the dominant low-frequency pole ω_{pL}

$$S_x^{\omega_L} \approx S_x^{\omega_{p_L}} \tag{7-22}$$

If the circuit has no dominant pole, the sensitivity of the low-cutoff frequency can be computed based on Eq. (7-20) and first-order sensitivity properties given in Appendix A as follows:

$$S_x^{\omega_L} = \frac{1}{\omega_L^2}\sum_{i=1}^{pn} \omega_{p_i}^2 \, S_x^{\omega_{p_i}} - \frac{2}{\omega_L^2}\sum_{i=1}^{zn} \omega_{z_i}^2 \cdot S_x^{\omega_{z_i}} \tag{7-23}$$

The sensitivity of high-cutoff frequency is approximately equal to the sensitivity of the dominant high-frequency pole ω_{pH}

$$S_x^{\omega_H} \approx S_x^{\omega_{p_H}} \tag{7-24}$$

or

$$S_x^{\omega_H} \approx \frac{1}{\omega_H^2}\sum_{i=1}^{pn} \frac{1}{\omega_{p_i}^2} S_x^{\omega_{p_i}} - \frac{2}{\omega_H^2}\sum_{i=1}^{zn} \frac{1}{\omega_{z_i}^2} \cdot S_x^{\omega_{z_i}} \tag{7-25}$$

The parameter testability *PT(h, SP)* can be expressed for linearized circuits for small parameter deviation (small Δh) as a function of the relative deviation of a specification *SP* and a relative deviation of the circuit parameter *h* as:

$$PT(h, SP) = \frac{\frac{\Delta SP}{SP}}{\frac{\Delta h}{h}} \tag{7-26}$$

However, as mentioned in Chapter 5, the computational cost is very high.

The specifications that have to be measured in order to test the parameter *h* is selected corresponding to the maximum absolute value of the parameter testability values

$$SP|_h = max(|PT(h, SP)|) \tag{7-27}$$

7.3. Simulation Examples

For the first and the second examples the sensitivities of the poles and zeros of the transfer function can be obtained using symbolic analysis. However, it is not possible to obtain the poles and zeros sensitivities for the μA741 operation amplifier using the symbolic analysis. Therefore, the approximation technique is used to obtain the symbolic form of the dominant pole of the μA741 operation amplifier.

7.3.1. The Simple Common-Emitter Amplifier

The schematic of the common-emitter amplifier is shown in Figure 7-4 [Sed98].

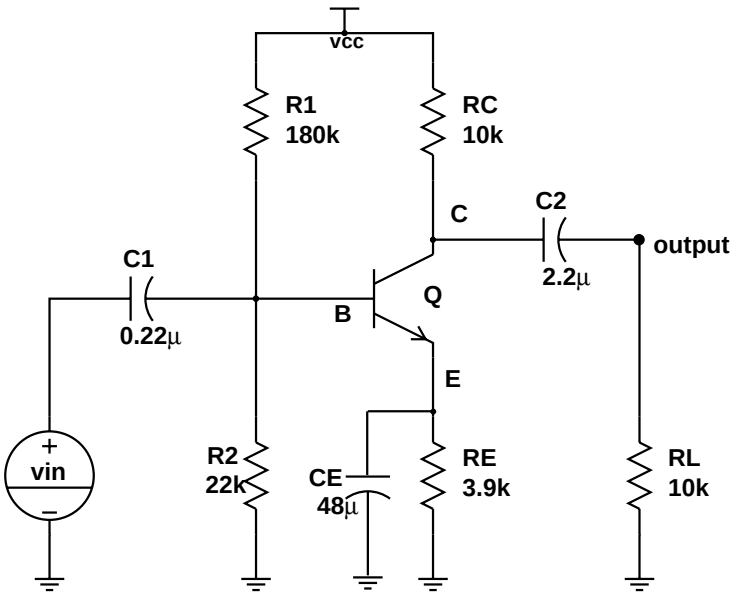


Figure 7-4: The schematic of the common-emitter amplifier

The small-signal transistor model is shown in Figure 7-5.

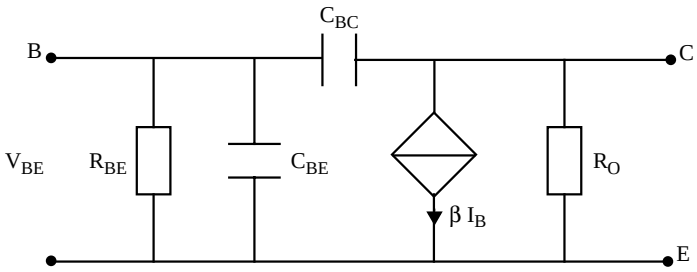


Figure 7-5: Simple small-signal model for BJT

The frequency response of the common-emitter amplifier is shown in Figure 7-6 (without considering the effect of the internal capacitors).

.

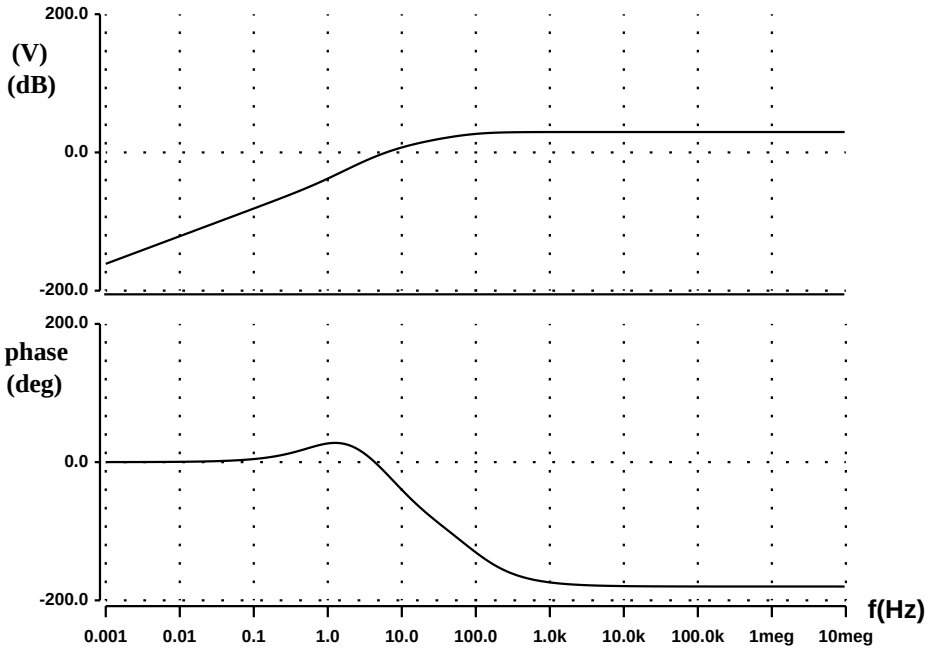


Figure 7-6: The frequency response of the common-emitter amplifier

The poles, zeros and midband gain of the common-emitter amplifies are given in Table 79.

Table 79: The poles zeros and midband gain of the common-emitter amplifier

P_1	P_2	P_3	P_4	Z_1	A_M
-452.206	-76.0989	-22.7273	$-6\ 10^7$	-5.34188	35.0655 dB

The low-frequency dominant pole is $\omega_L \cong P_1 = 452.206$ (the absolute value of dominant pole P_1), the low-cutoff frequency can be obtain $f_L = 71.9708$ Hz. The high-frequency dominant pole is $\omega_H \cong P_4 = 6\ 10^7$, the high-cutoff frequency is $f_H = 9.54929\ 10^6$ Hz.

The sensitivities of the poles, zero and midband gain with respect to the circuit parameters are given in Table 80.

Table 80: The sensitivities of the poles, zero and midband gain

	$S^{p_1}{}_h$	$S^{p_2}{}_h$	$S^{p_3}{}_h$	$S^{p_4}{}_h$	$S^{Z}{}_h$	$S^{A_M}{}_h$
R_1	-0.0456239	-0.0607254	0	0	0	0
R_2	-0.373287	-0.496844	0	0	0	0
R_C	0	0	-0.5	-0.333333	0	0.5
R_E	-0.00216173	-0.0573508	0	0	-1	0
R_L	0	0	-0.5	-0.333333	0	0.5
C_1	-0.817003	-0.182997	0	--	0	--
C_2	0	0	-1	--	0	--
C_E	-0.182997	-0.817003	0	--	-1	--
β	0.179935	0.755873	0	0	0	1
R_{BE}	-0.578928	-0.38508	0	0	0	-1
C_{BE}	--	--	--	0	0	--
C_{BC}	--	--	--	-1	0	--
R_O	0	0	0	-0.333333	0	0

where (--) denotes that the capacitor is not considered.

We must note that the internal capacitors are not considered by the low frequency analysis, therefore, they have no effect on the low-cutoff frequency. On the other hand, the external capacitors have no effect on the high-cutoff frequency.

The ambiguity group according to the dominant low-frequency pole is $\{R_C, R_L, R_O, C_2\}$ (by applying a low-frequency input signal) (cf. Section 7.2.4.). The testable parameters are $\{R_1, R_2, R_E, C_1, C_E, \beta, R_{BE}\}$.

The ambiguity groups according to the dominant high-frequency pole are $\{R_1, R_2, R_E, \beta, R_{BE}, C_{BE}\}$, $\{R_C, R_L, R_O\}$ (by applying a high-frequency input signal).

The ambiguity groups according to the zero are {R_E, C_E}, {R_1, R_2, R_C, R_L, R_B, C_1, C_2, β}.

The ambiguity groups according to the A_M are {R_1, R_2, R_E}, {R_C, R_L}.

The total ambiguity groups is {R_C, R_L,}

Untestable parameters are C_{BE} and C_2.

The parameter testability of the circuit parameters with respect to the low-cutoff frequency, high-cutoff frequency and midband gain is given in Table 81.

Table 81: The parameter testability

	$PT(h, f_L)$	$PT(h, f_H)$	$PT(h, A_M)$
R_1	-0.0456239	0	0
R_2	-0.373287	0	0
R_C	0	-0.333333	0.5
R_E	-0.00216173	0	0
R_L	0	-0.333333	0.5
C_1	-0.817003	0	0
C_2	0	0	0
C_E	-0.182997	0	0
β	0.179935	0	1
R_{BE}	-0.578928	0	-1
C_{BE}	0	0	0
C_{BC}	0	-1	0
R_O	0	-0.333333	0

The specifications to be measured for testing the circuit parameters are given in Table 82.

Table 82: The specifications to be measured

R_1	R_2	R_C	R_E	R_L	C_1	C_2	C_E	β	R_{BE}	C_{BE}	C_{BC}	R_O
f_L	f_L	A_M	f_L	A_M	f_L	UN	f_L	A_M	A_M	UN	f_H	f_H

where UN indicates to that the parameter can not be tested (untestable parameters) considering the above specifications.

The relative deviation of the low-cutoff frequency, high-cutoff frequency and midband gain are computed using Saber simulator [Anal97] and given in Table 83 ($\Delta h/h = 0.1$)

Table 83: The relative deviation of the f_L, f_H, and A_M

	f_L	$\Delta f_L/f_L$	f_H	$\Delta f_H/f_H$	A_M	$\Delta A_M/A_M$
nominal	73.0723	0	$9.54929\ 10^6$	0	-33.3333	0
R_1 +10%	72.7675	-0.00417121	$9.54929\ 10^6$	0	-33.3333	0
R_2 +10%	70.5953	-0.0338983	$9.54929\ 10^6$	0	-33.3333	0
R_C +10%	73.064	-0.000113912	$9.2599\ 10^6$	-0.0303	-34.9206	0.05
R_E +10%	73.048	-0.000333368	$9.54929\ 10^6$	0	-33.3333	0
R_L +10%	73.064	-0.000113912	$9.2599\ 10^6$	-0.0303	-34.9206	0.05
C_1 +10%	67.7939	-0.0722354	0	0	0	0
C_2 +10%	73.0568	-0.000212657	0	0	0	0
C_E +10%	71.911	-0.015893	$9.54929\ 10^6$	0	-33.3333	0
β +10%	74.5187	0.0197933	$9.54929\ 10^6$	0	-36.6667	0.1
R_{BE} +10%	69.2951	-0.0516916	$9.54929\ 10^6$	0	-30.303	-0.1
C_{BE} +10%	0	0	$9.54929\ 10^6$	0	0	0
C_{BC} +10%	0	0	$-8.68118\ 10^6$	-0.0909	0	0
R_O +10%	0	0	$9.2599\ 10^6$	-0.0303	0	0

The parameter testability of the circuit parameters computed by Eq. (7-26) is given in Table 84. Clearly, the results in Table 84 are close to the results in Table 81.

Table 84: The element testability computed using Eq. (7-26)

	$PT(h, f_L)$	$PT(h, f_H)$	$PT(h, A_M)$
R_1 +10%	-0.0417121	0	0
R_2 +10%	-0.338983	0	0
R_C +10%	-0.00113912	-0.303	0.5
R_E +10%	-0.000333368	0	0
R_L +10%	-0.00113912	-0.303	0.5
C_1 +10%	-0.722354	0	0
C_2 +10%	-0.00212657	0	0

Table 84: The element testability computed using Eq. (7-26)

	PT(h, f_L)	*PT(h, f_H)*	*PT(h, A_M)*
C_E +10%	-0.15893	0	0
β +10%	0.197933	0	1
R_{BE} +10%	-0.516916	0	-1
C_{BE} +10%	0	0	0
C_{BC} +10%	0	-0.909	0
R_O +10%	0	-0.303	0

7.3.2. The CMOS Differential Amplifier

The schematic of the single-ended CMOS differential amplifier is shown in Figure 7-7.

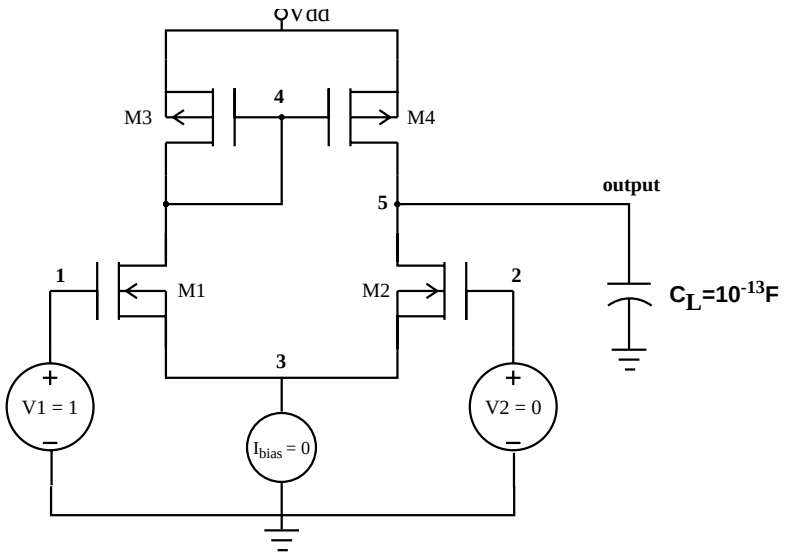


Figure 7-7: The schematic of the single-ended CMOS differential amplifier [Ana01]

The transistor model which is used for the differential amplifier is given in Figure 7-8.

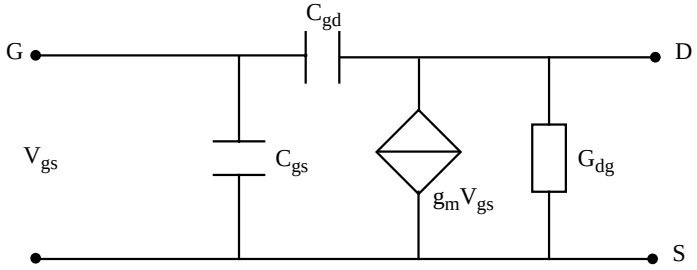


Figure 7-8: The transistor model of the differential amplifier

The poles of the differential amplifier are given in Table 85.

Table 85: The poles of the differential amplifier

P_1	P_2	P_3
-4.947422 10^6	-1.27509 10^8	-2.22303 10^8

The high-frequency ω_H is approximately equal to the dominant pole P_1 (a high-pass response). The pole sensitivities are given in Table 86.

Table 86: The pole sensitivities

	$S^{P1}{}_h$	$S^{P2}{}_h$	$S^{P1}{}_h$
GdsM1	0.0009105	0.00554056	-0.00160714
CgdM1	-0.000129784	-0.00136369	-0.0622911
CgsM1	0.0000576776	-0.484706	-0.0153517
gmM1	0.141887	0.483205	0.00813672
GdsM2	0.278479	0.012066	-0.0142175
CgdM2	-0.180272	-0.00314871	-0.0419516
CgsM2	0.0000576776	-0.484706	-0.0153517
gmM2	-0.142002	0.481335	0.0224124
GdsM3	0.000517439	0.000121001	0.00963608
CgdM3	0	0	0
CgsM3	-0.000901998	-0.00947766	-0.432923
gmM3	0.0428903	0.0100297	0.798732
GdsM4	0.71873	0.000279386	0.00648967
CgdM4	0.36723	0.000751493	0.105671
CgsM4	-0.000901998	-0.00947766	-0.432923
gmM4	-0.0414128	0.00742257	0.170418
CL	-0.450679	-0.00787178	-0.104879

The parameter testability of the differential amplifier parameters with respect to the high-frequency dominant pole ω_L and *DC* gain are given in Table 87.

Table 87: The element testability with respect to the ω_H and *DC* gain

	PT(h, ω_H*)*	*PT(h, DC* gain)
GdsM1	0.0009105	-0.00484391

Table 87: The element testability with respect to the ω_H and *DC* gain

	PT(h, ω_H)	*PT(h, DC* gain)
CgdM1	-0.000129784	N
CgsM1	0.0000576776	N
gmM1	0.141887	0.366771
GdsM2	0.278479	-0.271303
CgdM2	-0.180272	N
CgsM2	0.0000576776	N
gmM2	-0.142002	0.633229
GdsM3	0.000517439	-0.00427858
CgdM3	0	N
CgsM3	-0.000901998	N
gmM3	0.0428903	-0.35465
GdsM4	0.71873	-0.725499
CgdM4	0.36723	N
CgsM4	-0.000901998	N
gmM4	-0.0414128	0.360575
CL	-0.450679	N

where N indicates to that the parameter is not considered for this specification.

The ambiguity group according to the high-frequency ω_H is {GdsM1, CgdM1, CgsM1, CgsM2, CgsM3, GdsM3, CgsM4}. Note that the parameters in this group are not testable since their effect on the high-frequency ω_H is neglected.

The ambiguity groups according to the *DC* gain are {GdsM1, GdsM3} and {gmM1, gmM4} (the capacitors are not considered).

The selected specifications to be measured to test the capacitor C_L and small-signal parameters of the differential amplifier are given in Table 88.

Table 88: The selected specifications

GdsM4	CL	CgdM4	GdsM2	CgdM2	gmM1	gmM2	gmM3	gmM4
$\omega_{H,}$ *DC gain*	ω_H	ω_H	ω_H, *DC gain*	ω_H	*DC gain*	*DC gain*	*DC gain*	*DC gain*

The other parameters are not testable with respect to the high-frequency dominant pole and *DC* gain because their effect on the above specification can be neglected. Note that the transistor M3 is difficult to test it considering the high-cutoff frequency and *DC* gain due to the low values of their parameter testability.

The symbolic formula of the approximate pole of the differential amplifier can be obtained using the combination of the simplification before generation SBG and simplification after generation (SAG). This formula is given in [Ana01] and can be rewritten as

$$p = \frac{GdsM4 \cdot gmM3(gmM1 + gmM2) + GdsM2 \cdot gmM1(gmM3 + gmM4)}{(gmM1 + gmM2)(CgdM2 \cdot gmM3 + CL \cdot gmM3 + CgdM4(gmM3 + gmM4))}$$

The sensitivities of the approximate pole with respect to the capacitor C_L and small-signal parameters of the differential amplifier is given in Table 89. The results in Table 89 are very close to the results in Table 87.

Table 89: The sensitivities of the approximate pole

	CgdM2	CgdM4	CL	GdsM2	GdsM4	gmM1	gmM2	gmM3	gmM4
Sens.	-0.181	-0.363	-0.454	0.2761	0.7238	0.138	-0.138	0.0437	-0.043

7.3.3. The Operation Amplifier μA741

The schematic of the μA741 operation amplifier is shown in Figure 7-9 [Anal01].

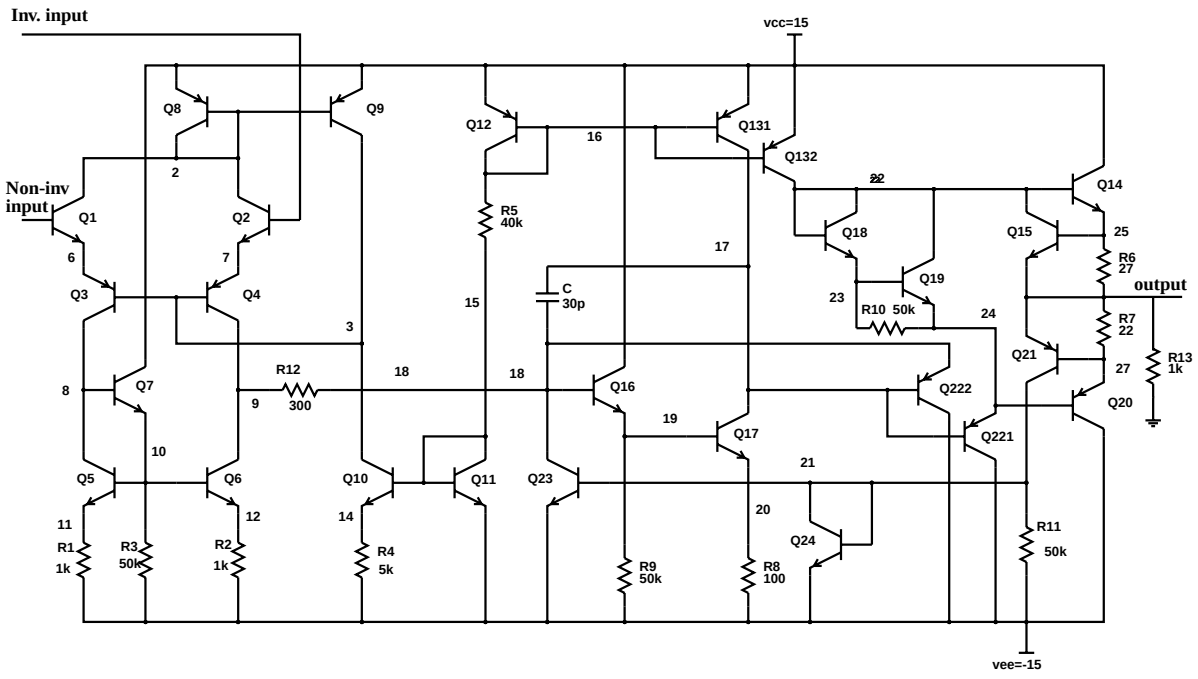


Figure 7-9: The schematic of the μA741 operation amplifier

The small-signal transistor mode is shown in Figure 7-8 [Anal01].

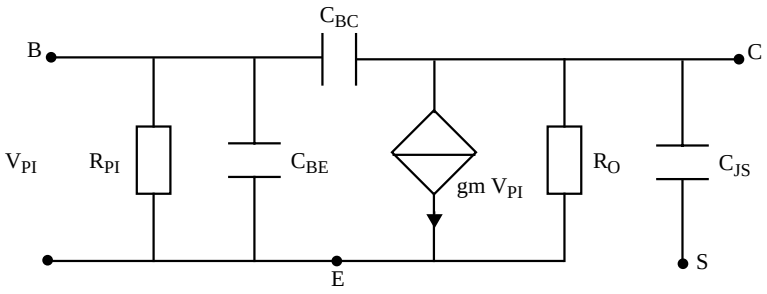


Figure 7-8: Simple small-signal model for BJT's

The symbolic formula of the low-cutoff frequency is given

$$p = \frac{(RoQ131 + RoQ17)(gmQ17R8RoQ4RpiQ17 + R9(RoQ4 + gmQ16gmQ17R8RpiQ16RpiQ17))}{C1gmQ16gmQ17R9RoQ131RoQ17RoQ4RpiQ16RpiQ17}$$

The parameter testability with respect to the low-cutoff frequency and *DC* gain is given in Table 90.

Table 90: Parameter testability w.r.t. low-cutoff frequency and DC gain

parameter	*PT(h, ω_L)*	*PT(h, DC gain)*
R8	0.512703	-0.512703
R9	-0.211975	0.211975
C1	-1	--
gmQ16	-0.699273	0.699273
gmQ17	-0.487297	0.487297
RoQ4	-0.300727	0.300727
RoQ131	-0.712589	0.712589
RoQ17	-0.287411	0.287411
RpiQ16	-0.699273	0.699273
RpiQ17	-0.487297	0.487297
gmQ2	--	0.497409
gmQ4	--	0.502591

The ambiguity groups according to the low-cutoff frequency are {gmQ16, RpiQ16} and {gmQ17, RpiQ17}. In other words, the parametric faults in the transistor Q16 and the transis-

tor Q17 can not be distinguished. The ambiguity groups according to the *DC* gain is {R13, gmQ14}. The rest of the circuit parameters are not testable with considering the low-cutoff frequency and the *DC* gain. Some testability parameters values of the low-cutoff frequency and the DC gain are close to each others (absolute value). This can be interpreted as being due to the low value of the low-cutoff frequency (3.1 Hz). The measurements that have to be performed in order to test the above parameters can be selected according to the maximum values of the parameter testability.

Further measurements have to be performed for testing other parameters. For example by measuring the DC voltage across the resistor R4 (assuming it is accessible), the parameters (gmQ1, gmQ2, gmQ3, gmQ4, gmRoQ10, gmQ10) can be tested.

7.4. Summary

In this chapter, the ambiguity groups and the measurement selection of the nonlinear circuits that can be linearized were discussed. The ambiguity groups are determined based on the pole and zero sensitivities. If the variations of two parameters affect the poles and zeros of the transfer function in the same way, this means these parameters belong to the same ambiguity groups.

The measurement selection is based on the parameter testability concept. The parameter testability is calculated based on the pole sensitivities with respect to the circuit parameters. In our examples, the dominant pole case was discussed. If the circuit has no dominant pole, the approximation techniques such as AWE (cf. Chapter 6) or symbolic simplification techniques [Anal01] for linearized circuits can be utilized.

Our algorithm can be utilized to reduce test time without sacrificing fault coverage, and to provide maximum information for fault identification.

Chapter 8

Conclusion

In this thesis we have presented a methodology for the testability analysis and the measurement selection for linear and linearized analog circuits. This methodology is based on the well-known pole and zero analysis and their sensitivities. Parametric faults which are difficult to be tested and detected are considered in this thesis.

In the fault diagnosis two phases can be considered: the first one is the phase of the testability analysis, while the second one is the phase of fault location. The testability analysis gives prior information about the degree of solvability of the fault diagnosis problem. Such information includes the number of testable and nontestable elements of a circuit, ambiguity groups, and nodes to be tested. The degree of the solvability of the fault diagnosis problem can be quantified by the testability measure concept. The testability measure is mathematically evaluated by the maximum number of linearly independent columns of the Jacobian matrix which is constructed by the derivative of the circuit performances with respect to the circuit elements. If the rank of the Jacobian matrix is equal to the number of circuit elements, this indicates that all faults in circuit elements can be identified. Otherwise, additional test nodes must be added or the number of testable elements must be reduced to be equal to the rank of the matrix. Such circuits are called low testability circuits. In low testability circuits, the testability analysis is strictly tied to the ambiguity group concept. The ambiguity groups consist of circuit elements that produce the same value of measurements. These elements can be determined by the linearly dependent columns of the Jacobian matrix.

In this thesis, a novel algorithm for the testability measure and the ambiguity groups determination was proposed in Chapter 4. This algorithm is based on the pole and zero analysis and the pole-zero sensitivity analysis. Unlike the other methods that depend on numerical methods such as QR factorization or SVD decomposition.

We have shown that the testability measure (the number of the testable elements of a circuit) is related to the number of the poles and zeros of the transfer function at a certain node as well as to the *DC* gain at this node. Furthermore, the relationship between the testability measure, which is computed based on pole and zero analysis, and controllability/observability concepts from control theory is discussed. The controllable (or noncontrollable) and observable (or nonobservable) states which are represented by voltages or currents of storage elements (capacitors and inductors) in linear analog circuits can be determined using pole-zero sensitivity analysis.

In our method, the ambiguity groups can easily be determined based on the pole and zero sensitivities as well as on the DC gain sensitivities, unlike the numerical methods by which the ambiguity groups are determined by the linearly dependent columns of the testability matrix (Jacobian matrix) using QR factorization or SVD decomposition.

Thus, our method presents a new definition of the ambiguity groups based on circuit theory. The ambiguity group can be defined as a group of circuit elements which affect the poles and zeros as well as the *DC* gain of a circuit in the same way.

Analog circuits have a large number of specifications to be checked in order to ensure circuit functionality. However, checking all specifications can result in a very long test time. Therefore, a subset of specifications is selected to be measured. This subset of specifications must ensure that it reduces test time without sacrificing fault coverage and maximizes the information for fault identification in the fault diagnosis problem.

In this thesis, a test method for measurement selection for linear circuits was proposed in Chapter 5 and Chapter 6. The measurement selection algorithm depends on the element testability concept. The element testability provides an insight into the difficulty in testing circuit elements as well as the effect of circuit element variations on circuit specifications. The element testability can easily be obtained based on the pole and zero sensitivities.

A measurement selection algorithm for second-order circuits is considered in Chapter 5. Specifications that need to be measured can be selected in the frequency-domain or in the time-domain because these specifications are related to the poles and zeros of a circuit which can

represent the time and frequency response. A measurement selection algorithm for higher-order circuits which can be approximated by second-order ones was presented in Chapter 6. The approximation of higher-order circuits by second-order ones is carried out by using a model-order reduction technique. The asymptotic waveform evaluation (AWE) moment matching as a method of model-order reduction is employed to extract a small set of dominant poles (a pair of complex-conjugate dominant poles) of the higher-order circuit. Consequently, the measurement selection algorithm for second-order circuits can be applied to select specifications that need to be measured.

The testability analysis for linearized analog circuits was presented in Chapter 7. A nonlinear analog circuit is linearized about an operation point and represented by its transfer function in the Laplace domain. The ambiguity groups can be determined based on the sensitivities of the poles and zeros of the linearized circuit.
The measurement selection is based on the parameter testability concept which gives an insight into the difficulty in testing the circuit parameters. Parameter testability can be obtained based on the pole sensitivities with respect to the circuit parameters. Our algorithm can also be utilized to reduce the test time without affecting fault coverage and to provide maximum information for fault identification.

8.1. Original Contributions

This section presents a brief summary of the original contributions found in this thesis.

- For the first time, the pole and zero sensitivity analysis is employed in order to compute the testability measure and to determine the ambiguity groups in analog circuits.
- The relationship between the testability measure and the number of the poles and zeros of a linear circuit in addition to the *DC* gain is discussed.
- A new interpretation of ambiguity groups is given based on the circuit theory in contrast to the mathematical interpretation given by linearly dependent columns of the testability matrix.
- The relationship between the testability analysis based on pole and zero analysis and controllability/observability from control theory.
- The element testability for linear circuits and the parameter testability for linearized circuits concepts are introduced in order to provide information about the difficulty in testing circuit

elements as well as the effect of variations of circuit elements on circuit specifications. Both concepts are independent of the time and the frequency.

- An algorithm for selecting specifications that need to be measured can be used in the frequency-domain or in the time-domain, because these specifications are related to the poles and zeros of a circuit which can represent the time and frequency responses.
- A measurement selection algorithm which can be employed simultaneously for reducing the test cost in terms of reducing the test time by reducing the number of specifications that need to be measured, and for maximizing the information about the fault identification.

8.2. Recommendations for Future Research

The software implementation for automating the testability analysis and measurement selection algorithms is the main goal for our future work. However, some further suggestions for future research can be given as follows

- The comparison between the complexity of our testability analysis method and the complexity of the previous methods [Liu94, Pan01, Star00, Fedi99, Man03] could be addressed.
- In this thesis, the element testability which reflects the difficulty in testing the circuit elements under a fault condition has been discussed. Since the circuit nodes are less than the circuit elements, it is desirable to compute the node testability which defined as the difficulty in testing the circuit nodes under a fault condition. The concept *root (pole-zero) localization* proposed in [Mant93, Gath01, Huan03] for a behavioral modeling of analog integrated circuits seems to be a promising concept for computing the node testability. It is also preferable to obtain the controllability and the observability of each node in a circuit.
- The parametric fault coverage could be computed using specifications which are selected to be measured. Also, these specifications could be utilized for developing a test signal generation algorithm.
- Measurement errors could be taken into account. Furthermore, the proposed algorithm for testability analysis could be extended to testing the switched-capacitor filters.

Appendix A

In this appendix we will describe two methods for computing the sensitivity, namely the adjoint method in Section A.1 and the measurement-based perturbation method, which is used in the Saber simulator, in Section A.2. Furthermore, the properties of the first-order sensitivity are given in Section A.3. The sensitivities of natural response specifications, time-domain specification, and frequency-domain specifications of second-order circuits are presented in Section A.4.

A.1. Adjoint Methods for Sensitivity Computation

In this section, the adjoint method for computing the sensitivity is addressed based on [Vlac94] (see also [Lito97]).

Consider a circuit of linear equations in the form

$$[Y][x] = [b] \tag{A-1}$$

where Y and b may be real or complex and depend on some circuit parameters h.

The solution of the linear equations is formally written as

$$[x] = [Y]^{-1}[b] \tag{A-2}$$

By differentiating Eq. (A-1) in order to evaluate the sensitivity of all components of the vector x to a single parameter h yields

$$Y\frac{\partial x}{\partial h} + \frac{\partial Y}{\partial h}x = \frac{\partial b}{\partial h} \tag{A-3}$$

Rewriting Eq. (A-3) yields

$$Y\frac{\partial x}{\partial h} = -\left(\frac{\partial Y}{\partial h}x - \frac{\partial b}{\partial h}\right) \tag{A-4}$$

If Eq. (A-1) is solved using *LU* decomposition and forward and backward substitution, the vector x is known. Thus the product $(\delta Y/\delta h)x$ can be formed and right-hand side of Eq. (A-4) can be generated. Since *LU* factors are already available, the solution of Eq. (A-4) requires only one additional forward and backward substitution to get $\delta x/\delta h$. The solution of Eq. (A-4) generates the sensitivity of the whole vector x with respect to a single variable element h.

The sensitivity of all components of x is seldom required. Frequently, a single output ϕ which is related to x is the output of interest, and the derivatives of ϕ with respect to many variable elements h_i are needed. This method is called *adjoint method* for computing the sensitivity. For notational simplicity, the subscript i of h will not be written in the derivations.

The formal solution of Eq. (A-4) is

$$\frac{\partial x}{\partial h} = -Y^{-1}\left(\frac{\partial Y}{\partial h}x - \frac{\partial b}{\partial h}\right) \tag{A-5}$$

Let the output of interest be a scalar variable $\phi(x)$. The $\phi(x)$ is a linear combination of the components of x

$$\phi = d^t x \tag{A-6}$$

where d is a constant vector. The objective now is to compute the sensitivity of the scalar function $\phi(x)$ with respect to h. By differentiating Eq. (A-6) yields

$$\frac{\partial \phi}{\partial h} = d^t \frac{\partial x}{\partial h} \tag{A-7}$$

Substitute for $\delta x/\delta h$ from (A-5)

$$\frac{\partial \phi}{\partial h} = -d^t Y^{-1}\left(\frac{\partial Y}{\partial h}x - \frac{\partial b}{\partial h}\right) \tag{A-8}$$

Note that the row vector $d^t Y^{-1}$ in Eq. (A-8) can be precomputed together with the solution vector x before the sensitivity calculations are carried out.

An adjoint vector x^a can be defined as

$$(x^a)^t = -d^t Y^{-1} \tag{A-9}$$

Postmultiply (A-9) by Y and take the transpose to get x^a as the solution to the system

$$Y^t x^a = -d \tag{A-10}$$

Substituting Eq. (A-9) into Eq. (A-8) yields

$$\frac{\partial \phi}{\partial h} = (x^{a\,t}) \frac{\partial Y}{\partial h} x - (x^{a\,t}) \frac{\partial b}{\partial h} \tag{A-11}$$

For each parameter h_i, the matrix $\delta Y/\delta h_i$ and the vector $\delta b/\delta h_i$ will be formed and the products indicated on the right-hand side of Eq. (A-11) evaluated. Using Eq. (A-11), the sensitivity of the function ϕ with respect to the parameter h_i can be computed as a function of the frequency. The computational procedure of the differential sensitivity for the adjoint approach is summarized as follows:

- Step 1: Solve the linear circuit described by Eq. (A-1).
- Step 2: Solve the adjoint circuit described by Eq. (A-9).
- Step3: For each parameter h_i, form $\delta Y/\delta h_i$and $\delta b/\delta h_i$. Insert in Eq. (A-11) to compute $\delta\phi/\delta h$.

By applying the sensitivity equation to the network problem, the right-hand side of Eq. (A-11) is just a multiplication of the component of x and x^a. The sensitivity formula can be expressed as

$$\frac{\partial \phi}{\partial h} = s^v (x_i^{\,a} - x_j^{\,a})(x_i - x_j) \tag{A-12}$$

where v is 1 for reactive elements and zero otherwise, x_i and x_j are the voltages nodes i and j, respectively, of the linear circuit, and x_i^a and x_j^a are the voltages nodes i and j, respectively, of the adjoint circuit.

A.2. Sensitivity Computation using Saber Simulator

The sensitivity can be computed by using *a measurement-based perturbation method* [Saber simulator online Handbook]. A specified parameter h_i is perturbed from its nominal value and the effect on a specified performance measure T_j for the design is determined as shown below:

$$\rho_{h_i}^{T_j} = \frac{\Delta T_j}{\Delta h_i} \tag{A-12}$$

This sensitivity is called *incremental sensitivity.* The incremental values $\Delta T_j/\Delta h_i$ tend to the differential sensitivity only in the limit as Δh --> 0.

To provide meaningful comparisons, the result is normalized as shown below:

$$\rho_{h_i}^{T_j} = \frac{\frac{\Delta T_j}{T_i}}{\frac{\Delta h_i}{h_i}} = \frac{h_i}{T_i} \cdot \frac{\Delta T_j}{\Delta h_i} \qquad \text{(A-13)}$$

where h_i is the nominal value of the perturbed parameter, T_j is the nominal value of the performance measure, ΔT_j is the amount by which the performance measure changes in response to the parameter perturbation, and Δh_i is the amount by which the parameter is perturbed.
When T_j or h_i is 0 or very close to 0, a fully normalized result cannot be calculated.

The perturbation method for calculating the sensitivity can be compared to another commonly used method, the adjoint (or matrix) method. Although the adjoint method provides fast results, it is more limited in its use because it can be used only to calculate the sensitivity of quantities that are part of the design, typically node voltages and some branch currents. Quantities that must be measured from a waveform, such as the duty cycle or rise time, cannot be determined with the adjoint method.
Thus, the perturbation method used by the Saber simulator is more versatile in that it can be used to determine the sensitivity of any measurable quantity that can be extracted from the results of an analysis.

Saber uses the following process to execute the sensitivity analysis:

1) Increase the parameter value by the value defined in the Perturbation field.
2) Run the specified analyses.
3) Calculate the specified measurements.
4) Repeat steps 1- 3 for each parameter in the Parameter List field.
5) Repeat steps 2 and 3 using the nominal parameter values.
6) Calculate the sensitivity based on the difference between the nominal and perturbed parameter values.

Practical considerations rule out incremental sensitivity. First, the incremental values $\Delta x/\Delta h$ tend to the differential sensitivity only in the limit as Δh --> *0*, and a very small value of Δh in computations is precluded by roundoff errors. Second, the sensitivity evaluation for each element *h* requires the formulation and solution of Eq. (A-1), resulting in high computational cost. These difficulties are avoided by using the adjoint methods as discussed above.

A.3. Sensitivity Properties

The properties of the first-order sensitivity are given [Fila95, Su96]

$$S_x^{ky} = \frac{x}{ky} \cdot \frac{\partial}{\partial x} ky = \frac{x}{y} \cdot \frac{\partial y}{\partial x} = S_x^y$$

$$S_x^{y+k} = \frac{x}{y+k} \cdot \frac{d(y+k)}{dx} = \frac{y}{y+k} \cdot \frac{x}{y} \cdot \frac{dy}{dx} = \frac{y}{y+k} S_x^y$$

$$S_{\frac{1}{x}}^{y} = \frac{\frac{1}{x}}{y} \cdot \frac{dy}{d\frac{1}{x}} = \frac{\frac{1}{x}}{y} \cdot \frac{dy}{dx} \cdot \frac{dx}{d\frac{1}{x}} = -\frac{x}{y} \cdot \frac{dy}{dx} = -S_x^y$$

$$S_x^{\frac{1}{y}} = \frac{x}{\frac{1}{y}} \cdot \frac{d\frac{1}{y}}{dx} = -S_x^y$$

$$S_x^{y_1 y_2} = \frac{x}{y_1 y_2} \frac{d(y_1 y_2)}{dx} = \frac{x}{y_1 y_2}\left(y_1 \frac{dy_1}{dx} + y_2 \frac{dy_2}{dx}\right) = \frac{x}{y_1}\frac{dy_1}{dx} + \frac{x}{y_2}\frac{dy_2}{dx} = S_x^{y_1} + S_x^{y_2}$$

$$S_x^{\frac{y_1}{y_2}} = S_x^{y_1} - S_x^{y_2}$$

$$S_{x^n}^{y} = \frac{1}{n} S_x^{y}$$

$$S_x^{y^n} = n S_x^{y}$$

$$S_x^{y} = S_z^{y} - S_x^{z}$$

$$S_x^{y_1 + y_2} = \frac{y_1 S_x^{y_1} + y_2 S_x^{y_2}}{y_1 + y_2}$$

$$S_x^{\ln y} = \frac{S_x^{y}}{\ln y}$$

$$S_x^{e^y} = y S_x^{y}$$

$$S_x^{\prod_{i=1}^{n} y_i} = \sum_{i=1}^{n} S^{y_i}$$

$$S_x^{\sum_{i=1}^{n} y_i} = \frac{\sum_{i=1}^{n} y_i S_x^{y_i}}{\sum_{i=1}^{n} y_i}$$

$$S_x^{\,y} = S_x^{\,|y|} + j(\arg y) S_x^{\,(\arg y)}$$

$$S_x^{\,|y|} = Re\{S_x^{\,y}\}$$

$$S_x^{\,\arg y} = \frac{1}{\arg y} Im\{S_x^{\,y}\}$$

where y is the circuit performance, x is the circuit element, and k is a constant and is independent of circuit element x.

A.4. Sensitivities of Natural Response, Time-Domain, and Frequency-Domain Specifications for Second-Order Circuits

The sensitivity of a circuit specification with respect to a circuit element can be derived based on the above-mentioned sensitivity properties and the equation of a specification given in Chapter 4.

The normalized differential sensitivities of the natural response specifications as a function of the normalized differential sensitivity of a circuit pole S_x^p are given [Herp86]

$$S_x^{\omega_n} = Re\{S_x^{\,p}\}$$

$$S_x^{Q} = -\sqrt{4Q^2 - 1} \cdot Im\{S_x^{\,p}\}$$

$$S_x^{\zeta} = -S_x^{Q}$$

where x is the circuit element, p is the circuit pole, ω_n is the natural frequency, Q is the Quality factor, ζ is the damping ratio, *Re* is the real part of the pole sensitivity, *Im* is the imaginary part of the pole sensitivity.

The normalized differential sensitivities of the time-domain specifications as a function of the normalized differential sensitivity of the natural response specifications are given

$$S_x^{t_{max}} = -S_x^{\omega_n} + \frac{\zeta^2}{1-\zeta^2} S_x^{\zeta}$$

$$S_x^{t_s} = -S_x^{\omega_n} - S_x^{\zeta}$$

$$S_x^{OS} = -S_x^{\zeta} \cdot \frac{\pi\zeta}{\sqrt{1-\zeta^2}} \left(1 + \frac{\zeta^2}{1-\zeta^2}\right)$$

$$S_x^{t_r} = -S_x^{\omega_n} + \frac{2.5\zeta}{0.8 + 2.5\zeta} S_x^{\zeta}$$

where t_{max} is the peak time, t_r is the time rise, t_s is the settling time, OS is the Maximum overshoot.

The normalized differential sensitivities of the frequency-domain specifications of low-pass filters as a function of the normalized differential sensitivity of the natural response specifications are given

$$S_x^{\omega_r} = S_x^{\omega_n} - \frac{2\zeta^2}{1-2\zeta^2} S_x^{\zeta}$$

$$S_x^{M_r} = S_x^{\zeta}\left(\frac{\zeta^2}{1-\zeta^2} - 1\right)$$

$$S_x^{BW} = S_x^{\omega_n} + \frac{S_x^{\zeta}}{2(1-2\zeta^2) + 2\sqrt{\zeta^4 + 4\zeta^2 + 2}}\left(-4\zeta^2 + \frac{4\zeta^4 + 2}{2\sqrt{\zeta^4 + 4\zeta^2 + 2}}\right)$$

where M_r is the resonant peak (the maximum value of the $|M(j\omega)|$), ω_r is the resonant frequency (the frequency at which the peak resonant M_r occurs), and BW is the bandwidth of low-pass filters.

The normalized differential sensitivities of the frequency-domain specifications of band-pass filters as a function of the normalized differential sensitivity of the natural response specifications are given

$$S_x^{BW} = S_x^{\omega_n} + S_x^{\zeta}$$

$$S_x^{\omega_H} = S_x^{\omega_n} + S_x^{\zeta}\frac{\zeta}{\sqrt{1+\zeta^2}}$$

$$S_x^{\omega_L} = S_x^{\omega_n} - S_x^{\zeta}\frac{\zeta}{\sqrt{1+\zeta^2}}$$

$$S_x^{\omega_{max}} = S_x^{\omega_n}$$

where BW is the bandwidth of band-pass filters, ω_H is the high-cutoff frequency (rad/sec), ω_L is the low-cutoff frequency (rad/sec), and ω_{max} is the center frequency (rad/sec).

References

[Abde96] A. Abderrahman, E. Cerny, B.Kaminska, “Optimization-Based Multifrequency Test Generation for Analog Circuits,” Journal of Electronic Testing: Theory and Applications, 13, 59-73, 1996.

[Abra90] Miron Abramovuci, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design.” Computer Science Press, 1990.

[Abra95] Jacob A. Abraham, “Mixed-Signal Test,” Tutorial in The European Design and Test Conference, ED&TC 1995.

[Amni00] Farzan Aminian and Mehran Aminian, “Neural-Network Based Analog Circuit Fault diagnosis Using Wavelet Transform as Preprocessor,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL.47, NO. Feb. 2000.

[Amin01] Farzan Aminian and Mehran Aminian, “Fault Diagnosis of Analog Circuits Using Bayesian Neural Networks with Wavelet Transform as Preprocessor,” Journal of Electronic Testing: Theory and Applications, 17, pp:29-36, 2001.

[Anal97] Analyzing Designs Using SaberDesigner, Release 4.2, Analogy, Inc. 1995-1997.

[Anal01] AnalogInsydes Version 2, Fraunhofer Institut für Techno- und Wirtschaftsmathematik (ITWM), 2001

[Arab97] K. Arabi and B. Kaminska, “Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits,” in Proceedings of International Test Conference, pp:786-795, 1997.

[Ashe03] Peter J. Ashenden, Gregory D. Peterson and Darrell A. Teegaden, “The System Designer’s Guide to VHDL-AMS: Analog, Mixed-Signal, and Mixed-Technology Modeling,” Moggan Kaufmann Publishers, 2003.

[Bali96a] Ashok Balivada, Hong Zheng, Naveena Nagi, Abhijit Chatterjee, Jacob A. Abraham, “A Unified Approach for Fault Simulation of Linear Mixed-Signal Circuits,” Journal of Electronic Testing: Theory and Applications, 9, 29-41, 1996.

[Bali96b] Ashok Balivada, Jin Chen, Jacob A. Abraham, “Analog Testing with Time Response Parameters,” IEEE Design&Test of Computers, pp:18-25, Summer 1996.

[Bali96c] Ashok Balivada, “Structured Test Generation Techniques for Analog and Mixed Signal Circuits,” Diss. The University of Texas at Austin, 1996

[Band85] John W. Bandler and Aly E. Salama, “Fault Diagnosis of Analog Circuits,” Proceedings of IEEE, VOL.73, NO.8, August 1985.

[Bane94] Prithviraj Banerjee, “Parallel Algorithms for VLSI Computer-Aided Design,” PTR Prentice Hall, 1994.

[Beck94] Toralf Becker, “Zur Applikation von Testbarkeitsanalyseverfahren für die Untersuchung des testfreundlichern Entwurfs digitaler und analoger Schaltungen,” Diss. Technische Universität Dresden, 1994.

[Beck95] T. Becker and U. Frühauf, “Applikation von Testbarkeitsmaßen bei analogen Schaltungen,” Nachrichten., Elektron., Berlin 45, 1995

[Biol01] D. Biolek, V. Biolkova and J. Dobes, “Semisymbolic Modeling of Large Linear Systems: Pending Issues,” www.utko.fee.vutbr.cz/~biolek/ veda/articles/ISSSE01.pdf

[Brat95] A.H. Brat, A.M.D. Richardson, R.J.A. Harvey and A.P. Dorey “A Design-For-Test Structure for Optimizing Analogue and Mixed Signal IC Test,” ED&TC pp: 24-33, 1995.

[Burd01] Bernhard Burdiek, “Generation of Optimum Test Stimuli for Nonlinear Circuits Using Nonlinear Programming and Time-Domain Sensitivities,” DATE, 2001

[Burn01] Mark Burns and Gordon W. Roberts, “An Introduction to Mixed-Signal IC Test and Measurement.” Oxford University Press, 2001

[Buhs00] Michael L. Bushnell and Vishwani D. Agrawal, “Essential of Electronic Testing for Digital, Memory&Mixed-Signal VLSI Circuits.” Kluwer Academic Publishers, 2000.

[Boyl74] Graeme R. Boyle, Barry M. Cohn, Donald o. Perderson, and James E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,”IEEE Journal of Solid-State Circuits, Vol. sc-9, No. 6, December 1974.

[Carm91] R. Carmassi, M. Catelani C. Iuculano, S. Manetti, and M. Marini, “Analog Network Testability Measurement: Symbolic Formulation Approach,” IEEE Trans. on Instrumentation and Measurement, VOl. 40, NO. 6, December 1991.

[Cate87] M. Catelani, G. Iuculano, A. Liberatore, S. Manetti, and M. Marini, “Improvements to Numerical Testability Evaluation,” IEEE Trans. on Instrumentation and Measurement, VOL. IM-36, NO. 4, December 1987.

[Cate96] M. Catelani, M. Gori, “On the Application of Neural Networks to Fault Diagnosis of Electronic Analog Circuits,” Measurements, Vol. 17, No. 2, pp:73-80, 1996.

[Caun96] Pascal Caunegre and Claude Abraham, “Fault Simulation for Mixed-Signal Systtems.” Journal of Electronic Testing: Theory and Applications, Vol.8, pp:143-152, 1996.

[Chan02] Soon-Jyh Chang, Chung Len Lee and Jwu E Chen, “Structural Fault Driven Specification-Constrained Test Frequency Generation for Analog Circuits,” International Mixed signal Testing Workshop, pp: 109-117, 2002.

[Chao95a] K. S. Chao, “State-Variable Techniques,” Chapter 23 in The Circuits and Filters Handbook, Ed. by Wai-Kai Chen, CRC Press and IEEE Press, 1995

[Chao95b] C.Y. Chao and L. Milor, “Built-In Self-Test and Fault Diagnosis for Analog Circuits in the Frequency Domain,” Tech. Report, http://techreportr.isr.umd.edu/TechReports/ISR/1995/TR_95-15/TR_95-15.phtml, 1995.

[Chao97] Chieh-Yuan Chao, Hung-Jen Lin, and Linda Milor, “Optimal Testing of VLSI Analog Circuits,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol.16,No.1, January 1997.

[Chat93] A. Chatterjee, “Concurrent Error Detection and Fault-Tolerance in Linear Analog Circuits Using Continuous Checksum,” IEEE Trans. on VLSI Systems, VOL. 1, pp: 138-150, June 1993.

[Chat96] A. Chatterjee and Naveena Nagi, “DC Built-In Self-Test for Linear Analog Circuits,: IEEE DEsign & Test of Computers, Summer 1996.

[Chat97] A. Chatterjee and Naveena Nagi, “Design for Testability and Built-In Self-Test of Mixed-Signal Circuits: A Tutorial,” International Conference on VLSI Design, pp: 388-392, January 1997.

[Chen79] H. S. M. Chen and R. Saek, “A Search Algorithm for the Solution of the Multifrequency Fault Diagnosis Equations,” IEEE Trans. 0n Circuits and Systems, VOL. CAS-26, NO. 7, July 1979.

[Cher99] S. Cherubal and A. Chatterjee, “Parametric Fault Diagnosis for Analog Systems using Functional Mapping,” DATE, 1999.

[Cher01] S. Cherubal and A. Chatterjee, “Test Generation Based on Diagnosis of Device Parameters for Analog Circuits,” DATE, 2001.

[Chip94] Eli Chiprout and Michel S. Nakhla, “Asymptotic Waveform Evaluation and Moment Matching for Interconnect Analysis,” Kluwer Academic Publishers, 1994.

[Claa03] Theo A.C.M. Claasen, “System on a Chip: Changing IC Design Today and in the Future,” IEEE Micro, May-June 2003.

[Dai90] Hong Dai and M. Sounders, “Time-Domain Testing Strategies and Fault Diagnosis for Analog Systems,” IEEE Trans. on Instrumentation and Measurement, VOL. 39, NO. 1, February 1990.

[Deva94] Gire Devarayanadurg and Mani Soma, “Analytical Fault Modeling and Static Test Generation for Analog ICs,” International Conference on Computer-Aided Design, pp: 44-47, 1994.

[Deva95] Gire Devarayanadurg and Mani Soma, “Dynamic Test Signal for Analog ICs,” International Conference on Computer-Aided Design, pp: 627-630, 1995.

[Dire69] Stephen W. Director and Ronlan A. Rohrer, “The Generalized Adjoint Network and Network Sensitivities” IEEE Transactions on Circuit Theory, Vol. CT-16, No. 3, pp: 318-323, August 1969.

[Dufo99] Benoit Dufort and Gordon W. Roberts, “On-Chip Analog Signal Generation for Mixed-Signal Built-In Self-Test,” IEEE Journal of Solid-State Circuits, VOL.34, NO.3, March 1999.

[Dufo00] Benoit Dufort and Gordon W. Roberts, “Analog Test Signal Generation Using Periodic Sigma/Delta Encoded Data Streams.” Kluwer Academic Publishers, 2000.

[Engi00] Nur Engin, “Linking Mixed-Signal Design and Test: Generation and Evaluation of Specification-Based Tests,” University of Twente in Enschede, the Netherlands, 2000.

[Engi03] Nur Engin and Hans G. Kerkhoff, “Fast Fault Simulation for Nonlinear Analog Circuits,” IEEE Design & Test of Computers, March-April, 2003.

[Fann99] A. Fanni, A. Giua, M. Marchesi, and A. Montisci, “A Neural Network Diagnosis Approach for Analog Circuits,” Journal of Applied Intelligence, pp:1-20, 1999.

[Fedi98a] G. Fedi, R. Giomi, A. Luchetta, S. Manetti, and M. C. Piccirilli, “On the Application of Symbolic Techniques to the Multiple Fault Location in Low Testability Analog Circuits,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 45, NO. 10, October 1998.

[Fedi98b] G. Fedi, A. Luchetta, S. Manetti, and M. C. Piccirilli, “A New Symbolic Method for Analog Circuit Testability Evaluation,” IEEE Trans. on Instrumentation and Measurement, VOL. 47, NO. 2, April 1998.

[Fedi99] G. Fedi, S. Manetti, M. C. Piccirilli, and J. Starzyk, “Determination of an Optimum Set of Testable Components in the Fault Diagnosis of Analog Linear Circuits,” IEEE Trans. on Circuits and Systems-I, Fundamental Theory and Applications, VOL. 46, NO. 7, July 1999.

[Feld95] P. Feldmann and R. W. Freund, “Efficient Linear Circuit Analysis by Páde Approximation via the Lanczos Process,” IEEE Trans. om Computer-Aided Design, vol.14, pp: 639-649, May 1995.

[Fidl84] J. K. Fidler, “Differential-Incremental Sensitivity Relationship,” Electronics Letters, Vol. 20, No. 10, pp: 626-627, May 1984

[Fila95] Igor M. Filanovsky, “Sensitivity and Selectivity,” Chapter 68 in the Circuits and Filters Handbook, Ed. Wai-Kai Chen, CRC Press and IEEE Press, 1995.

[Fris97] A. Frish, T. Almy, “HABIST: Histrogram-Based Analog Built-In Self-Test,” International Test Conference, pp:760-767, 1997.

[Gath01] C. Gathercole and H. A. Mantooth, “Pole-Zero Localization: A Behavioral Modeling Approach,” IEEE International Workshop on Behavioral Modeling and Simulation, pp: 59-65, Oct. 2001

[Giel91] G. Gielen and W. Sansen, “Symbolic Analysis for Automated Design of Analog Integrated Circuits,” Kluwer, 1991.

[Giel94] G. Gielen, P. Wambaco and W. M. Sansen, “Symbolic Analysis Methods and Applications for Analog Circuits: A Tutorial Overview,” Proceeding of the IEEE, Vol. 82, NO. 2, February 1994.

[Golu96] Gene H. Golub, Charles F. Van Loan, “Matrix Computations,” 3ed, The Johns Hopkins University Press, 1996

[Hale88] Stephen B. Haley, “The Generalized Eigenproblem: Pole-Zero Computation,” Proceedings of the IEEE, Vol.76, No. 2, February 1988.

[Half03] T. Halfmann and T. Wichmann, “Overview of Symbolic Methods in Industrial Analog Circuit Design,” Tech. Report, Fraunhofer ITWM, Nr. 44, 2003.

[Hami93] Naim Ben Hamida and Bozena Kaminska, “Multiple Fault Analog Circuit Testing by Sensitivity Analysis,” Analog Integrated Circuits and Signal Processing 4, pp: 231-243, 1993.

[Hami96a] Naim Ben Hamida, Khaled Saab, David Mache, Bozena Kaminska and Guy Quesnel, “LIMSoft: Automatic Tool for Design and Test Integration,” International Mixed Signal Testing Workshop, pp: 56-71, 1996.

[Harv94] R.J.A. Harvey, A.M.D. Richardson, E.M.J.G. Bruls, K. Baker, “Analogue Fault Simulation Based on Layout Dependent Fault Models,” International Test Conference,pp:641-649, 1994.

[Hass98] Marwan Hassoun, “Symbolic Analysis Techniques: A Review,” Chapter 2 in Symbolic Analysis Techniques: Applications to Analog Design Automation, Edited by F. Fernández, A. Rodríguez-Vázquez, J. L. Huertas, and G.E. Gielen, IEEE Press, 1998.

[Hemi90] Gertjan J. Hemink, Berend W. Meijer and Hans Kerkhoff, “Testability Analysis of Analog Systems,” IEEE Trans. on Computer-Aided Design, VOL. 9, NO. 6, June 1990.

[Henn98] E. Hennig, M. Wiese, and R. Sommer, “Symbolic Pole/Zero Approximation Using Eigenvalue Shift Prediction,” Proc. 5th International Workshop Symbolic Methods and Application to Circuit Design (SMACD98), 1998.

[Herp86] M. Herpy and J.-C. Berka, “Active RC Filter Design,” Akademiai Kiado, Budapest, 1986.

[Ho01] C.K. Ho, P. R. Shepherd, F. Eberhardt, and W. Tenten, “Hierarchical Fault Diagnosis of Analog Integrated Circuits,” IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 48, No. 8, August 2001.

[Houl96] A. Holubek, W. Vermeiren, and R. Spallek, “Analogue Fault Simulation on Distributed Platforms,” IFIP/IEEE International Conference on Distributed Platforms ICDP’96, Dresden, 1996.

[Horn99] Ernst-Helmut Horneber, “Schaltungssimulation- eine Übersicht,” in Simulationstechnik, 13 Symposium in Weimar, Herausgegeben von Georg Hohman, pp:1-14, Sept. 1999.

[Huan98a] Wei-Hsing Huang and Chin-Long Wey, “Diagnosibility Analysis of Analogue Circuits,” International Journal of Circuit Theory and Applications, VOL.26, pp:439-451, 1998.

[Huan98b] Wei-Hsing Huang and Chin-Long Wey, “Test Point Selection Process and Diagnosability Analysis of Analog Integrated Circuits,” Proc. International Conference on Computer Design, Oct. 1998.

[Huan98c] Wei-Hsing Huang, “Development of Efficient Fault Diagnosability Design Methodologies for Analog/Mixed-Signal Integrated Circuits,” Dissertation, Department of Electrical Engineering, Michigan State University, 1998.

[Huan03] Xiaoling Huang, Chris S. Gathercole and H. Alan Mantooth, “Modeling Nonlinear Dynamic in Analog Circuits Via Root Localization,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems. VOL. 22, NO. 7, July 2003.

[Huar98] X. Huarie and G. W. Roberts, “Arbitrary-Precision Signal Generation for Mixed-Signal Built-In Self-Test,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 45, NO. 11, November 1998.

[Huer93a] J. L. Huertas, “Test and Design for Testability of Analog and Mixed-Signal Integrated Circuits: Theoretical Basis and Pragmatical Approaches.” In Circuit Theory and Design: Selected Topics in Circuits and Systems, Ed. D.G. Haigh, J.L. Huertas, P.A. Humblet, M. Kunt, Elsevier Science Publishers, 1993.

[Huer93b] J. L. Huertas, A. Rueda, and D. Vazquez, “Testable Switched-Capacitor Filters, IEEE Journal of Solid-State Circuits, VOL.28, pp: 719-724, July 1993.

[Huss91] Scott D. Huss and Ronald S. Gyurcsik, “Optimal Ordering of Analog Integrated Circuit Tests to Minimize Test Time,” in Proc. ACM/IEEE Design Automation Conference DAC, pp: 494-499, 1991.

[Hyun98] Sam D. Huynh, Seongwon Kim, Mani Soma and Jinyan Zhang, “Testability Analysis and Multi-Frequency ATPG for Analog Circuits and Systems,” Proc. of ICCAD, pp: 376-383, 1998.

[Huyn99] Sam D. Huynh, Seongwon Kim, Mani Soma and Jinyan Zhang, “Automatic Analog Test Signal Generation Using Multifrequency Analysis,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 46, NO. 5, May 1999.

[Iucu86] G. Iuculando, A. Liberatore, S. Manetti and M. Marini, “Multi-Frequency Measurement of Testability with Application to Large Linear Analog Systems,” IEEE Trans. on Circuits and Systems, VOL. CAS-33, NO. 6, June 1986.

[John89] Barry W. Johnso, “Design and Analysis of Fault-Tolerant Digital Systems.” Addison-Wesley Publishing Company, 1989

[Kac03] Uros Kac, Franc Novak, Florence Azaïs, Pasacl Nout and Michel Renovell, “Extending IEEE Std. 1149.4 Analog Boundary Modules to Enhance Mixed-Signal Test,” IEEE Design & Test of Computers, March-April, 2003.

[Kerk94] Hans Kerkhoff, “Design for Testability,” Chapter 12 in Analog VLSI Signal and Information Processing, Ed. Mohammed Ismail and Terri Fiez, McGraw-Hill, Inc, 1994.

[Kami97] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Huertas, B. Kim, A. Rueda, and M. Soma, “Analog and Mixed-Signal Benchmark Circuits- First Release,” International Test Conference, 1997.

[Kuij95] F.C.M. Kuijstermans and M. Sachdev, “Defect-Oriented Test Methodology for Complex Mixed-Signal Circuits,” European Design and Test Conference (ED&TC), pp:18-23, March 1995.

[Koa95] Benjamin C. Kuo, “Automatic Control Systems,” 7ed. JohnWiley & Sons, 1995.

[Law00] Averil M. Law and W. David Kelton, “Simulation Modeling and Analysis,” McGraw-Hill Companies, 2000.

[Lee92] John Y. Lee, X. Huang, and R. A. Rohree, “Pole and Zero Sensitivity Calculation in Asymptotic Waveform Evaluation,” IEEE Trans. on Computer-Aided Design, VOL.11, NO. 5, May 1992.

[Lind95] Walter M. Lindermeir, Helmut E. Graeb, and Kurt J. Antreich, “Design Based Analog Testing by Characteristic Observation Inference,” in Proc. of International Conference on Computer-Aided Design, pp” 620-626, 1995.

[Lind97] Walter Matthias Lindermeir, “Testentwurf für analoge integrierte Schaltungen mit charakteristischen Beobachtungen.” Technische Universität München, 1997.

[Lind99] Walter M. Lindermeir, Helmut E. Graeb, and Kurt J. Antreich, “Analog Testing by Characteristic Observation Inference,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, VOL. 18, NO. 9, September 1999.

[Lito97] V. Litovski and M. Zwolinski, “VLSI Circuit Simulation and Optimization,” Chapman & Hall, 1997.

[Liu91] Ruey-Wen Liu, “Testing and Diagnosis of Analog Circuits and Systems.” Van Nostrand Reinhold, 1991.

[Liu94] Edward Liu, William Kao, Eric Felt and A. S. Vincentelli, “Analog Testability Analysis and Fault Diagnosis Using Behavioral Modeling,” Proc. Custom Integrated Circuit Conferenc, pp; 453-456, May 1994.

[Liu99] Zhi-Hong Liu, “Mixed-Signal Testing of Integrated Analog Circuits and Modules.” Diss. Ohio University, 1999.

[Liu96] Ji-Gou Liu, “Testbarkeitsanalyse analoger Schaltungen und Systeme -Ein Beitrag zur Meß- und Prüftechnik elektronischer Systems.”, Technische Universität Dresden, 1996.

[Liu02] D. Liu and J. A. Starzyk, “A Generalized Fault Diagnosis in Dynamic Circuits,” International Journal of Circuit Theory and Applications, Vol. 30, No. 5, pp: 487-510, 2002.

[Lu93] Yunsheng Lu and R. Dandapani, “Hard Faults Diagnosis in Analog Circuits Using Sensitivity Analysis,” PRoc. of VLSI Test Symposium, pp: 225-229, 1993.

[Lu94] A.K. Lu and G.W. Roberts, “An Analog Multi-Tone Signal Generator of Built-In Self-Test Applications,” Proc. of International Test Conference, pp: 650-659, 1994.

[Maho87] Matthew Mahoney, “Tutorial: DSP-Based Testing of Analog and Mixed-Signal Circuits,” IEEE Computer Society Press, 1987.

[Mant90] Alan Mantooth, “Higher Level Modeling of Analog Integrated Circuits, Georgia Institute of Technology, 1990.

[Mant95] H. Alan Mantooth and Mike Fiegenbaum, “Modeling with an Analog Hardware Description Language,” Kluwer Academic Publishers, 1995.

[Mane98] Stefano Manetti, “Analog Testability and Fault Diagnosis Using Symbolic Analysis,” Chapter 13 in Symbolic Analysis Techniques: Applications to Analog Design Automation, Edited by F. Fernández, A. Rodríguez-Vázquez, J. L. Huertas, and G.E. Gielen, IEEE Press, 1998.

[Mane03] Stefano Manetti and Maria Cristina Piccirilli, “A Singular-Value Decomposition Approach for Ambiguity Group Determination in Analog Circuits,” IEEE trans. on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 50, No. 4, April 2003.

[Meix91] Anne Meixner and Wojciech Maly, “Fault Modeling for the Testing of the Mixed Integrated Circuits.”, International Test Conference, pp:564-572, 1991.

[Milo89] Linda Milor and V. Visvanathan, “Detection of Catastrophic Faults in Analog Integrated Circuits,” IEEE Trans. on Computer-Aided Design, Vol.8, No.2, Feb. 1989.

[Milo90] Lida Milor and Alberto Sangiovanni-Vincentelli, “Optimal Test Set for Analog Circuits,” IEEE International Conference on Computer Aided Design, pp: 294-297, 1990.

[Milo94] Linda Milor, “Minimizing Production Test Time to Detect Faults in Analog Circuits,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol.13,No.6, June 1994.

[Milo98] Linda Milor, “A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, Vol.45, No. 10, October 1998.

[Mir95] S. Mir, M. Lubbaszewski, V. Liberal and B. Courtios, “Built-In Self-Test Approaches for Analogue and Mixed-Signal Integrated Circuits,” IEEE Midwest Symposium on Circuits and Systems, 1995.

[Mir96a] S. Mir, M. Lubaszewski, B. Courtois, “Fault-Based ATPG for Linear Analog Circuits with Minimal Size Multifrequency,” Journal of Electronic Testing: Theory and Applications, 9, 43-57, 1996.

[Mir96b] S. Mir, M. Lubaszewski, B. Courtois, “Unified Built-In Self-Test for Fully Differential Analog Circuits,” Journal of Electronic Testing: Theory and Applications, 9, 135-151, 1996.

[Mir97] S. Mir, A. Rueda, J. L. Huertas and V. Liberali, “A BIST Technique for Sigma-Delta Modulators Based on Circuit Reconfiguration,” International Mixed Signal Testing Workshop, pp: 179-184, 1997.

[Naig92] Naveene Nagi and Jacob A. Abraham, “Hierarchical Fault Modeling for Analog and Mixed-Signal Circuits,” in IEEE VLSI Test Symposium, pp:96-101, 1992.

[Nagi93] Vaveena Nagi, Abhijit Chatterjee and Jacob Abraham, “DRAFTS: Discretized Analog Circuit Fault Simulator,” ACM/IEEE Design Automation Conference (DAC), pp: 509-514, 1993.

[Nagi93] Vaveena Nagi, Abhijit Chatterjee and Jacob Abraham, “Fault Simulation of Linear Analog Circuits,” Journal of Electronic Testing: Theory and Applications, 4, 345-360, 1993.

[Nagi96] Naveene Nagi and Jacob A. Abraham, “Hierarchical Fault Modeling for Linear Analog Circuits,” Analog Integrated Circuits and Signal Processing, 10,89-99, 1996.

[Nass84] S.R, Nassif, A. J. Strojwas, and S. W. Director, “FABRICS II: A Statistically Based IC Fabrication Process Simulator,” IEEE Trans. on Computer-Aided Design, 1984

[Newt84] Arthur Richard Newton and Alberto L. Sangiovanni-Vincentelli, “Relaxation-Based Electrical Simulation,” IEEE Trans. on Computer-Aided Design, VOL. CAD-3, NO. 4, October 1984.

[Ohle91] Michael J. Ohletz, “Hybrid Built-In Self-Test (HBIST) for Mixed Analogue/Digital Integrated Circuits,” European Test Conference, pp: 307-316, 1991.

[Ohe96a] Michael J. Ohletz, “Fault Modeling and Simulation for the Test of Integrated Analog and Mixed-Signal Circuits.” Chapter 13 in “Low Power HF Microelectronics a Unified Approach.” Ed. by Gerson A. S. Machado, The Institution of Electrical Engineers, 1996.

[Ohle96b] Michael J. Ohletz, “Realistic Fault Mapping Scheme for the Fault Simulation of Integrated Analogue CMOS Circuits,” International Test Conference, pp: 776-785, Oct. 1996.

[Olbr96] Thomas Olbrich, Jordi Pérez, Ian A. Grout, Andrew M. D. Richardson, Carles Ferrer, “Defect-Oriented vs. Schematic-Level Based Fault Simulation for Mixed-Signal ICs.,” International Test Conference, pp: 511-520, 1996.

[Osse99] Adam Osseiran, “Analog and Mixed-Signal Boundary-Scan: A Guide to the IEEE 1149.4 Test Standard,” Kluwer Academic Publishers, 1999.

[Pan94] Chen-Yang Pan, Kwang-Ting Cheng and Sandeep Gupta, “A Comprehensive Fault for Opamps,” in Proc. ICCAD, pp: 244-348, Nov. 1994.

[Pan96] Chen-Yang Pan, Kwang-Ting Cheng and Sandeep Gupta, “Fault Macromodeling and a Testing Strategy for Opamps,” Journal of Electronic Testion: Theory and Applications, Vol.9, No.3, pp:225-235, 1996.

[Pan97] Chen-Yang Pan, Kwang-Ting Cheng, “Fault Macromodeling for Analog/Mixed-signal Circuits,” In International Test Conference, pp:, 1997.

[Pan97b] Chen-Yang Pan, Kwang-Ting Cheng, “Pseudorandom Testing for Mixed-Signal Circuits,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, VOL. 16, NO.10, October 1997.

[Pan97] Chen-Yang Pan, “Built-In-Self Test and Fault Simulation for Analog/Mixed-Signal Circuits.” University of California, 1997.

[Pan99] Chen-Yang Pan, Kwang-Ting Cheng, “Test Generation for Linear Time-Invariant Analog Circuits,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, Vol.46, No. 5, May 1999.

[Pang01] J. Pang and J. Starzyk, “Fault Diagnosis in Mixed-Signal Low Testability System,” Journal of Analog Integrated Circuits and Signal Processing, 28, pp: 161-171, 2001.

[Penf70] P. Penfield, R. Spence, and S. Duinker, “A Generalized Form of Tellegen’s Theorm” IEEE Transactions on Circuit Theory, Vol. CT-17, No. 3, pp: 302-305, August 1970.

[Perk98] A.J. Perkins, M. Zwolinski, C.D. Chalk and B.R. Wilkins, “Fault Modeling and Simulation Using VHDL-AMS,” Analog Integrated Circuits and Signal Processing. 16,141-155, 1998.

[Pi02] Tao Pi and Richard Shi, “Analog-Testability Analysis by Determinant-Decsion-Diagrams Based Symbolic Analysis,” International Mixed Signal Testing Workshop IMSTW 2002, pp: 9-13, 2002.

[Pill95] Lawrennce T. Pillage, Ronald A. Rohrer and Chandramouli Visweswariah, “Electronic Circuit and System Simulation Methods,” McGraw-Hill, Inc. 1995

[Prie81] R.W. Priester and J. B. Clary, “New Measures of Testability and Test Complexity for Linear Analog Failure Analysis,” IEEE Trans. on Circuits and Systems, VOL. CAS-28. NO. 11, November 1981.

[Prie98] J. A. Prieto, A. Rueda, I. Grout, E. Peralias, J. L. Huertas and A. M. D. Richardson, “An Approach to Realistic Fault Prediction and Layout Design for Testability in Analog Circuits,” DATE, pp:905-909, 1998.

[Pron00] M. Pronath V. Gloeckel, and H. Graeb, “A Parametric Test Methods for Analog Components in Integrated Mixed-Signal Circuits,” Proc. of International Conference on Computer Aided Design, ICCAD 2000.

[Raja00] Vivek Kumar Rajan, Krishna R. Pattipati and Jie Luo, “Fault Diagnosis in Mixed-Signal Circuits Via Neural Network Based Classification algorithm.

[Ram99] Rajesh Ramadoss and Michael L. Bushnell, “Test Generation for Mixed-Signal Devices Using Signal Flow Graphs,” Journal of Electronic Testing: Theory and Applications, 14, 189-205, 1999.

[Reno98] M. Renovell, F. Azaïs and Y. Bertrand, “Optimized Implementation of the Multi-Configuration DFT Technique for Analog Circuits,” DATE 1998, pp: 815-821, 1998.

[Robe95] Gordon W. Roberts and Albert K. Lu: “Analog Signal Generation for Built-In-Self-Test of Mixed-Signal Integrated Circuits.” Kluwer Academic Publishers, 1995.

[Robe97] Gordon Roberts, “DFT Techniques for Mixed-Signal Integrated Circuits,” Chapter 6.2 in Circuits and Systems in the Information Age, IEEE Press, pp:251-271, June 1997.

[Robe01] Gordon W. Roberts, “Metrics, Techniques and New Developments in Mixed-Signal Testing,” Tutorial in Design, Automation and Test in Europe Conference and Exhibition, DATE 2001.

[Rose98] R. Rosenberger and S. A. Huss, “A System Theoretic Approach to Behavioral Modeling and Simulation of Analog Functional Blocks,: DATE, pp: 721-728, 1998.

[Saab96] K. Saab, D. Marche, N. B. Hamida and B. Kaminska, “LIMSoft: Automatic Tool for Sensitivity Analysis and Test Vector Generation,” IEE Proc.-Circuits Devices Syst. Vol.143, No. 6, December 1996.

[Saab00] K. Saab, N. B. Hamida and B. Kaminska, “Parametric Fault Simulation and Test Vector Generation,” DATE 2000.

[Sach95] Manoj Sachdev, “A Realistic Defect-Oriented Testability Methodology for Analog Circuits,” Journal of Electronic Testion: Theory and Applications, Vol.6, pp:265-276, 1995.

[Sale94] Resve Saleh, Shyh-Jye Jou, and A. Richard Newton, “Mixed-Mode Simulation and Analog Multilevel Simulation,” Kluwer Academic Publishers, 1994.

[Sach98] Manoj Sachdef, “Defect-Oriented Testing for CMOS Analog and Digital Circuits,” Kluwer Academic Publishers, 1998.

[Schw89] A. F. Schwarz, “Computer-Aided Design of Microelectronic Circuits and Systems, Volume 1. General Introduction and Analog-Circuit Aspects,” Academic Press, 1989.

[Sebe95] C. Sebeke, J. P. Teixeira, M. J. Ohletz, “Automatic Fault Extraction and Simulation of Layout Realistic Faults for Integrated Analogue Circuits,” Proc. European Design and Test Conference (EDTC), pp:604-608, March 1995.

[Sebe96] Christian Sebeke, “Zur systematischen Fehlersimulation integrierter analoger Schaltungen,” Universität Hannover, Shaker Verlag, 1996.

[Sedr98] Adel S. Sedra and Kenneth C. Smith, “Microelectronic Circuits,: Oxford University Press, 1998.

[Sen79] Neeeraj Sen and Richard Saeks, “Fault Diagnosis for Linear Systems Via Multifrequency Measurements,” IEEE Trans. on Circuits ad Systems, VOL. CAS-26, NO.7, July 1979.

[Shi00] C.-J. Richard Shi and Xiang-Dong Tan, “Canonical Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams,” IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, VOL. 19, NO. 1, January 2000.

[Silv95] L. M Silveira, M. Kamon, and J. White, “Efficient Reduced-Order Modeling of Frequency-Dependent Coupling Inductances Associated with 3-D Interconnection Structures,” in Proc. IEEE/ACM Design Automation Conference, pp: 474-479, June 1995.

[Slam92] Mustapha Slamani and Bozena Kaminska, “Analog Circuit Fault Diagnosis Based on Sensitivity Computation and Functional Testing,” IEEE Design & Test of Computers, pp:30-39, March 1992.

[Slam94] Mustapha Slamani and Bozena Kaminska, “Multifrequency Testability Analysis for Analog Circuits,” Proc. of VLSI Test Symposium, pp: 54-59, 1994.

[Slam95] Mustapha Slamani and Bozena Kaminska, “Multifrequency Analysis of Faults in Analog Circuits,” IEEE Design & Test of Computers, pp:70-80, Summer 1995.

[Slam96] M. Slamani and B. Kaminska, “Fault Observation Analysis of Analog Circuits in Frequency Domain,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 43, NO. 2, February 1996.

[Soma90] M. Soma, “A Design for Testability Methodology for Active Analog Filters,” International Test Conference, pp:183-192, September 1990.

[Soma94] M. Soma and V. Kolarik, “A Design for Test Technique for Switched Capacitor Filters,’ VLSI Test Symposium, pp: 42-47, April 1994.

[Soma96a] Mani Soma, “Challenges in Analog and Mixed-Signal Fault Models.” IEEE Circuits & Devices, January 1996.

[Soma96b] M. Soma, “Automatic Test Generation Algorithms for Analogue Circuits,” IEE Proc. Circuits Devices Syst., Vol.143, Vo.6, December 1996.

[Soma96c] Mani Soma and IEEE P1149.4 WG, “Review of IEEE P1149.4 Mixed-Signal Test Bus Standard,” Proceeding IEEE Northcon, pp: 320-323, Nov. 1996.

[Soma01] Mani Soma, Sam Huynh, Jinan Zhang, Seongwon Kim and Giri Devarayanadurg, “Hierarchical ATPG for Analog Circuits and Systems,” IEEE DEsign & Test of Computers, January-February 2001.

[Somm99] Ralf Sommer, Manfred Thole, Thomas Halfmann, and Tim Wichkann, “Symbolic Modeling and Analysis of Analog Integrated Circuits,” Proc. on European Conference on Circuit Theory, Sept. 1999.

[Somm03] Ralf Sommer, Manfred Thole, Eckhard Hennig, Hans Zapf, “Schaltungsfehleridentifikation mit symbolischer Analyse im industriellen Designflow,” in 7. ITG/GMM-Diskussionssitzung ANALOG 03, pp: 37-42, Heilbronn 10-12 September 2003.

[Soud90] T. M. Souders and G. N. Stenbakken, “A Comprehensive Approach for Modeling and Testing Analog and Mixed-Signal Devices,” International Test Conference,1990

[Spaa95] John van Spaandonk, “Application of the Singular Value Decomposition to the Testing of Analog Circuits,” International Mixed Signal Testing Workshop, pp:159-164, 1995.

[Spaa96a] John van Spaandonk and T.A.M. Kevennarr, “Selecting Measurements to Test the Functional Behavior of Analog Circuits,” Journal of Electronic Testing: Theory and Applications, 9, pp:9-18, 1996.

[Spaa96b] Johannes van Spaandonk, “A Test Method for Analog Circuits Using Sensitivity Analysis and the Singular Value Decomposition,” Diss., Technische Universiteit Eindhoven, 1996.

[Spen88] Robert Spence and Randeep Singh Soin, “Tolerance Design of Electronic Circuits,” Addison-Wesley Publishing Company, 1998.

[Stan02] M. Stancic and H. G. Kerkhoff, “Testability-Analysis Driven Test-Generation of Analogue Cores,” International Mixed Signal Testing Workshop, pp: 103-107, 2002.

[Star00] J. A. Starzky, J. Pang, S. Manetti, M.C. Piccirilli, and G. Fedi, “Finding Ambiguity Groups in Low Testability Analog Circuits,” IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications, VOL. 47, NO. 8, August 2000.

[Sten87] G. N. Stenbakken and T. M. Souders, “Test-Point Selection and Testability Measures via QR Factorization of Linear Models,” IEEE Trans. on Instrumentation and Measurement. VOL.IM-36, NO. 2, June 1987.

[Sten89] G. N. Stenbakken, T. M. Souders, and G. W. Stewart, “Ambiguity Groups and Testability,” IEEE Trans. on Instrumentation and Measurement. VOL.38, NO. 5, Oct. 1989.

[Sten91] G. N. Stenbakken and T. M. Souders, “Linear Error Modeling of Analog and Mixed-Signal Devices,” International Test Conference, pp: 573-581, 1991.

[Stra97] B. Straube, W. Vermeiren and Udo Namyslo, “On Problems with Hierarchical Analogue Fault Simulation,” European Test Workshop, May, 1997.

[Stra00] B. Straube, B. Müller, W. Vermeiren, Chr. Hoffmann, S. Sattler, “Analogue Fault Simulation by aFSIM,” DATE 2000, User Forum, pp: 27-30, 2000.

[Stra01] B. Straube, W. Vermeiren, H. Albustani, V. Spenke, “Multi-Level Hierarchical Analogue Fault Simulation with aFSIM,” IEEE International Mixed Signal Testing Workshop, pp: 174-180, 2001.

[Stra02] B. Straube and W. Vermeiren, “A Nullator-Norator-Based Analogue Circuit DC-Test Generation Approach,” IEEE International Mixed Signal Testing Workshop, pp: 133-136, 2002.

[Stra03] B. Straube and W. Vermeiren, “A DC-Test Generation Approach to Nonlinear Analogue Networks by Means of Nullators and Norators,” European Test Workshop, pp: 99-100, 2003.

[Su96] Kendall L. Su, “Analog Filters,” Chapman & Hall, 1996.

[Sunt96] S.K. Sunter, “Cost/Benefit Analysis of the P1149.4 Mixed-Signal Test Bus,” IEE Proc.-Circuits Devices Syst. Vol.143, No. 6, December 1996.

[Sunt00] Stephen K. Sunter, “IC Techniques for Mixed-Signal DFT and BIST,” Tutorial in Internalional Test Conference, 2000.

[Sunt99] S. Sunter, “The P1149.4 Mixed-Signal Test Bus: Ready to Use,” Mini-Tutorial, IEEE International Mixed Signal Testing Workshop, pp: 117-121, 1999.

[Tian98] Michael W. Tian and C.-J. Richard Shi, “Efficient DC Fault Simulation of Nonlinear Analog Circuits,” DATE, pp: 899-904, 1998.

[Tone93] Michael F. Toner and Gordon Roberts, “A BIST Scheme for a SNR, Gain Tracking and Frequency Response Test of a Sigma-Delta ADC,” IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing, VOL. 42, NO. 1, January 1993.

[Vari97] P. N. Variyam and A. Chatterjee, “FLYER: Fast Fault Simulation of Linear Analog Circuits Using Polynomial Waveform and Perturbed State Representation,” International Conference on VLSI Design, pp: 408-412, Jan. 1997.

[Vari00] Pramodchandran N. Variyam and A. Chatterjee, “Digital-Compatible BIST for Analog Circuits Using Transient Response Sampling,” IEEE Design & Test of Computers, July-September, 2000.

[Veil95] Benoît R. Veillette and Gordon W. Roberts, “High Frequency Sinusiodal Generation Using Delta-Sigma Modulation Techniques,” ISCAS 95, pp: 637-640, 1995.

[Vinn98] Bapiraju Vinnakota, “Analog and Mixed-Signal Test.” Prentice-Hall, Inc, 1998.

[Vlac94] Jiri Vlach and Kishore Singha, “Computer Methods for Circuit Analysis and Design,” Van Nostrand Reinhold, 1994.

[Vlac03] Jiri Vlach and John Choma, “Analysis in the Frequency Domain,” Chapter 21 in The Circuits and Filters Handbook, Ed. by Wai-Kai Chen, Second Edition, CRC Press and IEEE Press, 2003.

[Wey87] Chin-Long Wey, “Design of Testability for Analogue Fault Diagnosis,” International Journal of Circuit Theory and Applications, VOL.15, pp:123-142, 1987.

[Wolf99] Stephen Wolfram, “MATHEMATICA Version 4,” Cambridge University Press, 1999.

[Walk86] H. Walker and W. Stephen “VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits,” IEEE Trans. on Computer-Aided Design, VOL. CAD-5, NO. 4, October 1986.

[Wors00] M. Worsman and M. W. T. Wong, “Non-Linear Analog Circuit Fault Diagnosis with Large Change Sensitivity,” International Journal of Circuit Theory and Applications, Vol. 28, Issue. 3, pp: 281-303, May-June 2000.

[Xing98] Y. Xing, “Defect-Oriented Testing of Mixed-Signal ICs: Some Industrial Experience,” International Test Conference, pp: 678-687, 1998.

[Yang99] Z.R. Yang and Zwolinski, “Fast, Robust DC and Transient Fault Simulation for Nonlinear Analogue Circuits,” DATE, pp:244-248, 1999.

[Yoon99] Heebyung Yoon, Junwei Hou, Swapan K. Bhattacharya, Abhijit Chatterjee and Madhavan Swaminathan, “Fault Detection and Automated Fault Diagnosis for Embedded Integrated Electrical Passives,” Journal of VLSI Signal Processing 21, 265-176, 1999.

[Zhan99] Jinyan Zhang, Sam Huynh and Mani Soma, “A Test Point Insertion Algorithm for Mixed Signal Circuits,” Proc. of VLSI Test Symposium, pp: 319-324, 1999.

[Zwol97] M. Zwolinski, A. D. Brown and C.D. Chalk, “Concurrent Analogue Fault Simulation,” International Mixed Signal Testing Workshop, pp:42-47, June 1997.